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High-voltage gain dc–dc boost converter with coupled inductors for photovoltaic systems

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Abstract: This study presents the analysis, design and experimental evaluation of a high-voltage gain dc–dc converter applied to photovoltaic (PV) systems. A PV module rated at 17 V is connected to the input side, whereas the converter is responsible for stepping the voltage up to 311 V with the achievement of maximum power point tracking (MPPT). An experimental prototype rated at 100 W is implemented, which does not employ electrolytic capacitors, thus increasing the useful life of the arrangement and also allowing the incorporation of the converter to the PV module. Prominent advantages of the topology are low cost and simplicity in terms of the MPPT algorithm and the system implementation, which are mandatory characteristics for renewable energy applications.

1 Introduction

Several types of applications such as uninterruptible power systems and adjustable-speed drives often demand the low dc voltage from batteries, photovoltaic (PV) panels, fuel cells and small wind turbines to be stepped up [1]. Typical low voltages range from 12 to 125 V and must be increased to 300 or 440 V so that a dc bus is obtained to supply a dc–ac stage [2].

The increasing demand for renewable energy in distributed generation systems has led to the development of several novel converter topologies. Typically high-frequency isolated converters can provide voltage step-up by adjusting the proper turns ratio, although the transformer is responsible for processing the total rated power, with consequent increase of size, weight and volume and reduction of efficiency [3]. Consequently, non-isolated dc–dc converters with high-voltage gain have been highlighted as an alternative solution in distinct applications [4].

It is worth to mention that the conventional boost converter is not adequate in such applications because the high output voltage demands high value for the duty cycle, which on the other hand leads the main switch to remain turned on for long time intervals in the switching period. Since the current although the diode is high, serious drawbacks concerning the reverse recovery phenomenon exist. Several approaches based on the boost converter have been proposed in the literature, for example, cascaded converters, quadratic converters, interleaved converters, boost converters based on the three-state switching cell (3SSC) and boost converters with coupled inductors. Some important topologies will be analysed and discussed as follows.

Wide conversion ratio and reduced current ripple can be achieved if two or more conventional boost converters are cascaded [5]. Thus, it is possible to derive quadratic or even cubic converters, which have been extensively studied in the literature through several topological modifications [6–8]. Considering two cascaded stages, the input voltage can be stepped up by the first stage by using high duty cycle values. On the other hand, the second stage is able to operate with reduced duty cycle, thus allowing the minimisation of switching losses [9, 10]. However, robustness is compromised because of the need of multiple active switches, diodes, inductors and capacitors to achieve very high output voltages, whereas the control circuit must be carefully designed in this case [11]. Adequate control schemes can be also used to achieve the simultaneous control of the existing active switches [12, 13].

The multiple active switches in cascaded boost converters can be replaced by diodes in a generic single-switch approach [14]. Even though the ratio between the output voltage and the input voltage is equal to the product of the converters' static gains some significant drawbacks still exist. Considering that many topologies can be used, the global efficiency of the resulting structure is significantly reduced, what does not make the aforementioned topologies adequate for high-power applications. In cases where the output voltage is very high, the voltage stresses across the main switch and the boost diode in the last stage are appreciable, that is, equal to the output voltage, thus leading to the use of costly components and poor efficiency. The reverse recovery problem in such diode and also stability are also of major concern. Besides, increased complexity in terms of the control system is expected because of the high-order dynamics [15].

Interleaving is a typical solution in high-power high-current applications, with consequent improvement of performance and reduction of size, weight and volume of magnetics [16, 17], and some approaches regarding the achievement of high-voltage gain have also been introduced [18–20]. For instance, the converter studied in [21] employs two boost converters coupled through an autotransformer with unity turns ratio and opposite polarity so that the current is equally shared between the switches. Besides, voltage doubler characteristic is achieved. Even though the current stress through the switches is reduced, the respective voltage stress is less than or equal to half the total output voltage. Isolated drive circuitry must also be employed in this case. Other topologies using the interleaving technique are proposed in [22], where voltage multiplier cells (VMCs) are adopted to provide high-voltage gain and reduced voltage stress across the semiconductor elements. In this case, interleaving allows the operation of the multiplier stages with reduction of the current stress through the devices. Besides, the sizes of input inductors and capacitors are drastically reduced. The voltage stress across the main switches is limited to half of the output voltage for a

single multiplier stage. However, high component count is necessary, with the addition of a snubber circuit because of sum of the reverse recovery currents through the multiplier diodes and consequent increase of conduction losses.

Considering the use of the 3SSC [23], several non-isolated dc–dc converters with high-voltage gain characteristic have been proposed so far. A novel family of dc–dc converters using the 3SSC and VMCs was introduced in [24], while significant advances have been achieved in terms of reduced voltage stress across the main switches, reduced input ripple current, minimisation of size, weight and volume associated to magnetics, reduced switching losses and high efficiency over the entire load range. However, the reduced useful life of series capacitors and high component count can be pointed out as drawbacks. The topology in [25] corresponds to a boost converter using the 3SSC and a secondary winding, where the advantages claimed by using the 3SSC are obtained [24]. Besides, for a given duty cycle, the static gain can be changed by properly adjusting the turns ratio without increasing the voltage stress for the active switches, which are less than half of the output voltage. In this structure, part of the input power is directly transferred to the load without being processed by the active switches, thus implying reduced conduction losses. Unfortunately, this converter does not work properly when the duty cycle is lower than 0.5 because of magnetic induction issues.

An extensive review on non-isolated boost converters is presented in [26], where the use of coupled inductors to achieve high-voltage gain is analysed, since they can act as a transformer that allows increasing the static gain in dc/dc converters [27, 28]. Numerous topologies have been introduced, for example, the dc–dc converter using a voltage doubler cell with reduced voltage stress across the main switch [29]. A bidirectional buck/boost converter is also studied in [30], where a passive clamp circuit is employed to minimise the voltage stress regarding the active switches. In both structures, the main drawback lies in high component count and complexity if compared with other simpler approaches existent in the literature.

A boost-based non-isolated dc–dc converter with coupled inductors is proposed in [31, 32], whose distinct advantages are simplicity, low component count, high-voltage step-up ability and low-voltage stress across the main switch. Even though efficiency is high, a passive snubber is necessary, whose design procedure is typically complex. Besides, the voltage stress across the output diode is appreciable.

Another interesting structure has been analysed in [33], as shown in Fig. 1*a*, which deserves some attention. Considering that the voltage across a single PV module is 17.4 V and must be stepped up to 311 V, simulation tests carried out in simulation program with integrated circuit emphasis software have shown that the maximum voltage across diode D_1 is very high, that is, about 800 V. This may lead to the use of high-cost diodes that inherently present high forward voltage drop and also low switching speed.

To solve this limitation and obtain a modular solution for PV systems that aggregate low cost and simplicity associated to high-voltage gain, this paper proposes the modified version of the topology represented in Fig. 1*b*, where three components are added, that is, diode D_3, inductor L_3 (which is coupled to L_1 and L_2) and one capacitor C_3. In this case, the voltage across the diode is divided by two, thus allowing the use of ultrafast diodes.

Even though the original topology shown in Fig. 1*a* has been thoroughly studied in [33], only the operation in continuous conduction mode (CCM) is investigated. Besides, resonance may occur between the leakage inductances of L_1 and C_g when the inductor is not fully discharged, as the converter may not operate adequately, which also occurs in the modified topology. Aiming to overcome this limitation, the converter in Fig. 1*b* must operate in discontinuous conduction mode (DCM), so that inductor L_1 can be fully discharged. It is also worth to mention that the aforementioned study has not been developed in [33].

Within this context, this paper proposes the DCM high-voltage gain dc–dc converter with coupled inductors shown in Fig. 1*b* to step the voltage up from 17.4 V (i.e. the voltage across a single module) to 311 V. Initially, the qualitative analysis and design procedure are developed, so that an experimental prototype rated at 100 W can be implemented and evaluated with the proper discussion of the most relevant results. The converter is also responsible for maximum power point tracking (MPPT) and does not use electrolytic capacitors, thus increasing the lifetime of the structure in a robust and low-cost solution for modular PV systems.

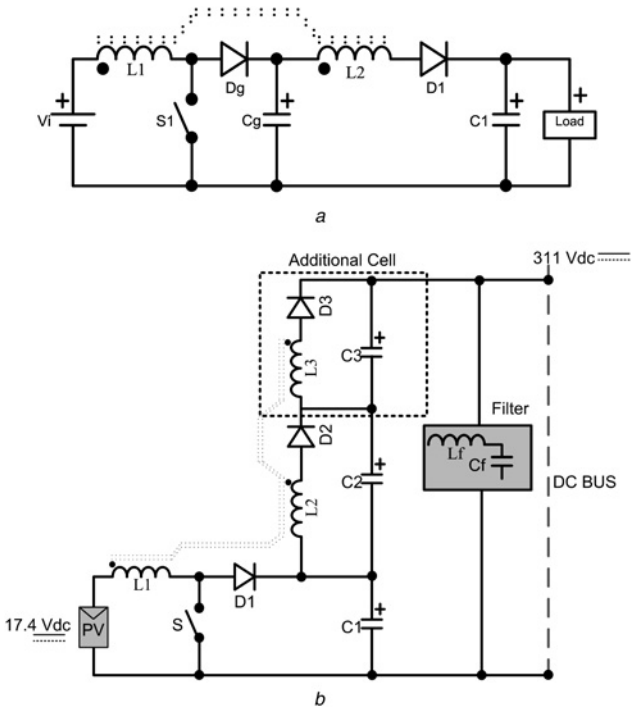

Fig. 1 *High-voltage gain dc–dc converters based using coupled inductors*
a Topology studied in [33]
b Proposed topology

2 Qualitative analysis of the proposed converter

The equivalent circuits that represent the converter operation for one switching cycle are shown in Figs. 2*a–c* and described as follows. The corresponding main theoretical waveforms are shown in Fig. 2*d* and represent the operation in DCM. Besides, the following assumptions are made:

- Parasitic elements such as leakage inductances and series resistances are neglected.
- All capacitors are large enough to maintain the voltages across them constant.
- The current ripples are neglected.
- All semiconductors are ideal.
- The magnetic coupling coefficient is unity.

The following parameters are also defined in Fig. 2*d*:

I_i and I_o are the input current and output current, respectively;
I_{C_1}, I_{C_2} and I_{C_3} are the currents through capacitors C_1, C_2 and C_3;
I_{L_1} and $I_{L_2} = I_{L_3}$ are the currents through inductors L_1, L_2 and L_3;
V_{C_1} is the voltage across capacitor C_1;
V_{L_2} is the voltage across inductor L_2;
$V_{g(S)}$ is the gating signal applied to switch S;
I_S is the current through switch S;
I_{D_1} is the current through diode D_1;
V_S is the voltage across switch S;
V_{D_1} is the voltage across boost diode D_1; and

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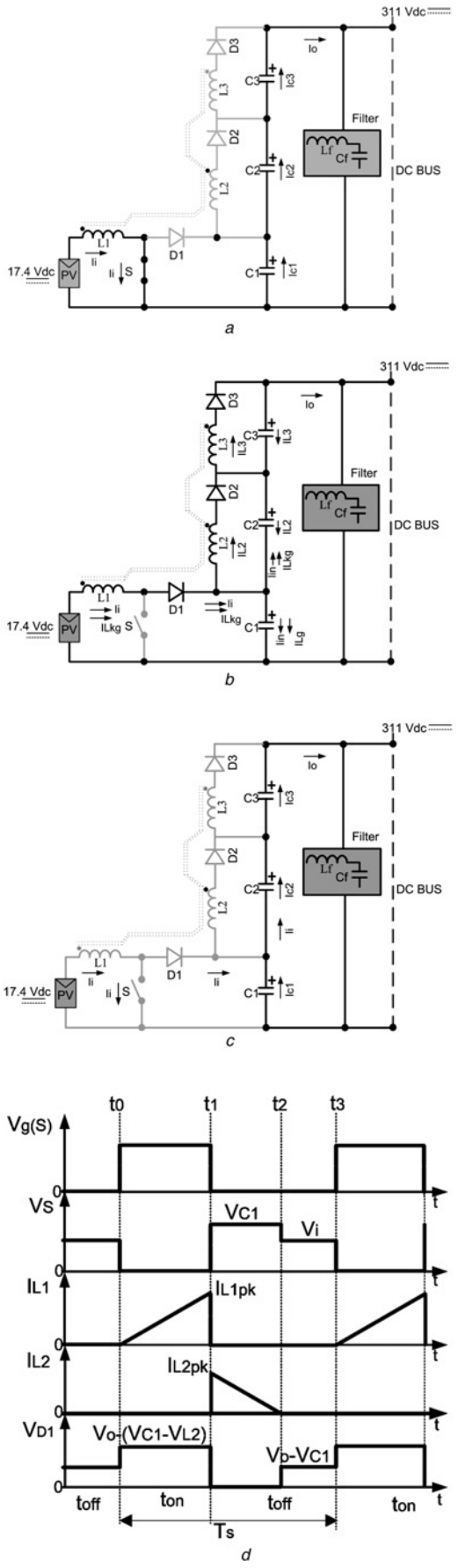

Fig. 2 *Qualitative analysis of the proposed converter in DCM*

a First stage
b Second stage
c Third stage
d Main theoretical waveforms

V_o is the output voltage.

First stage [t_0, t_1] (Fig. 2a): Switch S is turned on and energy is stored in inductor L_1. Besides, capacitors C_1, C_2 and C_3 are discharged delivering power to the dc bus.
Second stage [t_1, t_2] (Fig. 2b): Switch S is turned off and inductor L_1 is discharged, consequently charging inductors L_2 and L_3. Even though L_1 is fully discharged, it still delivers some energy from the PV panel to capacitor C_1. This is because of the leakage inductance inherent to inductor L_1, which is charged during the first stage and now discharged. It can be also seen that currents I_i, I_{L_2} and I_{L_3} charge the output capacitors, thus keeping the output voltage constant. Although the capacitors are charged, they contribute to the output current because charging process is very fast.
Third stage [t_2, t_3] (Fig. 2c): Switch S is off, whereas inductors L_1 and L_2 are fully discharged and the voltages across them are zero. Capacitor C_1 provides energy to the load since all diodes are reverse biased and there is no energy transfer from the input voltage source to the capacitors. The output voltage remains nearly constant in this case.

3 Design procedure

From the analysis of the operating stages, it is possible to determine the expressions for the accurate design of the converter elements. The mathematical manipulations that lead to the expressions will not be presented in detail, although they can be derived from Fig. 2. Let us consider the design specifications given in Table 1, which will be used in the implementation of the experimental prototype.

3.1 Inductors

The static gain of the converter in DCM is

$$\frac{V_o}{V_{i(min)}} = \frac{1}{1-D_{max}} + \frac{N_2}{N_1}\cdot\left(\frac{1}{1-D_{max}} - 1\right) \quad (1)$$

where N_1 and N_2 are the number of turns of inductors L_1 and L_2, respectively. It is also worth to mention that the same number of turns is adopted for inductors L_2 and L_3, that is, $N_2 = N_3$. Substituting the parameters in Table 1 in (1) gives

$$\frac{N_2}{N_1} \cong 29 \quad (2)$$

The inductance values that represent the boundary condition between CCM and DCM are

$$L_1 = \frac{V_{i(min)}\cdot T_s}{2\cdot P_o}\cdot\left[V_{i(min)}\cdot D_{max}^2 + \frac{N_1^2\cdot(1-D_{max})^2}{(N_1+N_2)^2}\cdot\left(V_o - V_{i(min)}\right)\right] = 2.584\ \mu H \quad (3)$$

Table 1 Design specifications for the step-up converters

Parameter	Specification
rated output power	$P_o = 100$ W
minimum input voltage	$V_{i(min)} = 10$ V
rated input voltage	$V_i = 17$ V
output voltage	$V_o = 311$ V
maximum duty cycle	$D_{max} = 0.5$
rated duty cycle	$D = 0.29$
switching frequency	$f_s = 50$ kHz
ripple voltage across the capacitors	$\Delta V_{C_1} = \Delta V_{C_2} = \Delta V_{C_3} = 1\%\ V_o$

$$L_2 = L_3 = \left(\frac{N_2 + N_1}{N_1}\right)^2 \cdot L_1 = 2.384\ \text{mH} \tag{4}$$

where $V_{i(min)}$ is the minimum output voltage, T_s is the switching period and P_o is the output power.

The peak currents through the inductors are

$$I_{L_1(pk)} = \frac{V_i \cdot D \cdot T_s}{L_1} = 38.16\ \text{A} \tag{5}$$

$$I_{L_2(pk)} = I_{L_3(pk)} = \frac{(V_o - V_i) \cdot t_d}{L_2} = 1.361\ \text{A} \tag{6}$$

where

$$t_d = \frac{L_2 \cdot I_{L_1(pk)}}{(V_o - V_i)} \cdot \frac{N_1}{(N_1 + N_2)} \cong 10\ \mu\text{s} \tag{7}$$

Besides, the root-mean-square (rms) currents through the inductors are

$$I_{L_1(rms)} = \sqrt{\frac{1}{T_s}\int_0^{D \cdot T_s} \left(\frac{V_i \cdot t}{L_1}\right)^2 \cdot dt} = \frac{\sqrt{3 \cdot D^3} \cdot V_i}{f_s \cdot L_1} = 11.866\ \text{A} \tag{8}$$

$$\begin{aligned} I_{L_2(rms)} &= I_{L_3(rms)} \\ &= \sqrt{\frac{1}{T_s}\int_0^{t_d} \left[\frac{(V_o - V_i) \cdot t}{L_1} \cdot \left(\frac{N_1}{N_1 + N_2}\right)\right]^2 \cdot dt} \\ &= \frac{\sqrt{3 \cdot f_s \cdot t_d^3} \cdot (V_o - V_i)}{3 \cdot L_1} \cdot \left(\frac{N_1}{N_1 + N_2}\right)^2 = 0.521\ \text{A} \end{aligned} \tag{9}$$

3.2 Capacitors

From the theoretical analysis, capacitor C_1 can be calculated according to the following expression

$$C_1 = \frac{I_{L_2(pk)} \cdot D_{nom}}{2 \cdot f_s \cdot \Delta V_{C_1}} \cong 2.2\ \mu\text{F} \tag{10}$$

where I_o is the output current, f_s is the switching frequency and ΔV_{C_1} is the ripple voltage across C_1.

Besides, capacitors C_2 and C_3 can be determined as

$$C_2 = C_3 = \frac{10 \cdot P_o}{V_o{}^2 \cdot 2 \cdot \pi \cdot f_s} \cong 220\ \text{nF} \tag{11}$$

where f_s is the switching frequency.

3.3 Switch S

The voltage and current stresses for the main switch S can be obtained from expressions (12) to (15)

$$V_{S(max)} = \frac{V_i}{1 - D} \cong 24\ \text{V} \tag{12}$$

$$I_{S(avg)} = \frac{1}{T_s}\int_0^{D_{max} \cdot T_s} \left(\frac{V_i \cdot t}{L_1}\right) \cdot dt = \frac{V_i \cdot D_{nom}^2 \cdot T_s}{2 \cdot L_1} = 5.534\ \text{A} \tag{13}$$

$$I_{S(rms)} = I_{L_1(rms)} = 11.866\ \text{A} \tag{14}$$

$$I_{S(max)} = I_{L_1(pk)} = 38.16\ \text{A} \tag{15}$$

3.4 Diodes

The maximum reverse voltages across the diodes are

$$V_{D_1(max)} = V_{C_1} = 27.27\ \text{V} \tag{16}$$

$$\begin{aligned} V_{D_2(max)} = V_{D_3(max)} &= V_o - \left(\frac{V_{i(min)}}{1 - D} - V_{i(min)} \cdot \frac{N_2}{2 \cdot N_1}\right) \\ &= 436\ \text{V} \end{aligned} \tag{17}$$

The average, rms and maximum currents through diode D_1 are

$$\begin{aligned} I_{D_1(avg)} &= \frac{1}{T_s}\int_0^{D_{max} \cdot T_s} \left[\frac{\left(V_{s(max)} - V_{i(min)}\right) \cdot t \cdot N_1^2}{(N_1 + N_2)^2 \cdot L_1}\right] \cdot dt \\ &= \frac{D_{max}^2 \cdot \left(V_{s(max)} - V_{i(min)}\right)}{2 \cdot f_s \cdot L_1} \cdot \left(\frac{N_1}{N_1 + N_2}\right)^2 = 15\ \text{mA} \end{aligned} \tag{18}$$

$$\begin{aligned} I_{D_1(rms)} &= \sqrt{\frac{1}{T_s}\int_0^{t_d} \left[\frac{\left(V_{s(max)} - V_{i(min)}\right) \cdot t \cdot N_1^2}{(N_1 + N_2)^2 L_1}\right]^2 \cdot dt} \\ &= \frac{\sqrt{3 \cdot f_s \cdot t_d^3} \cdot \left(V_{s(max)} - V_{i(min)}\right)}{3 \cdot L_1} \cdot \left(\frac{N_1}{N_1 + N_2}\right)^2 \cong 25\ \text{mA} \end{aligned} \tag{19}$$

$$I_{D_1(max)} = \frac{\left(V_{s(max)} - V_i\right) \cdot t_d}{L_2} \cong 65\ \text{mA} \tag{20}$$

The average, rms and maximum current through diodes D_2 and D_3 are

$$\begin{aligned} I_{D_2(avg)} = I_{D_3(avg)} &= \frac{1}{T_s}\int_0^{D_{max} \cdot T_s} \left[\frac{\left(V_o - V_{i(min)}\right) \cdot t \cdot N_1^2}{(N_1 + N_2)^2 L_1}\right] \cdot dt \\ &= \frac{D_{max}^2 \cdot \left(V_o - V_{i(min)}\right)}{2 \cdot f_s \cdot L_1} \cdot \left(\frac{N_1}{N_1 + N_2}\right)^2 \cong 324\ \text{mA} \end{aligned} \tag{21}$$

$$\begin{aligned} I_{D_2(rms)} = I_{D_3(rms)} &= \sqrt{\frac{1}{T_s}\int_0^{t_d} \left[\frac{(V_o - V_i) \cdot t \cdot N_1^2}{(N_1 + N_2)^2 \cdot L_1}\right]^2 \cdot dt} \\ &= \frac{\sqrt{3 \cdot f_s \cdot t_d^3} \cdot (V_o - V_i)}{3 \cdot L_1} \cdot \left(\frac{N_1}{N_1 + N_2}\right)^2 \cong 533\ \text{mA} \end{aligned} \tag{22}$$

$$I_{D_2(max)} = I_{D_3(max)} = \frac{(V_o - V_i) \cdot t_d}{L_2} = 1.394\ \text{A} \tag{23}$$

4 Experimental results

To validate the theoretical assumptions, the experimental prototype depicted in Fig. 3 was developed, whose elements are described in Table 2. A single PV module KC65T manufactured by Kyocera and described in Table 3 was used in the experimental tests, while a well-known MPPT algorithm was implemented. Perturb and observe (P&O) was chosen because of its simplicity, which consolidates it as a viable commercial approach [35, 36]. The measured waveforms were collected within the period from 12:00 to 15:00, while energy is injected in a constant voltage dc bus as shown in Fig. 4.

P&O is one the simplest MPPT methods [37–40] with excellent performance and can be easily implemented in low-cost systems [40]. Some more sophisticated methods are based on the same

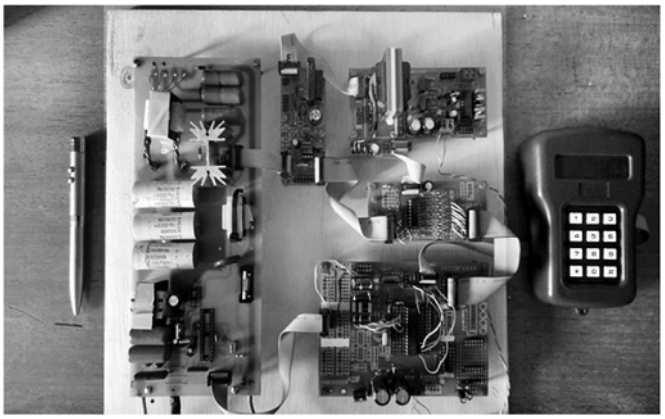

Fig. 3 *Experimental prototype*

principle employed in P&O method, for example, hill climbing (HC) and modified HC. Fig. 4 shows the flowchart representation of P&O technique, where $V(k)$ and $I(k)$ are the present voltage and current of the PV array and $V(k–1)$ and $I(k–1)$ are their previous values, respectively. The principle lies in disturbing the voltage or the current of the PV module and observing its effect on the resulting power. The algorithm compares the power of the previous step with that for next step so that it can increase or decrease the voltage or current. This method changes the reference value, which can be a constant current or voltage. The operating point is then periodically moved towards the maximum power point (MPP) by either increasing or decreasing the array voltage or current.

Fig. 5*a* shows some waveforms that describe the MPPT operation, which is achieved very fast, that is, in about 500 ms. It can be stated that the input current and input voltage are close to the rated values so that maximum power can be extracted. The input power can be obtained by multiplying the aforementioned waveforms.

Fig. 5*b* presents the ripple voltage across the input capacitor that is typically connected in parallel with the PV array. The ripple voltage is about 0.5 V, whereas a 10 μF polypropylene capacitor is used, what may increase the useful life of the PV system if compared with electrolytic counterparts.

The operation of the converter in DCM can be clearly seen in Fig. 5*c*, where inductors L_1 and L_2 are fully discharged. When the current through inductor L_1 increases, it is possible to note some oscillation, which is caused by the leakage inductance existent in EE-type ferrite cores. Besides, it is damped around the peak value of the current, according to Fig. 5*d*. Unlike the theoretical analysis, the waveforms regarding L_1 and L_2 present some overlapping, which is probably because of the leakage inductance of the inductors.

The voltage across the main switch is shown in Fig. 6*a*, whose maximum value is about 50 V. The oscillatory behaviour is because of the high magnetic leakage, which is also typical in high-voltage gain flyback topologies based on EE cores. To damp it, it is possible to use toroidal cores in the coupled inductors.

It is possible to see in Fig. 6*b* that the addition of another cell to the topology in Fig. 1*a* has allowed the limitation of the maximum voltage across diode D_3 to about 400 V. The same oscillatory

Table 2 Components used in the experimental prototype

Parameter	Specification
turns ratio of the coupled inductor	$N_2 = N_3 = 29 \cdot N_1$
inductors	$L_1 = 2.583$ μH, core NEE by Thornton and $N_{L_1} = 1$ turns – 20 × American wire gauge (AWG) 22 $L_2 = L_3 = 2.34$ mH, core NEE by Thornton and $N_{L_2} = N_{L_3} = 29$ turns – 20 × AWG 22
capacitors	$C_1 = 2.2$ μF, polypropylene ,400 V and model B32594 by Epcos $C_2 = C_3 = 220$ nF, polypropylene, 630 V and model B32694 by Epcos
main switches	metal–oxide semiconductor field effect transistor IRF3207 by international rectifier
diodes $D_1, \ldots, D_3$	D_1 – 1N4002, 1 A and 100 V by Fairchild D_2 and D_3 – UF4005 and 1 A, 600 V by Fairchild

Table 3 Typical electric characteristics of PV module KC65T under standard test conditions [34]

Method	Extracted energy
maximum power (P_{max})	65 W
voltage at P_{max} (V_{mp})	17.4 V
current at P_{max} (I_{mp})	3.75 A
short-circuit current (I_{sc})	3.99 A
open-circuit voltage (V_{oc})	21.7 V
temperature coefficient of I_{sc}	1.59×10^{-3} A/°C
temperature coefficient of V_{oc}	-8.21×10^{-2} V/°C

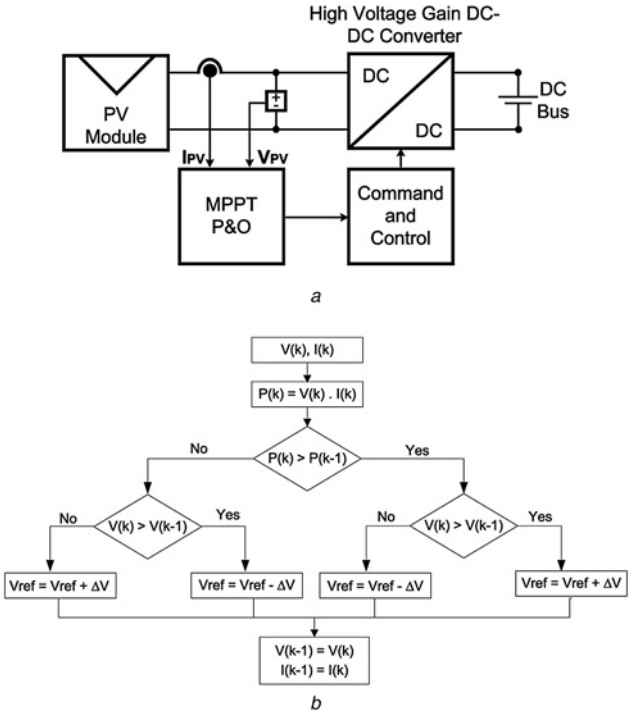

Fig. 4 *P&O algorithm*

a Control system
b Flowchart

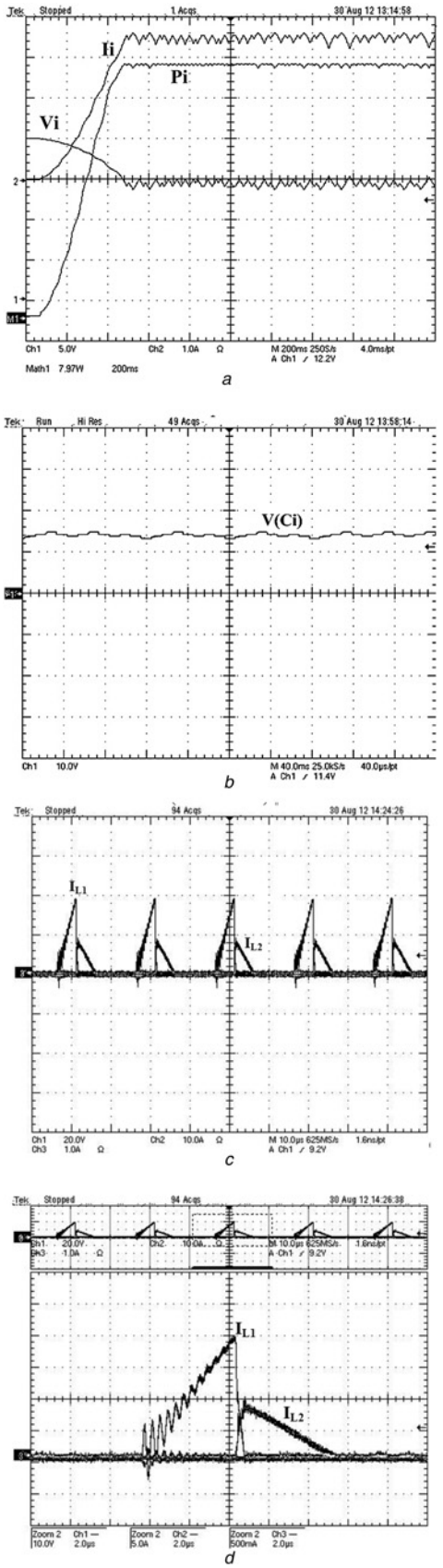

Fig. 5 *Experimental results*

a Input current, input voltage and input power (I_i – 1 A/div., V_i – 5 V/div., P_i – 8 W/div. and time – 200 ms/div.)
b Voltage across input capacitor $C_i = 10$ μF (V_{C_i} – 10 A/div. and time – 40 ms/div.)
c Currents through inductors L_1 and L_2 (I_{L_1} – 20 A/div., I_{L_2} – 1 A/div. and time – 10 μs/div.)
d Detailed view of the currents through inductors L_1 and L_2 (I_{L_1} – 10 A/div., I_{L_2} – 500 mA/div. and time – 2 μs/div.)

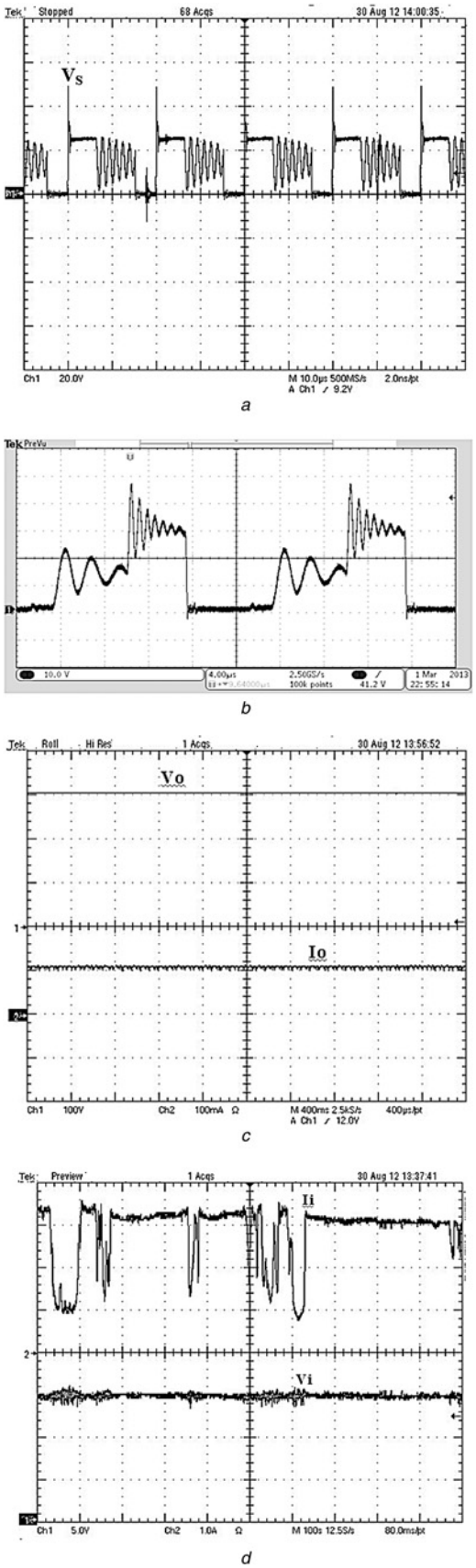

Fig. 6 *Experimental results*

a Voltage across switch S (V_S – 20 V/div. and time – 10 μs/div.)
b Voltage across diode D_3 (V_{D_3} – 100 V/div. and time – 4 μs/div.)
c Output voltage and output current (V_o – 100 V/div., I_o – 100 mA/div. and time – 400 ms/div.)
d Input voltage and input current recorded during about 10 min (V_i – 5 V/div., I_i – 100 mA/div. and time – 100 s/div.)

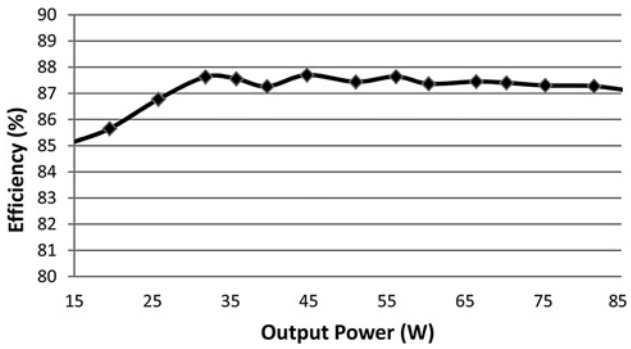

Fig. 7 *Efficiency curve*

behaviour exists in this case because of the magnetic leakage. The output voltage and output current are presented in Fig. 6*c*, where it can be seen that their respective ripples are negligible.

After acquiring the aforementioned waveforms, some data regarding the closed-loop operation of the converter acting as a maximum power point tracker were recorded during about 10 min, whereas the resulting profile of the input voltage and the input current is presented in Fig. 6*d*. It is possible to see that the input current varies because it is proportional to the solar irradiance. When the sun is partially covered by clouds, the current through the PV module decreases significantly, but the actuation of the MPPT algorithm is fast when the solar irradiance level increases.

Finally, the efficiency curve of the converter operating at 50 kHz as a function of the output power is shown in Fig. 7. It can be seen that average efficiency is about 87.1%. Of course, efficiency can be further improved by reducing the switching frequency and/or using toroidal cores.

5 Conclusion

This paper has presented a high-voltage gain dc–dc converter operating in DCM, which does not use electrolytic capacitors and can be used to achieve MPPT in PV systems. The high reverse voltage across the output diode in the original topology because of the resonance between the inductor parasitic inductance and the switch intrinsic capacitance can be alleviated by adding another cell to the converter, which is composed of an inductor, a capacitor and a diode. Low component count, reduced dimensions and intrinsic simplicity are distinct advantages of the introduced topology.

The proposed converter is adequate for low input voltages and low-power applications, where a high-voltage dc bus is necessary to supply an inverter. It is worth to mention that a single PV module has been employed, while high-voltage conversion ratio is obtained. The leakage inductance of the coupled inductor is somewhat small and is not supposed to influence the converter operation significantly.

The converter efficiency is about 87.5% at the rated condition specified in Table 1, which is not as high as that achieved in [31, 32] (about 95.8% at 320 W), where a passive regenerative is used to minimise switching losses. However, it should be considered that the input voltage in the proposed topology is low, that is, $V_i = 17$ V, whereas the output voltage is high, that is, $V_o = 311$ V. The average input current at rated condition is $I_i = 5.82$ A, being much higher than the average output current $I_o = 322$ mA. In this case, efficiency tends to decrease at low power levels, especially because conduction losses in the semiconductors and the copper losses in the inductor increase with the square of the rms current, thus representing a significant amount of the input power.

It can be stated that the converter represents a low cost and robust solution for PV systems based on modular approaches, whereas a simple MPPT algorithm has proven to be very effective in this case. Finally, it is expected that efficiency can be further increased with the use of toroidal cores instead of EE counterparts.

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7 References

1 Ortega, M., Jurado, F., Valverde, M.: 'Novel topology for dc/dc unidirectional converter for fuel cell', *IET Power Electron.*, 2014, **7**, (3), pp. 681–691
2 Bascopé, R.P.T., Branco, C.G.C., Bascopé, G.V.T., Cruz, C.M.T., de Souza, F.A. A., Barreto, L.H.S.C.: 'A new isolated dc–dc boost converter using three-state switching cell'. Proc. Applied Power Electronics Conf. and Exposition, 2008, pp. 607–613
3 Barreto, L.H.S.C., Praça, P.P., Oliveira, D.S., Silva, R.N.A.L.: 'High-voltage gain boost converter based on three-state commutation cell for battery charging using PV panels in a single conversion stage', *IEEE Trans. Power Electron.*, 2014, **29**, (1), pp. 150–158
4 Abusara, M.A., Sharkh, S.M.: 'Design and control of a grid-connected interleaved inverter', *IEEE Trans. Power Electron.*, 2013, **28**, (2), pp. 748–764
5 Middlebrook, R.D.: 'Transformerless dc-to-dc converters with large conversion ratios', *IEEE Trans. Power Electron.*, 1988, **3**, (4), pp. 484–488
6 Novaes, Y.R., Rufer, A., Barbi, I.: 'A new quadratic, three-level, dc/dc converter suitable for fuel cell applications'. Proc. Power Conversion Conf. – Nagoya, 2007, pp. 601–607
7 Lopez-Santos, O., Martinez-Salamero, L., Garcia, G., Valderrama-Blavi, H., Mercuri, D.O.: 'Efficiency analysis of a sliding-mode controlled quadratic boost converter', *IET Power Electron.*, 2013, **6**, (12), pp. 364–373
8 Chen, S.-M., Liang, T.-J., Yang, L.-S., Chen, J.-F.: 'A cascaded high step-up dc–dc converter with single switch for microsource applications', *IEEE Trans. Power Electron.*, 2011, **26**, (4), pp. 1146–1153
9 Ye, Y.-m., Cheng, K.W.E.: 'Quadratic boost converter with low buffer capacitor stress', *IET Power Electron.*, 2014, **7**, (5), pp. 1162–1170
10 Patidar, K., Umarikar, A.C.: 'High step-up pulse-width modulation dc–dc converter based on quasi-Z-source topology', *IET Power Electron.*, 2015, **8**, (4), pp. 477–488
11 Huber, L., Jovanovic, M.M.: 'A design approach for server power supplies for networking applications'. Proc. IEEE Applied Power Electronics Conf. and Exposition, 2000, pp. 1163–1169
12 Haroun, R., Cid-Pastor, A., El Aroudi, A., Martinez-Salamero, L.: 'Synthesis of canonical elements for power processing in dc distribution systems using cascaded converters and sliding mode control', *IEEE Trans. Power Electron.*, 2014, **29**, (03), pp. 1366–1381
13 Haroun, R., El Aroudi, A., Cid-Pastor, A., Martínez-Salamero, L.: 'Synthesis of a power gyrator based on sliding mode control of two cascaded boost converters using a single sliding surface'. Proc. Tenth Int. Multi-Conf. on Systems, Signals & Devices, 2013, pp. 1–6
14 Demian Junior, A.E., Treviso, C.H.G., Gallo, C.A., Tofoli, F.L.: 'Non-isolated dc–dc converters with wide conversion range used to drive high-brightness LEDs'. Proc. Brazilian Power Electronics Conf., 2009, pp. 598–605
15 Vighetti, S., Ferrieux, J., Lembeye, Y.: 'Optimization and design of a cascaded dc/dc converter devoted to grid-connected photovoltaic systems', *IEEE Trans. Power Electron.*, 2012, **27**, (4), pp. 2018–2027
16 Barreto, L.H.S.C., Coelho, E.A.A., Farias, V.J., Oliveira, J.C., de Freitas, L.C., Vieira, J.B.Jr.: 'A quasi-resonant quadratic boost converter using a single resonant network', *IEEE Trans. Ind. Electron.*, 2005, **52**, (2), pp. 552–557
17 Jang, Y., Jovanovic, M.M.: 'Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end', *IEEE Trans. Power Electron.*, 2007, **22**, (4), pp. 1394–1401
18 Luo, Q.-m., Yan, H., Chen, S., Zhou, L.-w.: 'Interleaved high step-up zero-voltage-switching boost converter with variable inductor control', *IET Power Electron.*, 2014, **7**, (12), pp. 3083–3089
19 Nouri, T., Hosseini, S.H., Babaei, E., Ebrahimi, J.: 'Interleaved high step-up dc–dc converter based on three-winding high-frequency coupled inductor and voltage multiplier cell', *IET Power Electron.*, 2015, **8**, (2), pp. 175–189
20 Aquino, R.N.A.L.S., Tofoli, F.L., Praça, P.P., Oliveira, D.S.Jr., Barreto, L.H.S.C.: 'Soft switching high-voltage gain dc–dc interleaved boost converter', *IET Power Electron.*, 2015, **8**, (1), pp. 120–129
21 Yungtaek, J., Jovanovic, M.M.: 'New two-inductor boost converter with auxiliary transformer', *IEEE Trans. Power Electron.*, 2004, **19**, (1), pp. 169–175
22 Gules, R., Pfitscher, L.L., Franco, L.C.: 'An interleaved boost dc–dc converter with large conversion ratio'. Proc. IEEE Int. Symp. on Industrial Electronics, 2003, pp. 411–416
23 Torrico-Bascopé, G.V., Barbi, I.: 'Generation of a family of non-isolated DC–DC PWM converters using new three-state switching cell'. Proc. IEEE Power Electronics Specialists Conf., 2000, vol. 2, pp. 858–863
24 Tofoli, F.L., Oliveira, D.S.Jr., Torrico-Bascopé, R.P., Alcazar, Y.J.A.: 'Novel nonisolated high-voltage gain dc–dc converters based on 3SSC and VMC', *IEEE Trans. Power Electron.*, 2013, **27**, (9), pp. 3897–3907
25 Bascopé, G.V.T., Bascopé, R.P.T., Oliveira, D.S.Jr., Antunes, F.L.M., Araújo, S. V., Branco, C.G.C.: 'A high step-up dc–dc converter based on three-state

switching cell'. Proc. IEEE Int. Symp. on Industrial Electronics, 2006, pp. 998–1003
26 Li, W., He, X.: 'Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications', *IEEE Trans. Ind. Electron.*, 2011, **58**, (4), pp. 1239–1250
27 Mohammadi, M., Taheri, M., Milimonfared, J., Abbasi, B., Behbahani, M.R.M.: 'High step-up dc–dc converter with ripple free input current and soft switching', *IET Power Electron.*, 2014, **7**, (12), pp. 3023–3032
28 Nouri, T., Hosseini, S.H., Babaei, E.: 'Analysis of voltage and current stresses of a generalised step-up dc–dc converter', *IET Power Electron.*, 2014, **7**, (6), pp. 1347–1361
29 Hu, X., Gong, C.: 'A high voltage gain dc–dc converter integrating coupled-inductor and diode–capacitor techniques', *IEEE Trans. Power Electron.*, 2014, **29**, (2), pp. 789–800
30 Hsieh, Y.-P., Chen, J.-F., Yang, L.-S., Wu, C.-Y., Liu, W.-S.: 'High-conversion-ratio bidirectional dc–dc converter with coupled inductor', *IEEE Trans. Ind. Electron.*, 2014, **61**, (1), pp. 210–222
31 Wai, R.-J., Duan, R.-Y.: 'High step-up converter with coupled inductor', *IEEE Trans. Power Electron.*, 2005, **20**, (5), pp. 1025–1035
32 Wai, R.-J., Wang, W.-H., Lin, C.-Y.: 'High-performance standalone photovoltaic generation system', *IEEE Trans. Power Electron.*, 2008, **55**, (1), pp. 240–250
33 Zhao, Q., Lee, F.C.: 'High-efficiency, high step-up dc–dc converters', *IEEE Trans. Power Electron.*, 2003, **18**, (1), pp. 65–73
34 KC65T – High efficiency multicrystal photovoltaic module. Available at http://www.kyocerasolar.com/assets/001/5170.pdf. Accessed on 11 March 2014
35 Sera, D., Mathe, L., Kerekes, T., Spataru, S.V., Teodorescu, R.: 'On the perturb-and-observe and incremental conductance MPPT methods for PV systems', *IEEE J. Photovolt.*, 2013, **3**, (3), pp. 1070–1078
36 Bastidas-Rodriguez, J.D., Franco, E., Petrone, G., Andrés Ramos-Paja, C., Spagnuolo, G.: 'Maximum power point tracking architectures for photovoltaic systems in mismatching conditions: a review', *IET Power Electron.*, 2014, **7**, (6), pp. 1396–1413
37 Femia, N., Fortunato, M., Lisi, G., Petrone, G., Spagnuolo, G., Vitelli, M.: 'Guidelines for the optimization of the P&O technique in grid-connected double-stage photovoltaic systems'. Proc. IEEE Int. Symp. on Industrial Electronics, 2007, pp. 2420–2425
38 Femia, N., Petrone, G., Spagnuolo, G., Vitelli, M.: 'Optimizing duty-cycle perturbation of P&O MPPT technique'. Proc. IEEE 35th Power Electronics Specialists Conf., 2004, vol. 3, pp. 1939–1944
39 Femia, N., Petrone, G., Spagnuolo, G., Vitelli, M.: 'Optimizing sampling rate of P&O MPPT technique'. Proc. IEEE 35th Annual Power Electronics Specialists Conf., 2004, vol. 3, pp. 1945–1949
40 Femia, N., Petrone, G., Spagnuolo, G., Vitelli, M.: 'Optimization of perturb and observe maximum power point tracking method', *IEEE Trans. Power Electron.*, 2005, **20**, (4), pp. 963–973