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Three-state switching cell (3SSC)-based non-isolated dc–dc boost-type converter with balanced output voltage and wide voltage conversion range

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Abstract: This work presents a non-isolated step-up dc–dc converter with wide voltage conversion range based on the three-state switching cell, which is suitable for distinct applications, e.g. renewable energy and uninterruptible power supply (UPS) systems. Prominent advantages can be addressed to the topology, i.e. continuous input current, thus making it a proper choice for the use of battery banks as the input voltage source; the ability to operate at high power, high-current levels while maintaining current sharing through the main switches without the need of special control schemes; reduction of size, weight, and volume of filter elements, which are designed for twice the switching frequency; the maximum voltage across the controlled switches is half of the total output voltage; naturally balanced voltages across the dc-link capacitors exist; and the voltages across the switches are naturally clamped to that across the output filter capacitor, avoiding the need for external snubbers. The complete qualitative analysis of the converter is presented, including the operating principle and a step-by-step design procedure. A transformerless online UPS topology is also briefly described as a potential application for the introduced converter. Finally, experimental waveforms obtained from a 1.55-kW prototype are shown and relevant issues are discussed.

1 Introduction

Energy storage systems have been intensively used to supply critical loads, e.g. medical systems, emergency systems, computers, network servers, communication systems, industrial processes, and many others [1]. Besides, they play an important role in distributed generation, where energy is supposed to be stored during grid-connected operation so that it can be used later to supply distinct loads during power outages [2], being also employed to supply additional power during standalone mode operation if necessary [3].

Some energy storage systems e.g. UPSs typically depend strongly on battery banks, dc–dc converters, and dc–ac converters for their proper operation. Considering that the standard voltages across batteries are low, it is often necessary to use many series-connected units to supply the existing voltage source inverter (VSI), which provides ac rms voltages rated at 127 or 220 V, for instance. To reduce the required number of batteries for this purpose, step-up converters are used, which can be classified as either isolated or non-isolated topology. Even though the use of high-frequency transformers is common in practical switched-mode power supplies due to the minimisation of size, weight, and volume associated with high-switching frequencies since the 1970s [4], this may not still be an attractive choice in some modern applications e.g. light-emitting diode drivers, where it is often desired to minimise equipment overall dimensions. Within this context, non-isolated converters with wide conversion ranges have been a modern topic in power electronics considering the existence of numerous approaches and topologies where isolation is not a must.

Perhaps one of the first works on this topic was the one proposed in [5], where a wide voltage conversion range can be achieved by cascading several dc–dc converters, resulting in the so-called quadratic converters with high-voltage step-up and/or step-down. However, this is not a feasible choice when dealing with high-power levels and high-output voltages, considering the fact that high-component count associated with poor efficiency and appreciable voltage stresses regarding the semiconductors exist.

Coupled-inductor-based converters also allow obtaining high-voltage step-up in a simple and straightforward approach by simply adjusting the turns ratio involving the various windings, although they are often restricted to low-power levels and associated with significant drawbacks, e.g. voltage ringing and reduced efficiency due to the leakage inductance of the transformer [6–8].

Interleaving is a classical solution in the literature for high-power, high-current applications, with consequent improvement of performance and reduction of size, weight, and volume of magnetics [9], as some topologies regarding the achievement of high voltage gain have also been introduced. For instance, the converter proposed in [10] employs voltage multiplier cells (VMCs) that allow extending the static gain of the traditional interleaved boost topology in a modular approach. The converter is able to operate at high power levels with reduced current ripple, although high component count is necessary in order to obtain wide conversion ranges. Besides, current sharing among the existing phases is also of major concern, which can be affected by eventual intrinsic differences regarding the semiconductor elements and inductors and also the duty cycle mismatch as reported in [11]. To solve such inconvenient issues, the use of complex control schemes may be necessary to keep current balance among the semiconductors [12].

The three-state switching cell (3SSC) was introduced in [13], which was composed of two active switches, two diodes, and one autotransformer. Numerous converter topologies basically presented by the same group of authors using this concept have been proposed since then due to its prominent characteristics, e.g. reduced dimensions of filter elements, which are designed for twice the switching frequency similarly to the two-phase interleaved converter; the current stress involving semiconductors is reduced, as higher power levels can be achieved; overall losses are properly distributed among the semiconductors, resulting in better heat distribution and consequently more efficient use of heat sinks; part of the input power is directly transferred to the load

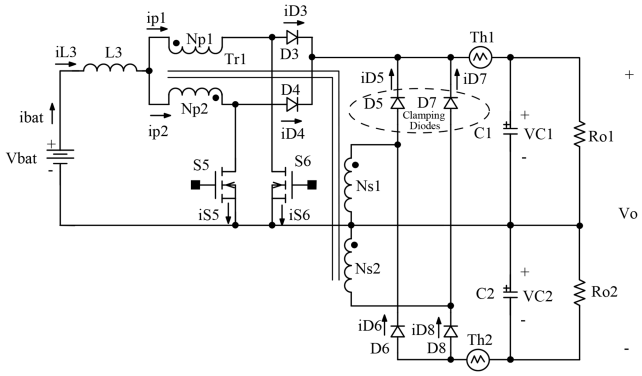

Fig. 1 *Proposed high-voltage step-up dc–dc converter with symmetrical output voltages*

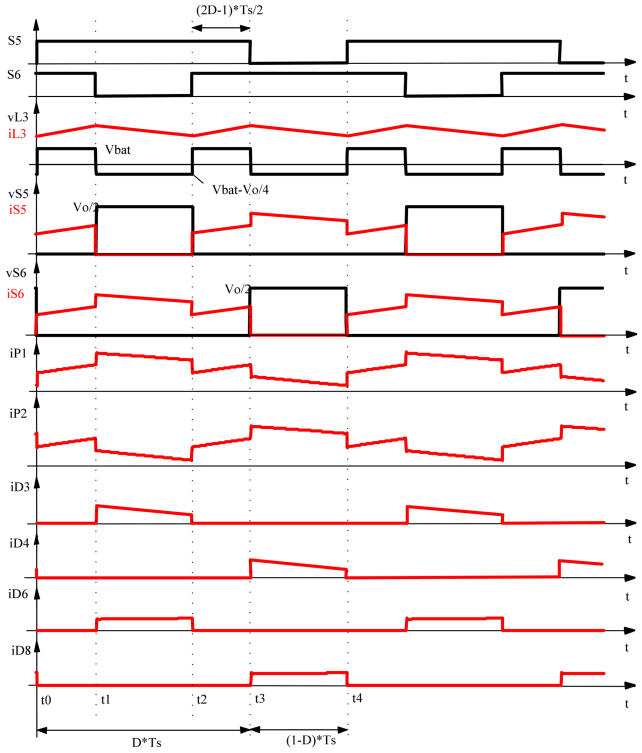

Fig. 2 *Main theoretical waveforms*

through the diodes and coupled inductors (i.e. autotransformer), and not through the main switches. The 3SSC is often misled by the interleaving technique, although current sharing is naturally maintained by the autotransformer considering that it is adequately implemented, without the need for special control schemes.

The 3SSC has been successfully used in the generation of several non-isolated dc–dc converters with high voltage gain characteristic. The topology in [14] corresponds to a boost converter using the 3SSC and one secondary winding, where the advantages associated with the 3SSC are obtained [13]. Besides, for a given duty cycle, the static gain can be modified by properly adjusting the turns ratio without increasing the voltage stress for the active switches, which are less than half of the output voltage. In this structure, part of the input power is directly transferred to the load without being processed by the active switches, thus implying reduced conduction losses. Unfortunately, this converter does not work properly when the duty cycle is <0.5 due to magnetic induction issues.

Within this context, this study proposes a step-up dc–dc converter based on the 3SSC, which comprises a capacitor divider as shown in Fig. 1 and is adequate to supply neutral-point-clamped, half-bridge, and dual half-bridge inverters. The main advantages of the introduced topology are non-pulsating input current with low ripples, thus increasing the very lifetime of the battery bank; the input filter inductor is designed for twice the switching frequency, thus allowing reduction of the converter dimensions; the voltage stress across the switches is half of the total output voltage and naturally clamped to that across the output filter capacitor; natural voltage balance is achieved in the split dc-link due to the autotransformer of the 3SSC. Firstly, the detailed analysis of the converter is presented, while a design procedure of the power stage elements is also discussed. Then a possible practical application for the converter in the conception of an online transformerless online uninterruptible power supply (UPS) is proposed. Finally, a 1.55-kW laboratory prototype is evaluated, while relevant waveforms are presented.

2 Proposed high step-up dc–dc converter

The 3SSC-based dc–dc boost converter is represented in Fig. 1, which is supposed to be analysed in this session considering the steady-state operation. The topology is composed of the following components: one input voltage source V_{bat} representing a battery bank; one storage inductor L_3; one autotransformer T_{r1} whose transformer turns ratio is $a = N_{s1}/N_{p1} = N_{s2}/N_{p2}$, where N_{p1} and N_{p2} are the number of the turns of the primary windings and N_{s1} and N_{s2} are the number of the turns of the secondary windings; two output filter capacitors C_1 and C_2; two active switches S_5 and S_6; six rectifier diodes D_3, D_4, D_5, D_6, D_7, and D_8; and the load resistors R_{o1} and R_{o2}.

2.1 Qualitative analysis

To analyse the converter, the following assumptions are considered: operation in continuous conduction mode (CCM); pulse width modulation with a fixed frequency is used to drive the main switches; and the duty cycle is higher than 0.5, thus characterising the operation in overlapping mode, which is a behaviour associated with the 3SSC [13]. Besides, semiconductors and magnetics are ideal. To balance the voltages across filter capacitors C_1 and C_2, the turns ratio involving the primary and secondary windings is the same, i.e. $a = N_{s1}/N_{p1} = N_{s2}/N_{p2}$. It is also worth to mention that parameter a can be properly chosen in order to adjust the static gain as desired and achieve wide conversion ratio. During the converter soft-start, the control circuit provides the duty cycle transition from zero up to the rated value without transient problems.

The main waveforms that describe the converter operation are shown in Fig. 2, which are essential to understanding the circuit behaviour during each stage and also derive the quantitative analysis that allows designing the power stage elements properly. Considering one switching period, four operating stages result as shown in Fig. 3. It is worthy to mention that diodes D_5 and D_7 allow natural voltage balance across output capacitors C_1 and C_2 since the numbers of turns of the secondary windings are the same.

The following parameters are also defined in Fig. 2:

$v_{L3}(t)$, $i_{L3}(t)$ – voltage and current waveforms in inductor L_3, respectively;
$v_{S5}(t)$, $v_{S6}(t)$, $i_{S5}(t)$, $i_{S6}(t)$ – voltage and current waveforms in switches S_5 and S_6;
$i_{P1}(t)$, $i_{P2}(t)$ – currents through windings N_{p1} and N_{p2}, respectively;
$i_{D3}(t)$, $i_{D4}(t)$, $i_{D6}(t)$, i_{D8v} – currents through diodes D_3, D_4, D_6, and D_8;
D – duty cycle;
V_o – total output voltage;
T_s – switching period.

First stage [t_0, t_1] (Fig. 3*a*): switches S_5 and S_6 are turned on. Energy is only stored in inductor L_3 and not transferred to the load. All the rectifier diodes are reverse biased in this interval.

Second stage [t_1, t_2] (Fig. 3*b*): only switch S_5 remains turned on. The voltage across switch S_6 is equal to that across capacitor C_1. Diodes D_3 and D_6 are forward biased. The inductor and the

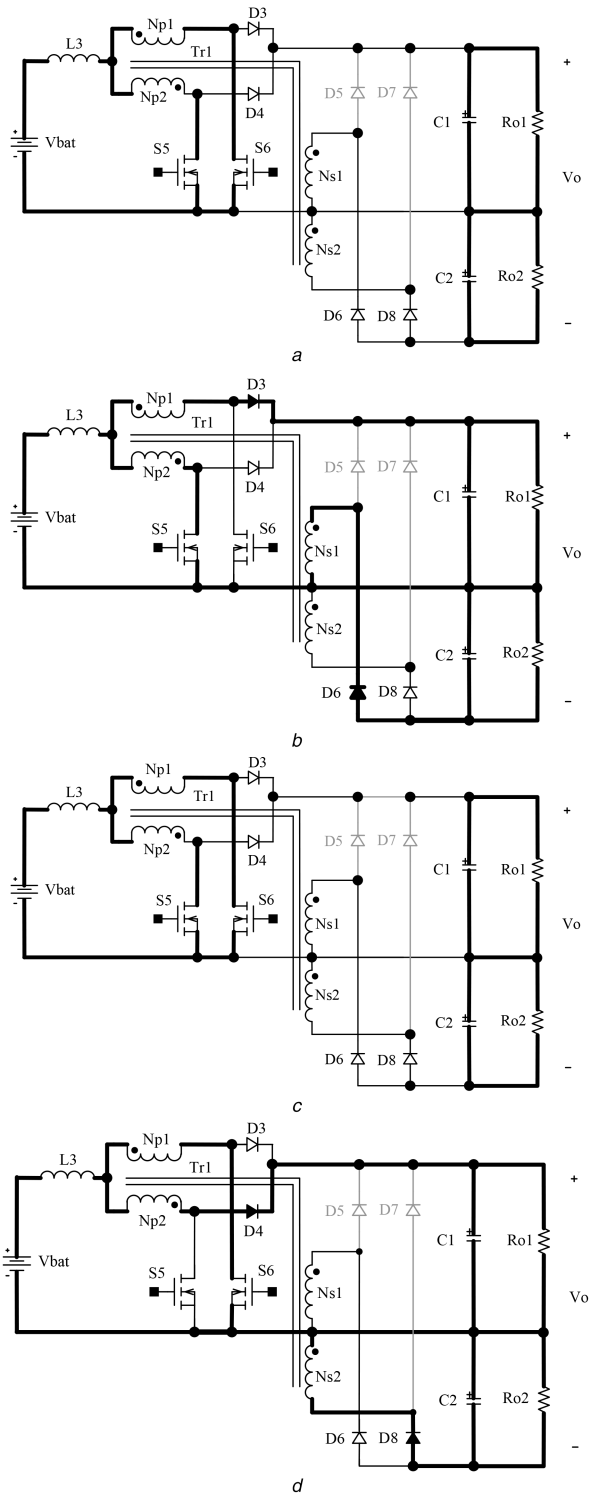

Fig. 3 *Operating stages of the proposed dc–dc converter*
(a) First stage, ***(b)*** Second stage, ***(c)*** Third stage, ***(d)*** Fourth stage

input voltage source transfer energy to filter capacitors C_1 and C_2 and also the loads R_{o1} and R_{o2}.

Third stage [t_2, t_3] (Fig. 3*c*): this stage is similar to the first one, where switches S_5 and S_6 are turned on and energy is stored only in L_3.

Fourth stage [t_3, t_4] (Fig. 3*d*): only switch S_6 remains turned on. The voltage across switch S_5 is equal to the voltage across the capacitor C_2. Diodes D_4 and D_8 are forward biased. The inductor and the input voltage source transfer energy to filter capacitors C_1 and C_2 and also the loads R_{o1} and R_{o2}.

Table 1 Specifications of the dc–dc converter

input voltage range	V_{bat} = 63–81 V
rated input voltage	$V_{bat(nom)}$ = 72 V
output power	P_o = 1.55 kW
output voltage	V_o = 400 V
switching frequency	f_s = 40 kHz
ripple current through the inductor	$\Delta I_{L3} = 0.3 I_{bat(max)}$
transformer turns ratio	a=2
rated duty cycle at the maximum battery voltage	D_{max}=0.685
ripple voltage across the output capacitors	$\Delta V_{C1} = 0.05 V_o$
theoretical efficiency	η = 0.95

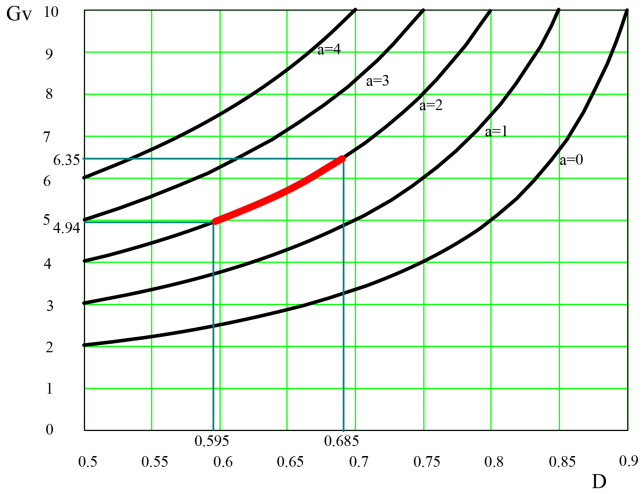

Fig. 4 *Static gain as a function of the duty cycle for distinct transformer turns ratios*

2.2 Quantitative analysis and design example

Considering the operation in CCM and $D > 0.5$, the quantitative analysis of the proposed converter can be developed assuming that symmetrical voltages exist across the output capacitors C_1 and C_2, which occur when the transformer turns ratio between the primary and secondary windings is $N_{s1}/N_{p1} = N_{s2}/N_{p2}$. For this purpose, it is necessary to analyse the main theoretical waveforms and operating stages represented in Figs. 2 and 3, respectively.

Besides, let us consider a design example according to the specifications in Table 1, which are also used in the implementation of an experimental prototype.

2.2.1 Static gain: The static gain G_V can be obtained applying the volt-second balance to the filter inductor, also considering the waveform corresponding to $v_{L3}(t)$. Then expression (1) results, while the curves in Fig. 4 can be plotted and the rated duty cycle varies according to the voltage across the battery bank. Of course, the number of series-connected batteries can be reduced if parameter a is increased as desired. To achieve balanced voltages across output capacitors C_1 and C_2, parameter $a = N_{s1}/N_{p1} = N_{s2}/N_{p2} = 2$ is adopted in this case

$$G_V = \frac{V_o}{V_{bat}} = \frac{1}{(1-D)}\left(1 + \frac{a}{2}\right). \quad (1)$$

2.2.2 Filter inductor L_3: Analysing $i_{L3}(t)$, it is possible to determine the input filter inductance as

$$L_3 = \frac{V_{bat(min)}(2D_{max} - 1)}{2 f_s \Delta I_{L3}} = 37.50\,\mu\text{H}. \quad (2)$$

where $V_{bat(min)}$ is the minimum voltage across the battery and ΔI_{L3} is the current ripple through L_3.

2.2.3 High-frequency transformer: Considering symmetrical output voltages across the capacitors, the high-frequency transformer must be designed according to the processed active power P_p and the recommendations given in [13], i.e.

$$P_p = \frac{3}{4}P_o = 1162.5\,\text{W}. \tag{3}$$

By integrating the waveforms of the currents through the primary and secondary windings over one switching period, it is possible to determine their respective rms values as in (4) and (5).

$$I_{P1(rms)} = I_{P2(rms)} = \frac{I_{bat(max)}}{4}\sqrt{2(3 - D_{max})} = 13.93\,\text{A}, \tag{4}$$

$$I_{S1(rms)} = I_{S2(rms)} = \frac{I_{bat(max)}}{4}\sqrt{(1 - D_{max})} = 3.63\,\text{A}, \tag{5}$$

where $I_{bat(max)}$ is the maximum current through the battery, which occurs when the input voltage is minimum, i.e. $V_{bat} = 63$ V, given by

$$I_{bat(max)} = \frac{P_o}{V_{bat(min)}\eta} = 25.9\,\text{A}. \tag{6}$$

The peak voltage across each primary winding of the transformer is

$$V_{P1(pk)} = V_{P2(pk)} = \frac{V_o}{4} = 100\,\text{V}. \tag{7}$$

2.2.4 Output filter capacitors: Considering that the voltage ripple is small, the average voltages across capacitors C_1 and C_2 are given by the following equation:

$$V_{C1} = V_{C2} = \frac{V_o}{2} = 200\,\text{V}. \tag{8}$$

If the proposed converter is used to supply a half-bridge inverter, the output filter capacitances can be calculated using the following equation:

$$C_1 = C_2 = \frac{P_o}{f_r \cdot \Delta V_{C1} \cdot V_o} = 3229.17\,\mu\text{F}, \tag{9}$$

where $f_r = 60$ Hz is the ac grid frequency. Finally, it can be stated that the rms of the currents through the capacitors can be determined from the output current through the inverter.

2.2.5 Active switches S_5 and S_6: The maximum voltages across switches S_5 and S_6 without considering eventual overshoot due to the leakage inductances of the transformer can be determined from the analysis of the operating stages shown in Fig. 3 as

$$V_{S5(max)} = V_{S6(max)} = \frac{V_o}{2} = 200\,\text{V}. \tag{10}$$

The rms and average currents through the switches are obtained by integrating their respective theoretical waveforms over the switching period as in (11) and (12), respectively

$$I_{S5(rms)} = I_{S6(rms)} = \frac{I_{bat(max)}}{4}\sqrt{(5 - D_{max})} = 13.43\,\text{A}, \tag{11}$$

$$I_{S5(avg)} = I_{S6(avg)} = \frac{I_{bat(max)}}{4}(1 + D_{max}) = 10.91\,\text{A}. \tag{12}$$

2.2.6 Rectifier diodes D_3–D_8: The maximum reverse voltages across diodes D_3–D_4 and D_5–D_8 can be determined from the analysis of the operating stages shown in Fig. 3 as (13) and (14), respectively

$$V_{D3,\ldots,D4(max)} = \frac{V_o}{2} = 200\,\text{V}, \tag{13}$$

$$V_{D5,\ldots,D8(max)} = V_o = 400\,\text{V}. \tag{14}$$

The rms and average currents through the aforementioned diodes are determined by integrating their respective theoretical waveforms over the switching period as in the following equations:

$$I_{D3,\ldots,D8(rms)} = \frac{I_{bat(max)}}{4}\sqrt{(1 - D_{max})} = 3.63\,\text{A}, \tag{15}$$

$$I_{D3,\ldots,D8(avg)} = \frac{I_{bat(max)}}{4}(1 - D_{max}) = 2.04\,\text{A}. \tag{16}$$

Considering symmetrical voltages across capacitors C_1 and C_2, it can be stated that the rms and average currents through diodes D_5 and D_7 are zero. It is worthy to mention that such diodes are used to avoid voltage unbalance across capacitors C_1 and C_2. For design purposes, semiconductors with similar characteristics are adopted for D_3, D_4, D_6, and D_8.

2.3 Potential application of the proposed dc–dc converter in the conception of a transformerless online UPS

UPSs are classified as offline, line interactive, and online according to standard IEC 62040-3 [15], as there are three possible options to supply loads when the ac grid voltage is not within the recommended limits. However, the online UPS is the configuration that presents the best performance when power grid disturbances occur due to the high-size filter capacitors required for the existing dc link. Therefore, it can be considered as an excellent power conditioner for critical loads, e.g. computers, printers, medical equipment, data storage systems, air traffic control systems, among others [16–18].

As it was previously mentioned, low dc voltages which are typically available from batteries, fuel cells, and photovoltaic modules must be stepped up in distinct applications in order to supply a VSI [19]. After a proper literature review on transformerless online UPSs with a common neutral point, two types of architectures could be found. The first one employs a single filter capacitor in the dc link as in [20], while the second one requires two series-connected filter capacitors instead as in [21–24]. Another important issue to be observed in transformerless online UPS topologies lies in the interconnection of batteries to the dc link, as the use of many series-connected batteries may not be feasible for rated power levels higher than 5 kW due to the significant cost of such components as stated in [25]. On the other hand, for lower output power ratings, few batteries should be used instead, although the voltage levels across the battery bank and the dc link are not compatible. To overcome such a drawback, step-up dc-dc converters are typically used, where a wide conversion ratio is a must [21–25].

According to [26], duty cycles up to about 0.7 should be used to reach conversion ratios up to 3.3, which can be reached with the classical non-isolated dc–dc boost converter. However, for higher duty cycles, significant drawbacks tend to exist, such as appreciable conduction losses due to the on-resistance of power metal oxide semiconductor field effect transistors (MOSFETs) and especially copper losses in the filter inductor. To step up the voltage across the battery bank, there are some interesting options regarding non-isolated dc–dc converters with high power processing capability as mentioned in [27, 28] specifically for transformerless online UPSs. It is possible to use dc–dc boost converters either with limited static gain or high voltage step-up, being the latter approach better recommended for the single filter capacitor configuration as in [21–23]. Non-isolated dc–dc

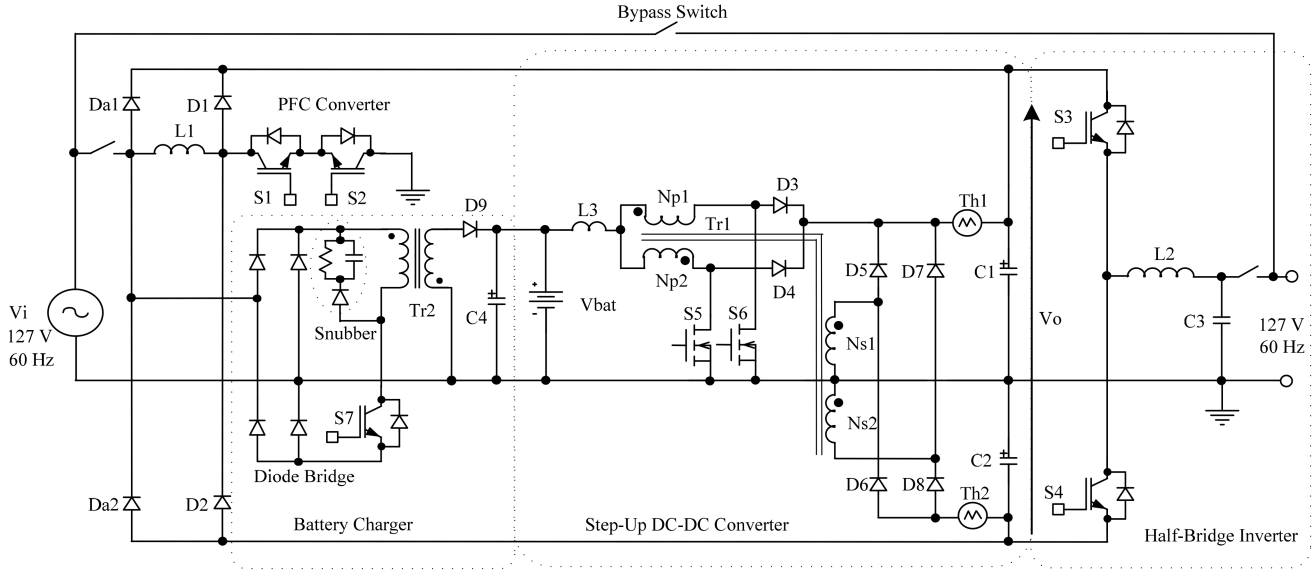

Fig. 5 *Proposed transformerless online UPS system*

Table 2 Comparison among non-isolated boost-type dc–dc converters for high voltage step-up and high–power applications

Characteristic	Topologies				
	[32]	[10][a]	[33][a]	[34][b]	Proposed topology
static gain	$\frac{4}{1-D}$	$\frac{\text{VMC}+1}{1-D}$	$\frac{\text{VMC}+1}{1-D}$	$\frac{1}{1-D}\left(1+\sum_{j=1}^{n} a_j\right)$	$\frac{1}{(1-D)}\left(1+\frac{a}{2}\right)$
voltage stress across the main switches	$\frac{V_o}{4}$	$\frac{V_o}{\text{VMC}+1}$	$\frac{V_o}{2\text{VMC}^{0.3}}$	$\frac{V_o}{\left(1+\sum_{j=1}^{n} a_j\right)}$	$\frac{V_o}{2}$
switches	2	2	2	2	2
diodes	4	2VMC + 2	2VMC + 2	2*a* + 2	6
autotransformers	—	—	1	1	1
capacitors	4	2VMC + 1	2VMC + 1	2*a* + 1	2
inductors	2	2	1	1	1

[a]VMC – number of voltage multiplier cells.

[b]a_j – turns ratio of a given secondary winding j.

converters with high voltage step-up and symmetrical output voltages can also be used as in [29].

A possible configuration for a transformerless online UPS is shown in Fig. 5, which is essentially based on the 3SSC-based dc–dc converter represented in Fig. 1. It can be seen that a half-bridge VSI is employed, which is supplied by the capacitive divider of the dc–dc converter. A satisfactory voltage balance across capacitors C_1 and C_2 is maintained due to the autotransformer associated with the 3SSC. As a possible drawback for the proposed topology, there is the direct current path between the battery bank and the dc link capacitors, while the inrush current during its connection may be appreciable. However, this issue can be avoided by using a negative temperature coefficient thermistor or other type of limiter device as shown in Fig. 5. This work is essentially focused on the thorough analysis of the non-isolated dc–dc converter, while the detailed study of the UPS is not part of the scope.

2.4 Comparison with other non-isolated dc–dc converter topologies with high voltage step-up

Non-isolated dc–dc converters with high voltage step-up is a modern topic in power electronics, as numerous topologies have been proposed so far as an alternative to the use of high-frequency transformers, aiming at reducing cost and overall dimensions while improving efficiency. However, many topologies available in the literature are only feasible to low-power levels rated at a few hundred watts [30].

When dealing with high-power, high-current applications, interleaved converters are often highlighted as a prominent choice, even though slight constructive differences among the components of the system phases and duty cycle mismatch may eventually lead to current unbalance, thus requiring the use of specific control techniques [31]. On the other hand, converters based on the 3SSC typically do not present such a limitation considering that the autotransformer is properly designed and implemented in practice in order to achieve unity turns ratio, i.e. the windings have nearly the same impedance, thus ensuring proper current sharing [13].

To establish a fair comparison among the proposed converter and some topologies previously presented in the literature, let us consider Table 2. The work developed in [32] comprises a quadrupler interleaved boost converter with an extended static gain, where the voltage across the main switches is one-fourth of the output voltage, but voltage balance involving the capacitor divider is of major concern. VMCs associated with the interleaved boost converter are also an option to achieve high-voltage step-up as in [10] resulting in a modular approach but at the cost of the high-component count, which may compromise efficiency. A family of converters employing the 3SSC and VMCs is introduced in [33], where trade-offs between the number of components and wide conversion ratio must be made so that efficiency is not drastically affected. Similarly, the topology in [34] relies on multiple secondary windings coupled to the autotransformer of the 3SSC to provide a wide conversion ratio.

It can be easily noticed that the converter shown in Fig. 1 does not present the widest conversion ratio among the aforementioned structures, especially considering the modular approaches described in [10, 33, 34]. However, it consists of a proper choice to supply dc–ac converters that employ split dc-links, e.g. half-bridge inverters, with a good voltage balance regarding the capacitor divider, which is due to the autotransformer of the 3SSC. Besides, a reduced component count is achieved in the proposed topology when compared with the use of VMCs in both 3SSC-based and

Table 3 Components used in the power stage of the dc–dc converter

boost inductor	L_3 = 35 μH, core NT-60/21/20-260-IP12R by Thornton, N_{L3} = 5 turns, 37 × 26AWG, l_g = 5 mm
transformer	core NEE-55/28/21 by Thornton, $N_{p1} = N_{p2}$ = 14 turns, 24 × 26 AWG, $N_{s1} = N_{s2}$ = 28 turns, 6 × 26 AWG
output capacitors C_1, C_2	electrolytic capacitors, 3 × 1000 μF/250 V
rectifier diodes D_3–D_8	ultrafast diode HFA15PB60 by international rectifier
switches S_5–S_6	MOSFET IRFP4242PBF by international rectifier

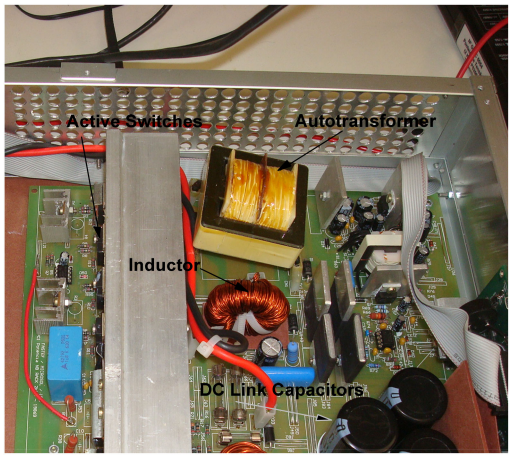

Fig. 6 *Picture of the experimental prototype*

interleaved converters, since the static gain depends on the duty cycle and the turns ratio a as shown in expression (1).

3 Experimental evaluation of the proposed dc–dc converter

To validate the theoretical assumptions, an experimental prototype of the dc–dc converter was assembled according to the specifications in Table 1, while the components listed in Table 3 were used in Fig. 6. Once again, it is worthy to mention that the UPS configuration shown in Fig. 5 is not supposed to be thoroughly analysed.

Experimental results were obtained for the dc–dc converter supplying a half-bridge VSI. Figs. 7*a* and *b* show that the average voltage across the battery bank is V_{bat} = 64.5 and 71.8 V, respectively. The frequency of the inductor current ripple is twice the switching frequency, which results in reduced dimensions of filter elements. Besides, in both cases, it can be seen that the current through the batteries, i.e. the inductor current is continuous with reduced ripples. This is an essential feature of battery-powered systems so that the lifetime of the battery bank is preserved.

Fig. 7*c* corresponds to the drain-to-source voltages across the main switches, whose maximum values are equal to about half of the total output voltage as stated in the theoretical analysis. Besides, Fig. 7*d* shows that the voltages across the output capacitors are nearly balanced and regulated even though asymmetrical loads are connected to the dc link due to the autotransformer that constitutes the 3SSC.

Finally, Fig. 8 represents the converter efficiency at $V_{i(bat)(nom)}$ = 72 V over a wide load range, which is about 94% at rated load condition.

4 Conclusions

This work has presented a study of a high-voltage gain non-isolated dc–dc converter suitable for online transformerless UPSs with a common neutral. The proposed converter can be properly

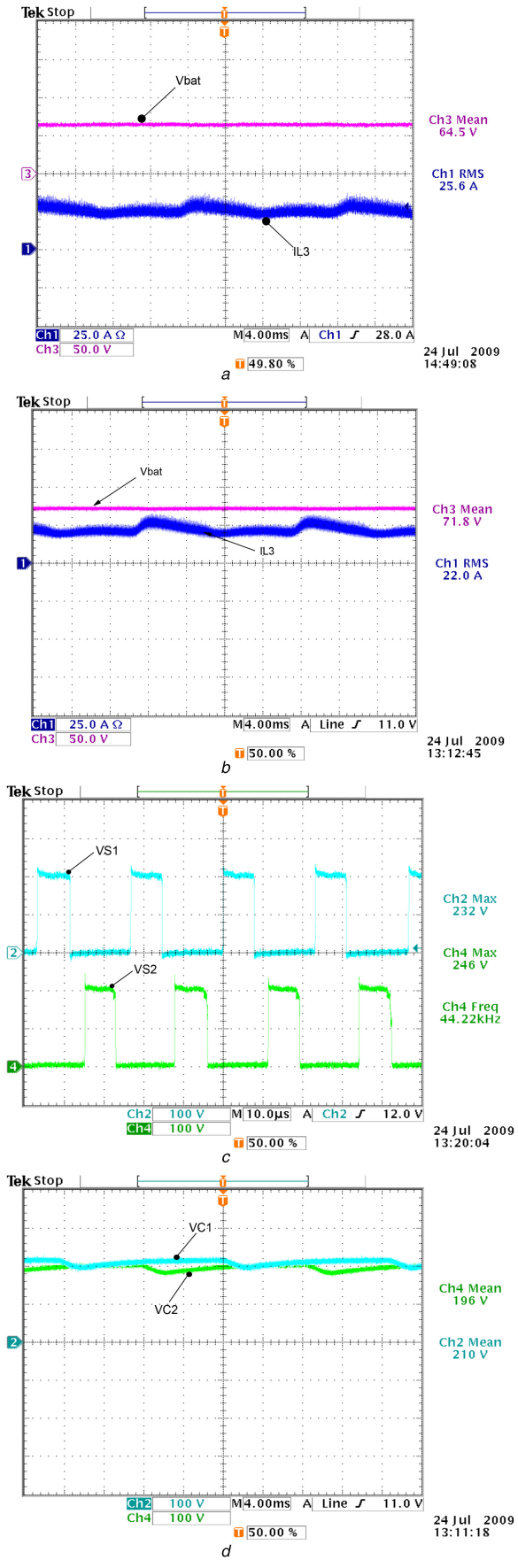

Fig. 7 *Experimental results*

(a) Battery voltage and current through inductor L_3 (50 V/div; 25 A/div; 4 ms/div), ***(b)*** Battery voltage and current through inductor L_3 (50 V/div; 25 A/div; 4 ms/div). ***(c)*** Drain-to-source voltages V_{S1} and V_{S2} (100 V/div; 100 V/div; 10 μs/div), ***(d)*** Voltages across output capacitors V_{C1} and V_{C2} (100 V/div; 100 V/div; 4 ms/div)

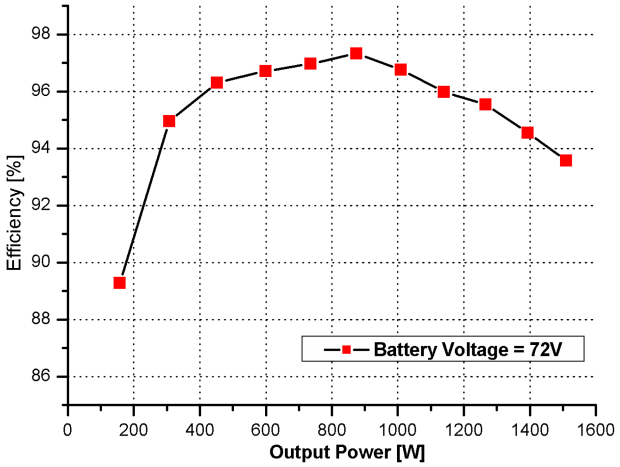

Fig. 8 *Efficiency as function of the output power*

used to step the battery voltage up to the dc link voltage where a VSI is connected without requiring many series-connected batteries. From the experimental waveforms, the following advantages can be addressed to the topology: non-pulsating input current, consequently reducing I^2R losses in the battery due to internal resistances; the maximum voltage across the active switches is half of the total dc-link voltage; the inductor current ripple frequency is twice the switching frequency, thus leading to reduced size, weight, and volume of filter elements; the transformer does not process the rated active power, which also contributes to the reduction of its very dimensions; the voltage across the output filter capacitors are symmetrical and naturally balanced; and the maximum reverse voltage across the rectifier diodes is equal to total output voltage. Besides, higher conversion ratios can be obtained by adjusting the turns ratio of the autotransformer. Efficiency at rated load condition is about 94%, even though performance can be further improved by using high-quality semiconductors. Finally, it is reasonable to state that the aforementioned converter can also be used in the development of standalone and grid-connected systems for microgrid applications.

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