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OLYMPIO CIPRIANO DA SILVA FILHO

A FAMILY OF HIGH-FREQUENCY ISOLATED SINGLE-PHASE AC-AC CONVERTERS

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A FAMILY OF HIGH-FREQUENCY ISOLATED SINGLE-PHASE AC-AC CONVERTERS

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Concentration Area: Electric Power Systems.

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To those who are not among us,

but continue to live in our hearts.

RESUMO

Propõe-se uma família de conversores CA-CA monofásicos isolados em alta frequência. Um conjunto de elementos ativos e passivos comuns é compartilhado por todas as topologias da família e tem como base o intercalamento de indutores e o conversor DAB (*Dual Active Bridge*). Isso permite elevada densidade de potência e capacidade de corrente, além de possibilitar a comutação suave em parte dos semicondutores. A família é composta por nove topologias sendo três simétricas e seis assimétricas. Todas as topologias são descritas, modeladas e simuladas. O desempenho dinâmico é verificado face a afundamento de tensão e degrau de carga. Análises matemáticas e simulações mostraram que diferenças entre as funções de chaveamento aplicadas às chaves, que definem as tensões no primário e secundário do transformador, elevam a corrente de circulação e por consequência, as perdas. Esse problema é minimizado em parte dos conversores da família que podem utilizar o esquema proposto de atuador parcial. Além disso, as correntes no transformador foram minimizadas em alguns conversores assimétricos através de duas novas modulações. Com objetivo de reduzir o volume total de magnéticos e as perdas, métodos de integração e modelagem de magnéticos foram estudados. Como resultado dois magnéticos integrados foram desenvolvidos e testados para a topologia em Ponte-completa Simétrica. Na Universidade de Kassel foi desenvolvida uma plataforma experimental com a qual obteve-se resultados para cinco topologias da família. Os resultados mostraram boa resposta dinâmica de todos os conversores avaliados. Além disso, a integração trouxe redução do volume total dos magnéticos e elevação da eficiência do converter testado.

Palavras-chave: Conversor CA-CA, monofásico, isolado em alta frequência, Conversor intercalado, DAB, compensador de tensão.

ABSTRACT

A family of single-phase AC-AC converters isolated at high frequency is proposed. A set of common active and passive elements is shared by all topologies of the family and is based on the interleaved inductors and the DAB (Dual Active Bridge) converter. This enables high power density and current capacity, as well as smooth switching in part of the semiconductors. The family consists of nine topologies being three symmetrical and six asymmetrical. All topologies are described, modeled and simulated. The dynamic performance is checked against voltage sag and load step. Mathematical analysis and simulations showed that differences between the switching functions applied to the switches, which define the primary and secondary voltages of the transformer, increase the circulation current and, consequently, the losses. This problem is minimized in part of the converters of the family that can use the proposed partial actuator scheme. In addition, the currents in the transformer were minimized in some asymmetrical converters through two new modulation schemes. In order to reduce the total magnetic volume and losses, methods for magnetic integration and modeling were studied. As a result, two integrated magnets were developed and tested for the Symmetric Full-bridge converter. At the University of Kassel, an experimental platform was developed with which results were obtained for five topologies. The results showed a good dynamic response of all evaluated converters. In addition, the integration brought a reduction in the total volume of the magnets and an increase in the efficiency of the tested converter.

Keywords: AC-AC converter, single-phase, isolated in high frequency, interleaved converter, DAB, voltage compensator.

KURZFASSUNG

Eine Familie von hochfrequenten isolierten einphasigen AC/AC-Wandlern wird vorgestellt. Eine Reihe von gemeinsamen aktiven und passiven Bauelementen wird von allen Topologien der Familie benutzt und basiert auf die verschachtelten Induktivitäten und den DAB (Dual Active Bridge) Konverter. Dies ermöglicht hohe Leistungsdicht und Strombelastbarkeit sowie ein sanftes Schalten in einem Teil der Halbleiter. Die Familie besteht aus neun Schaltungstopologien, von denen drei symmetrisch und sechs asymmetrisch sind. Alle Topologien werden beschrieben, modelliert und simuliert. Das dynamische Verhalten wird gegen Spannungseinbruch und Lastsprung geprüft. Mathematische Analysen und Simulationen zeigten, dass Unterschiede zwischen den auf die Schalter angewandten Schaltfunktionen, die die Primär- und Sekundärspannungen des Transformators definieren, den zirkulierenden Strom und infolgedessen die Verluste erhöhen. Dieses Problem wird in einem Teil der Umrichter der Familie minimiert, zu dem man das vorgeschlagene Teilaktuator-Schema verwenden kann. Darüber hinaus wurden die Ströme im Transformator bei einigen asymmetrischen Wandlern durch zwei neue Modulationsverfahren minimiert. Um das gesamte Volumen sowie die Verluste der magnetischen Bauelementen zu reduzieren, wurden Methoden zur Integration und Modellierung der Magnetics untersucht. Als Ergebnis wurden zwei integrierte Magnetics entwickelt und im symmetrischen Vollbrückenkonverter getestet. An der Universität Kassel wurde eine experimentelle Plattform entwickelt, mit der Ergebnisse von fünf Topologien erzielt wurden. Die Ergebnisse zeigten ein gutes dynamisches Verhalten aller bewerteten Topologien. Darüber hinaus brachte die Integration der Magnetics eine Reduzierung des Gesamtvolumens und eine Erhöhung des Wirkungsgrades des untersuchten Umrichters.

Schlüsselwörter: AC/AC-Wandler, einphasig, mittelfrequent isoliert, verschachtelter Wandler, DAB, Spannungskompensator.

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1 INTRODUCTION

The AC-AC conversion has many applications, e.g., voltage regulators, Dynamic Voltage Restorers, and Uninterruptible Power Supplies (UPS). These applications solve problems related to low power quality such as voltage sags, swells, harmonics, flicker, and short-term interruptions. Amongst the mentioned problems, voltage sag is one of the most relevant (GOSWAMI, A. K.; GUPTA; SINGH, 2008) and frequent (GOSWAMI, A. K.; GUPTA; SINGH, 2008). Such problems affect the proper functioning of sensitive loads like computers, robots, Programmable Logical Controllers (PLC), among others that may fail or misbehave causing the complete stop of the energy customer activity (CHAPMAN, 2001), which potentially lead to financial losses (GOSWAMI, A. K.; GUPTA; SINGH, 2008).

There are a great number of ac-ac topologies available in the literature, which can be classified as either direct (ac-ac) or indirect (ac-dc-ac). The indirect group can be divided between the converters with and without a constant DC-link. Conventional converters, like the buck, boost, and buck-boost have their ac-ac versions available as direct converters (FANG ZHENG PENG; LIHUA CHEN; FAN ZHANG, 2003) (FEDYCZAK; STRZELECKI; BENYSEK, 2002). Isolated versions of other basic converters like Forward and Flyback are also available, as presented in (LEI LI *et al.*, 2006). In (AHMED *et al.*, 2016a) the Z-source converter topology is employed to perform direct ac-ac conversion with high-frequency isolation. In addition, (QIN; KIMBALL, 2013) presents the ac-ac version of the Dual Active Bridge (DAB) converter. One of the main drawbacks of these converters is the use of bi-directional switches, which increase costs and losses (BONG-HWAN KWON *et al.*, 2002).

Indirect converters can perform the ac-dc-ac conversion using a constant DC-link. An example is the three-phase voltage back-to-back converter (KOLAR *et al.*, 2011). The advantage of the indirect conversion over the direct conversion is the decoupling between the conversion stages (ac-dc-ac), which allows the independent control of rectifier and inverter currents and reactive compensation.

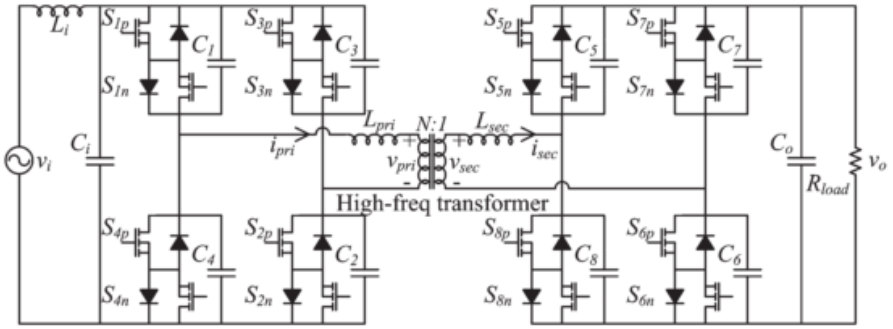
In addition to the isolated versions of the basic converters, the isolation can also be provided by dc-dc high-frequency isolated converters, e.g., the Dual Active Bridge (DAB) (DE DONCKER; DIVAN; KHERALUWALA, 1988), Series Resonant Converter (SCR) (ZHENG; CZARKOWSKI, 2007), etc. The DAB allows high power and high efficiency for high power density applications (KRISMER; KOLAR, 2012)(INOUE; AKAGI, 2007).

1.1 Literature review

A revision of direct converters based on basic converters like the buck, boost, and buck-boost, with and without isolation, is presented in (FEDYCZAK; STRZELECKI; BENYSEK, 2002) and (FANG ZHENG PENG; LIHUA CHEN; FAN ZHANG, 2003). Alternate current versions of the Forward and Flyback converters are presented in (LEI LI *et al.*, 2006) and (LEI LI; DAOLIAN CHEN, 2003). In order to handle alternated current, these topologies employ bi-directional switches, which increase the losses and the costs.

One bidirectional converter using the principle of the DAB converter is presented by (QIN; KIMBALL, 2013). The converter, presented in Figure 1, uses sixteen switches and phase-shift modulation to control the power flow between both sides of the transformer. In order to do this, an inductance is placed in series with the transformer leakage inductance that limits the current rate and the maximal transferred power. A high frequency three level voltage is applied to both sides of the transformer, but its amplitude follows the grid voltage amplitude. The converter operates with ZVS (*Zero Voltage Switching*), but its range variates with the load power factor. For resistive loads, the converter presents ZVS during the whole grid cycle, while with the load power factor of 0.95 the ZVS range decreases to 60º of the grid cycle.

Figure 1 – AC-AC DAB converter.



Source: (QIN; KIMBALL, 2013)

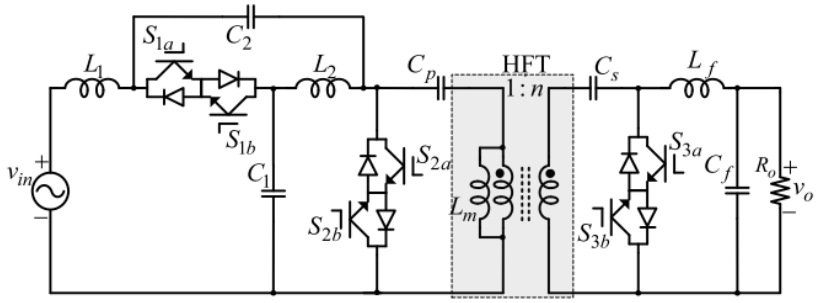
A high frequency isolated converter is presented by (ZHU LING; LI LEI, 2010) and it uses two cascaded isolated Cùk converters to reduce the switch voltage stress. Eight switches are employed and two high-frequency transformers are needed. One advantage of this converter is the generated three-level output voltage that reduces the filter requirements. However, this converter requires a more complex control system.

One input series output parallel converter structure is presented by (LI; HU, 2011). This converter splits the input voltage stress and output current stress and it is able to produce a three-level output voltage as well. The converter presents bidirectional power flow but employs two transformers, which increases the volume of the magnetic devices.

The isolated direct converter presented by (ZHU; LI, 2012). The switches arrangement connected to the primary side of the transformer uses sixteen switches generating a five-level converter input voltage. The arrangement connected to the transformer secondary side is composed of two bidirectional switches and generates a three level voltage, which is imposed on an LC filter. The major drawback of this converter is the high number of switches.

One family of Z-source converters is proposed by (AHMED *et al.*, 2016a). The converters are isolated in high frequency and present buck-boost characteristic with soft switching. One topology of the proposed family is presented in Figure 2. In addition to the bidirectional switches, the experimental results presented high input current THD (Total Harmonic Distortion).

Figure 2 –*Z-source* with high-frequency isolation.

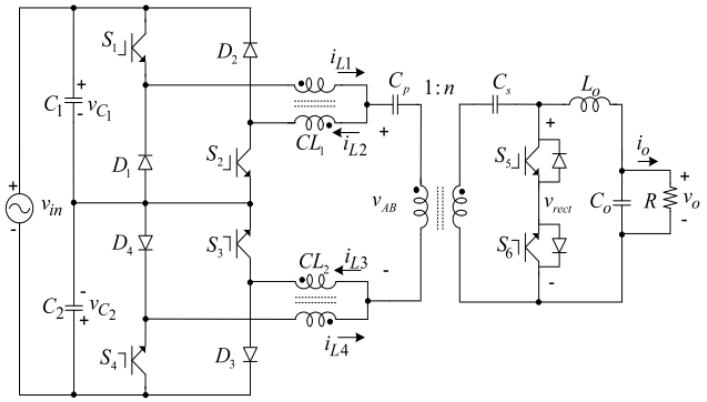


Source: (AHMED *et al.*, 2016a)

The converter presented by (AHMED *et al.*, 2016b) (Figure 3) uses two interleaved transformers to perform interleaving obtaining two times the switching frequency in the passive elements. Another advantage is the division of the voltage stress in the grid side due to the semiconductor arrangement. However, due to the transformer leakage inductance, the switches in the load side present voltage spikes, which become significant in high power applications requiring the use of snubber circuits.

In addition to the direct converters shown so far, it is also possible to use indirect converters with constant DC bus to perform the *ac-ac* conversion. These converters have two stages as opposed to the single stage assigned to the direct converters. The two stages *are* the *ac-dc* rectifier stage and the *dc-ac* inverter stage. When the conversion requires isolation, it can

Figure 3 – High-frequency isolated transformer using an interphase transformer.

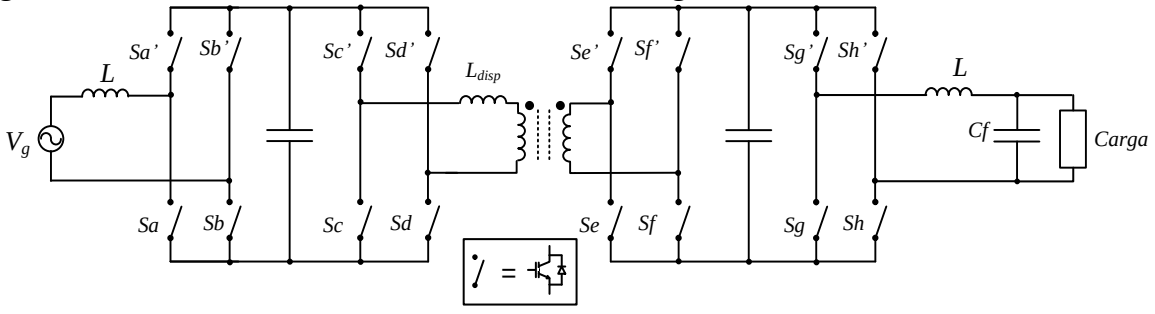


Source: (AHMED *et al.*, 2016b)

be done using a high-frequency transformer and a *dc-dc* converter such as DAB (DE DONCKER; DIVAN; KHERALU*WALA, 1988)* as shown in Figure 4. In this case, the conversion presents three stages: rectification, inversion and the *dc-dc* stage. This topology has already been widely used in several studies applied in solid-state transformers such as (INOUE; AKAGI, 2007), (HUANG et al., 2010) and (KINGDOM, 2007).

The advantages of indirect conversion over direct conversion are presented in e.g., (KOLAR et al., 2011), (FRIEDLI et al., 2012). Among the advantages, one can mention the decoupling of the stages in relation to the control due to the use of the DC bus. This allows, e.g., the currents in the rectifier and inverter to be controlled independently, which is not possible with a direct converter. Another characteristic that differs between these types of converters is the compensation of reactive that, in the converter of the indirect type depends on the dimensioning of the elements, while in the direct converters depend on a series of restrictions pointed out in (FRIEDLI et al., 2012). Better performance can also be cited when nonlinear loads are fed.

Figure 4 – Ac-ac converter with constant DC-link using DAB.



Source: Adapted from (HUANG *et al.*, 2011)

1.2 Goals and expected contributions

From the above, there are contributions to be made in the study of topologies based on indirect converters with constant DC-link, which bring high current capacity and use isolation at high frequency.

Thus, this thesis proposes a family of single-phase ac-dc-ac converters based on the DAB converter and interleaving transformer. The converters should be able to mitigate short and long duration voltages sags, keeping control of the input power factor, control of both DC-links and a sinusoidal output voltage.

Among the other contributions expected from the proposed study, there are:

- Modeling of the proposed converters;
- Analysis of the commutation to identify the regions with soft switching;
- Reduce the number of magnetic devices used by the converter of the family through magnetic device integration.
- Acquisition of experimental results for the proposed converters.

The combination of interleaving transformer and semiconductor legs give rise to nine different topologies, which are modeled, simulated and tested. Three of the proposed topologies are symmetric from the transformer point of view, while the other six are asymmetric.

The next chapters are organized as follows:

- Chapter 2 presents the proposed converter family showing all the topologies and performing a rough comparison between them.
- Chapter 3 presents the Symmetric Half-bridge topology, its operation, and model. The design of the passive elements involved is also presented as well as the experimental platform used to obtain the experimental results.
- Chapter 4 analyses the Symmetric Full-bridge topology, its low-frequency modulation, and the transformer power flow.
- Chapter 5 analyses the Symmetric Interleaved Full-bridge converter and presents the actuator types concept.
- Chapter 6 analyses the one pair of asymmetric topologies, which involves one Interleaved Full-bridge side and a Half-bridge side.

- Chapter 7 analyses two asymmetric topologies involving Half-bridge and Full-bridge sides. In this chapter, a novel modulation scheme is also presented.
- Chapter 8 analyses the last two topologies, which associates Full-bridge and Interleaved Full-bridge sides. A new modulation is also presented in order to reduce the transformer current.
- Chapter 9 presents the modeling and test of two magnetic integrated devices. One integrates two magnetic elements into a single core while the other integrates four magnetic elements into a single core.
- Chapter 10 reviews the work contributions and presents the conclusions.

2 PROPOSED FAMILY OF CONVERTERS

2.1 Origin

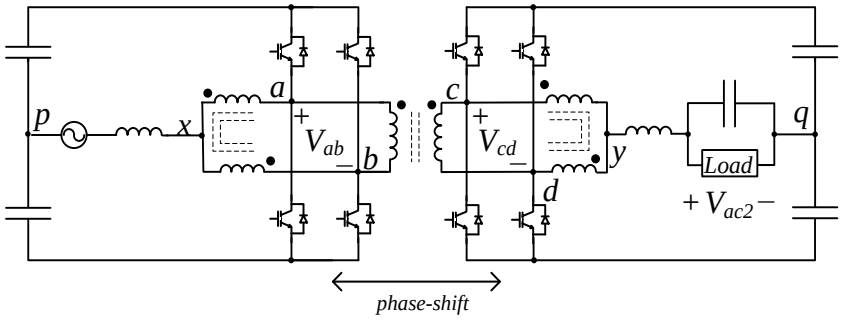
The proposed family of converters has its roots on the AC-AC topology presented by (OLIVEIRA *et al.*, 2012) reproduced in Figure 5. Notice that the AC-AC conversion is performed without bidirectional switches. This topology is based on the DAB (*Dual Active Bridge*) converter and on the interleaving technique, which uses an autotransformer (interleaved transformer). There are two interphase transformers, one connected to the source and another to the load.

The presented topology can be viewed as two half-bridge converters (one connected to the source and other to the load) with interleaving. The maximum voltage applied to the source and to the load is half of the DC-link voltage, due to the half-bridge connection. In order to improve the DC-link usage, one can add one bridge leg replacing the central connection of the DC-link, creating a full-bridge topology. This change can be performed in the source side, load side or both, creating three new topologies with different characteristics. However, considering all combinations, one part of the topology remains unchanged, the base-topology. This arrangement of switches and magnetic devices is presented in Figure 6.

2.1.1 Base topology

The base topology is divided into two sides: the primary side (connected to the source) and the secondary side (connected to the load). One interleaved transformer and two

Figure 5 – Original converter proposed by (OLIVEIRA *et al.*, 2012).

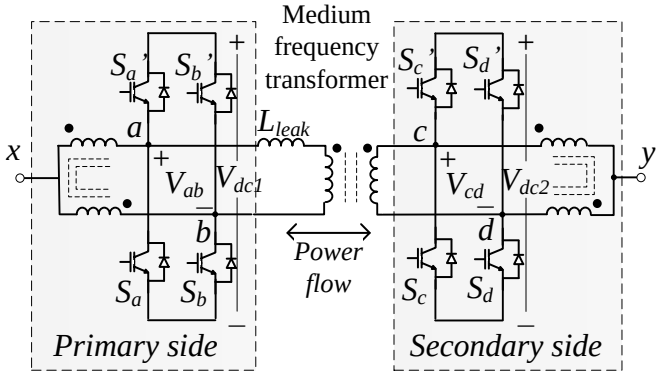


Source: (OLIVEIRA et al., 2012) and modified.

bridge legs compose each side of the topology. A medium frequency transformer responsible for the isolation lies between the two sides. The energy transfer inductance L_{leak}, is displayed separately to ease the visualization but can be constructed integrated with the transformer. Each side of the topology has one constant DC-link, V_{dc1} and V_{dc2}. (not shown). The DC-link determines, from the switches states, the voltages V_{ab} and V_{cd} in the primary and secondary sides of the transformer, respectively. Such voltages, together with the leakage inductance (energy transfer inductance) and the phase-shift modulation control the power flow between both sides of the base-topology, which can be bidirectional. The voltage obtained between the point 'x' of Figure 6 and the source, and between the point 'y' and the load, depending on the topological arrangement connected. Regarding the topology presented in Figure 5, the voltage between the point 'x' and 'p' has three levels. When a Full-bridge topology is used, a five-level voltage is obtained. In summary, from the base topology, one formulates many distinct topologies, which establishes a family of AC-AC converters.

The proposed family of converters has, like remarks, the use of the DAB converter and the interleaving technique. The DAB converters allow high power densities as well as soft switching. The interleaving technique shares the currents uniformly between the semiconductors, which reduce the current stress and costs. Moreover, the interleaving improves the loss distribution, which allows high power applications (BASCOPE; FERREIRA NETO; BASCOPE, 2011). The high-frequency transformer reduces volume and losses. The constant DC-link decouples source and load, in such a way that perturbation in one side does not affect the other side. In addition, the converters allow input power factor correction and an effective frequency in passive elements higher than the switching frequency, which enables filter reduction.

Figure 6 – Base topology common to all topologies of the proposed family.



Source: Author.

2.2 Classification

As many different topologies are proposed, it is necessary to classify and nominate then according to a criterion. As presented before, the topologies of the family have a common base-topology (Figure 6). Thereby, the differences between topologies are restricted to the topological arrangements ‘P’ and ‘Q’ presented in Figure 7a. Two of them were already mentioned: half-bridge and full-bridge. There is another possibility, which consists of two new legs with an interphase transformer.

The arrangements possibilities are:

- Half-bridge (HB) – topology presented by (OLIVEIRA *et al.*, 2012) (presented in Figure 7b).
- Full-bridge (FB) – replacement of the central connection of the DC-link in Figure 5 with one bridge leg (Figure 7c).
- Interleaved full-bridge (IFB) – replacement of the central connection of the DC-link in Figure 5 with two legs and one interphase transformer (Figure 7d).

Distinct arrangements can be adopted in the primary and secondary sides, which lead to nine different topologies to be analysed (Table 1). From all possible topologies, three have the same arrangement in the primary and secondary and are considered symmetric.

Notice that the connections ‘P’ and ‘Q’ are the input of the arrangements. The input of the converter is the port established between the connection ‘P’ and the point ‘x’, while the output of the converter is the port set between the connection ‘Q’ and the point ‘y’.

Table 1 – Nomenclature of the topologies defined from arrangements ‘P’ and ‘Q’.

		Arrangement Q	
Arrangement P	***Half-bridge (HB)***	***Full-bridge (FB)***	***Interleaved full-bridge (IFB)***
Half-bridge (HB)	Symmetric Half-bridge (SHB)	Half-bridge/ Full-bridge (HB-FB)	Half-bridge/Interleaved Full-bridge (HB-IFB)
Full-bridge (FB)	Full-bridge/Half-bridge (FB-HB)	Symmetric Full-bridge (SFB)	Full-bridge / Interleaved Full-bridge (FB-IFB)
Interleaved full-bridge (IFB)	Interleaved Full-bridge/Half-bridge (IFB-HB)	Interleaved Full-bridge/Full-bridge (IFB-FB)	Symmetric Interleaved Full-bridge (SIFB)

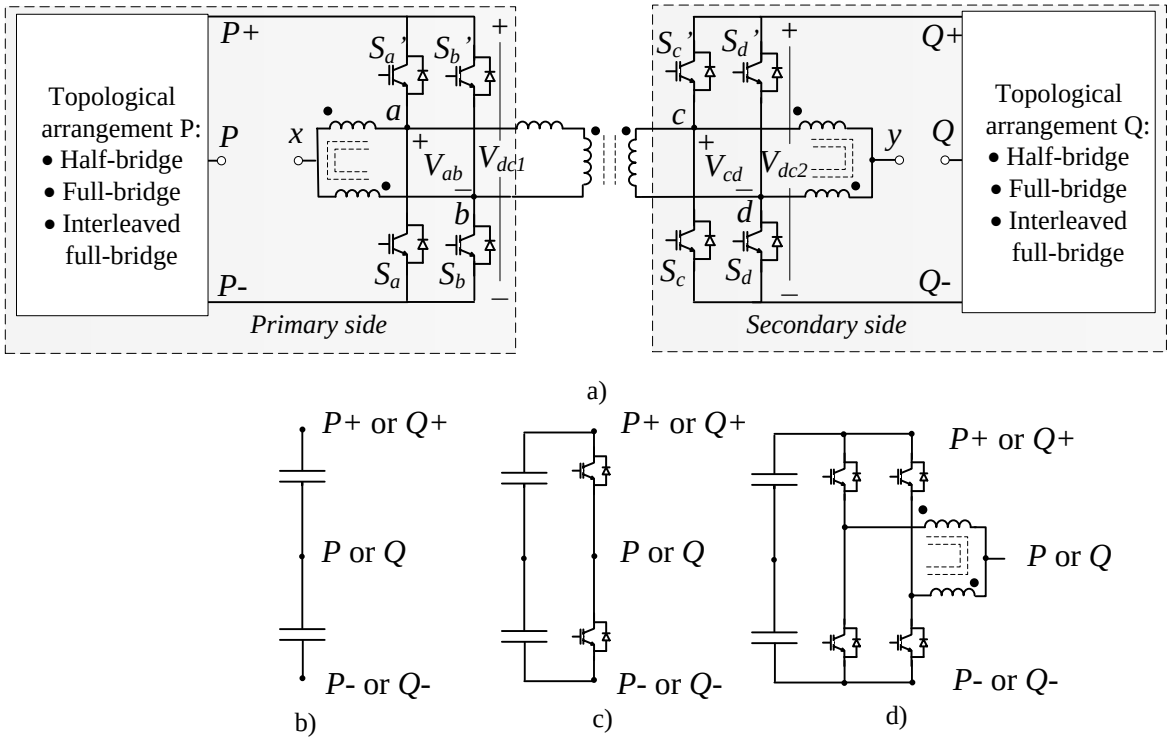
Source: Author.

2.2.1 Characteristics of the proposed converters

The arrangements previously defined provide certain characteristics to the sides of the converter. These characteristics are listed below:

- The number of levels of the voltages formed in the input/output of the converter. The number of levels affects the voltage WTHD (Weighted Total Harmonic Distortion), which is related to the size of the inductive filters;
- The maximum possible value of the voltage which can be applied to the input/output of the converter with relation to the DC-link voltage – indicates the DC-link usage;
- Number of employed semiconductors – this quantity is tied to the cost of the converter;
- Number of discrete/individual magnetics needed – this amount is associated with costs and losses;

Figure 7 – Classification of the proposed family: a) classification according the topological arrangements; b) half-bridge arrangement; c) full-bridge arrangement; d) interleaved full-bridge arrangement.



Source: Author.

- Effective frequency obtained in the input/output of the converter – this value depends on the arrangement used and can lead to smaller filters.

As the converter is formed by two sides, its characteristics are defined as a combination of the characteristics of its sides. For this reason, it is important to identify the characteristics of the sides of the converter according to the arrangement it contains.

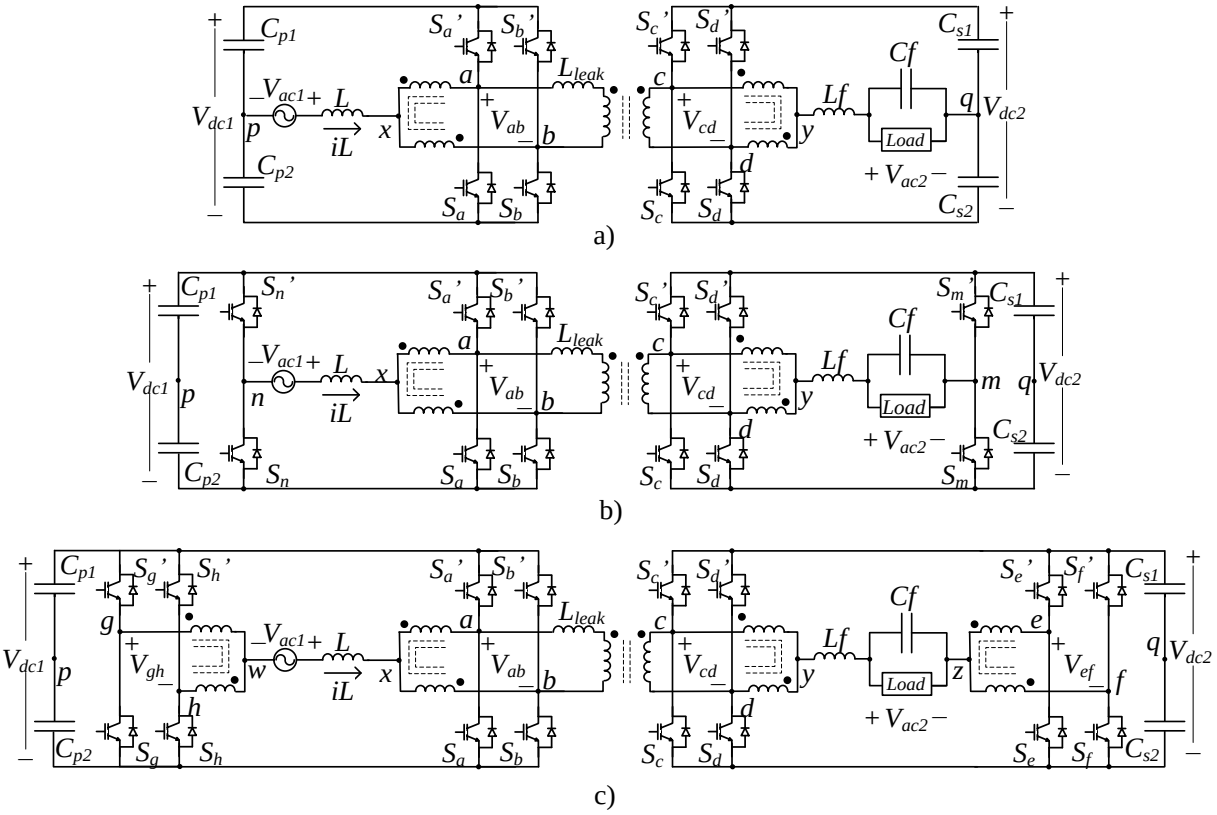
2.3 Converters

Figure 8 shows the symmetric topologies of the family of the proposed converters. The main characteristics of such topologies are the use of the same arrangement for ‘P’ and ‘Q’. This ease the analysis of the converter and can reduce the transformer’s current, as it will be presented afterward. There are three symmetric topologies in the family: the Symmetric Half-bridge (SHB), Symmetric Full-bridge (SFB) and Symmetric Interleaved Full-bridge (SIFB).

The Symmetric Half-bridge (SHB) is presented in Figure 8a An interleaved transformer, two legs and a DC-link with the connection in the middle point compose each side of the converter. The primary side is connected to the source through the inductance L while the secondary side is connected to the load through an LC filter. This is common to all topologies. This is the simplest converter and it presents the minimum number of switches (eight) among all possible converters. A three-level voltage is set in the input/output of the converter and the effective frequency obtained is twice the switching frequency, however, due to the half-bridge characteristic, only half of the DC-link voltage can be applied. This topology does not need any other magnetic device beside the inductive filters of the input and output. The input/output of the converter features a five-level voltage with the same effective frequency of the previous case.

The Symmetric interleaved full-bridge (SIFB) is presented in Figure 8c. The arrangements ‘P’ and ‘Q’ assume the form of Figure 7d. Notice that two interleaved transformers are added and they increase the input/output effective frequency to four times the switching frequency. This is possible at the cost of the highest number of switches among the possible configurations: sixteen. The number of voltage levels and the DC-link usage remains the same when compared to the SFB topology.

Figure 8 – Symmetric topologies of the proposed family: a) symmetric half-bridge; b) symmetric full-bridge; c) symmetric interleaved full-bridge.



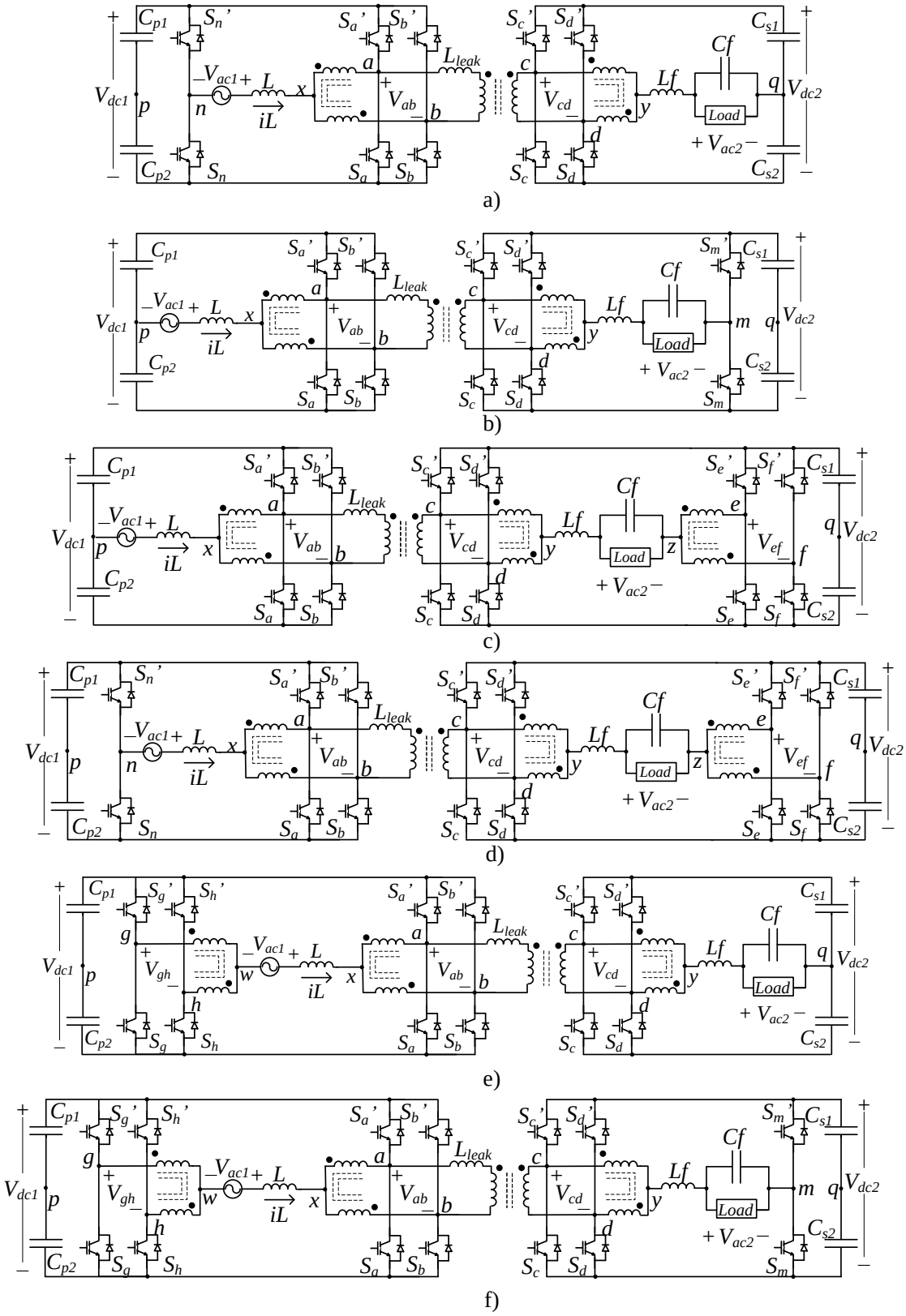
Source: Author.

The Symmetric Full-bridge (SFB) is presented in Figure 8b. As mentioned before, a leg replaces the DC-link central connection. The number of switches increases to twelve with the advantage of full DC-link usage. As in the previous case, no additional magnetic is needed.

The asymmetric topologies formed by the combination of the arrangements ‘P’ and ‘Q’ are presented in Figure 9. Essentially, the characteristics of the asymmetric topologies are a combination of the characteristics of the converters’ sides defined by the arrangements ‘P’ and ‘Q’. It will be shown, however, important differences related to the instantaneous voltage applied to the transformer, which affects the efficiency of the converters.

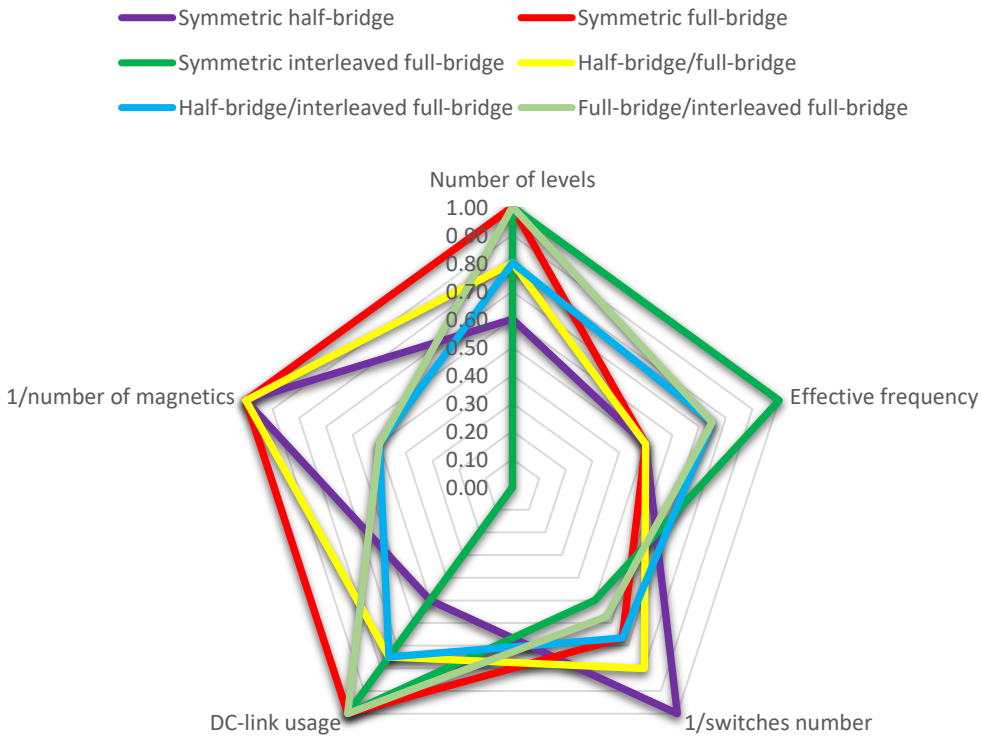
Figure 10 presents a summary of the characteristics of all proposed topologies. In this graph, the biggest area presents the best characteristics. The counterparts of the asymmetric topologies are not shown since they present the same results. One notices that the Symmetric full-bridge converter presents the best set of characteristics followed by the half-bridge/full-bridge. The Half-bridge/interleaved full-bridge presents the worst set of characteristics.

Figure 9 – Asymmetric topologies of the proposed family: a) Full-bridge/Half-bridge; b) Half-bridge/Full-bridge; c) Half-bridge/Interleaved Full-bridge; d) Full-bridge/Interleaved Full-bridge; e) Interleaved Full-bridge/Half-bridge; f) Interleaved Full-bridge/Full-bridge.



Source: Author.

Figure 10 – Comparison between the proposed converters.



Source: Author.

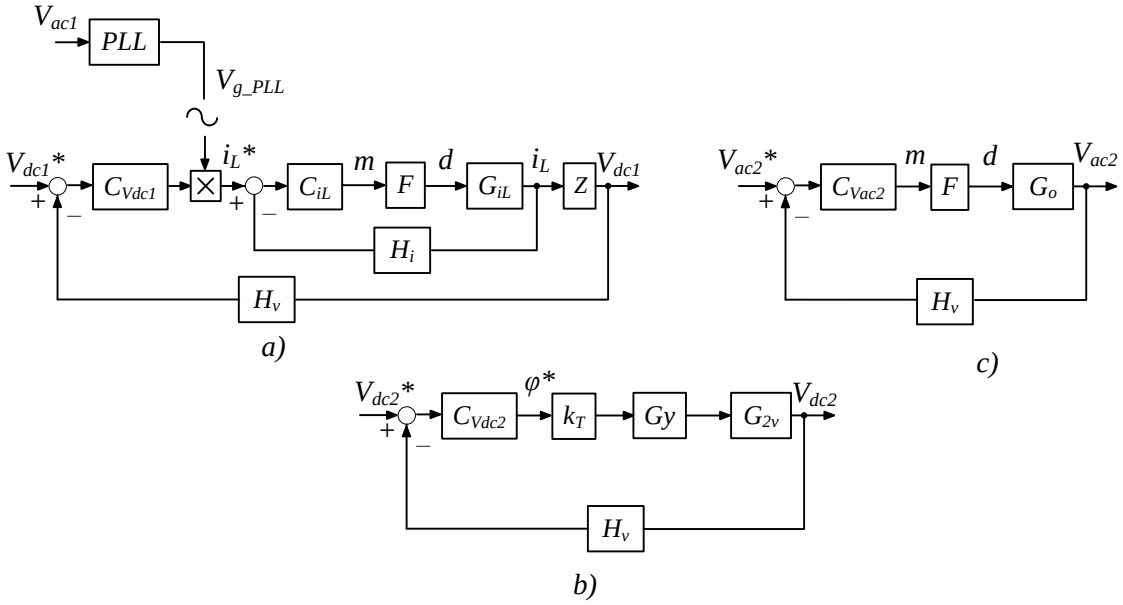
2.4 Converters steady-state behaviour and control strategy

All converters perform AC-AC conversion and they behave similarly in steady state. They must maintain a sinusoidal input current *iL* in phase with the grid voltage V_{ac1} performing Power Factor Control (PFC). In addition, they must control the DC-link voltages V_{dc1} and V_{dc2} at constant values. Moreover, they must control the output voltage (load voltage) V_{ac2} and maintain it sinusoidal in the event of load change or voltage sag or swells. Figure 11 presents the generic control block diagram used by every converter of the proposed family.

2.4.1 Input current and DC-link voltage control of the primary side

The current and voltage use a cascade control scheme. The outer loop controls the DC-link voltage V_{dc1}, while the inner loop controls the input current *iL*. The transfer function G_{iL} relates the input current with the duty cycle while the impedance *Z* relates the input current

Figure 11 – Control block diagrams for the proposed converters.



Source: Author.

with the DC-link voltage. The transfer function is based on the boost converter (ORTMANN, 2012). The controller C_{Vdc1} used to track the reference value V_{dc1}* and its output is multiplied by the grid reference given by the PLL. This generates the current reference *iL** which is in phase with the input voltage V_{ac1} enabling Power Factor Correction. As this current reference is sinusoidal, it is adopted a resonant controller, in order to guarantee zero error in steady state.

2.4.2 Secondary side DC-link voltage control

The control of the voltage V_{dc2} is performed controlling the power flow between the converter's sides. Considering constant the load and the voltage V_{dc1}, increasing the power flow stores energy in the secondary DC-link, which increases the voltage. When the power flow is decreased under the load requirements, the voltage of the secondary DC-link reduces.

In order to perform such control, the phase-shift modulation is used and the secondary DC-link voltage is controlled using Gyrator theory. The block diagram of Figure 11b presents the modulator gain k_T, the Gyrator gain (*Gy*) and the transfer function *G2v*. The controller C_{Vdc2} set the phase-shift between primary and secondary sides' bridges to make V_{dc2} equal to its reference value, V_{dc2}*. The transfer function, the gains and the procedures to implement this control strategy are described in (SANTOS, 2011).

2.4.3 Load voltage control

The load voltage must be sinusoidal with constant amplitude. Figure 11c presents the block diagram for the control of the load voltage (V_{ac2}). This is the simplest control block where the controller C_{Vac2} is resonant. The transfer function G_{Vac2} relates the load voltage with the duty cycle. The block H_v is the voltage sensor gain and the block F is the modulator.

3 SYMMETRIC HALF-BRIDGE CONVERTER

The Symmetric Half-bridge converter is the simplest converter of the proposed family and is composed of only eight switches. This Chapter describes its operation, modulation scheme, modeling of the converter and the transformer, current ripple calculation, ZVS analysis, and experimental results.

The design used to test this converter is also presented. The same design was used to test the other family converters in order to manufacture only one set of magnetic devices. The experimental platform where the test was carried on is also presented. This same platform is used to obtain the results for all converters.

3.1 Operation of the converter

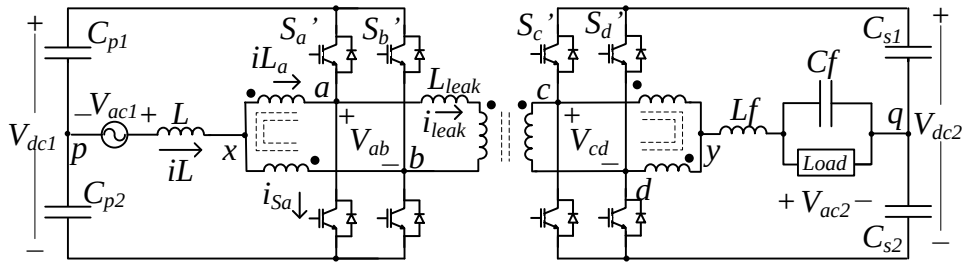
One can consider that each side of the converter (Figure 12) works with two sub-converters, each connected to one leg. Each leg has two complementary switches S_i and S_i', where 'i' can designate *a*, *b*, *c* and *d*. The commands to the legs of the same converter side must have 180º phase-shift in order to set the interleaving. The position of the switches S_a and S_b in the primary side define the voltage v_{ab} (applied to the transformer primary side) and v_{xp} (converter input voltage). The switches S_c and S_d define the voltage v_{cd} (transformer secondary side voltage) and v_{yq} (converter output voltage). The converter voltages are listed in Table 2**.**

Table 2 – Converter voltages of both converter sides.

Switching state		**Voltages**	
S_a/S_c	S_b/S_d	v_{ab} | v_{cd}	v_{xp} | v_{yq}
0	0	0	$V_{dc1}/2$ | $V_{dc2}/2$
0	1	V_{dc1} | V_{dc2}	0
1	0	$-V_{dc1}$ | $-V_{dc2}$	0
1	1	0	$-V_{dc1}/2$ | $-V_{dc2}/2$

Source: Author.

Figure 12 – Symmetric Half-bridge converter.



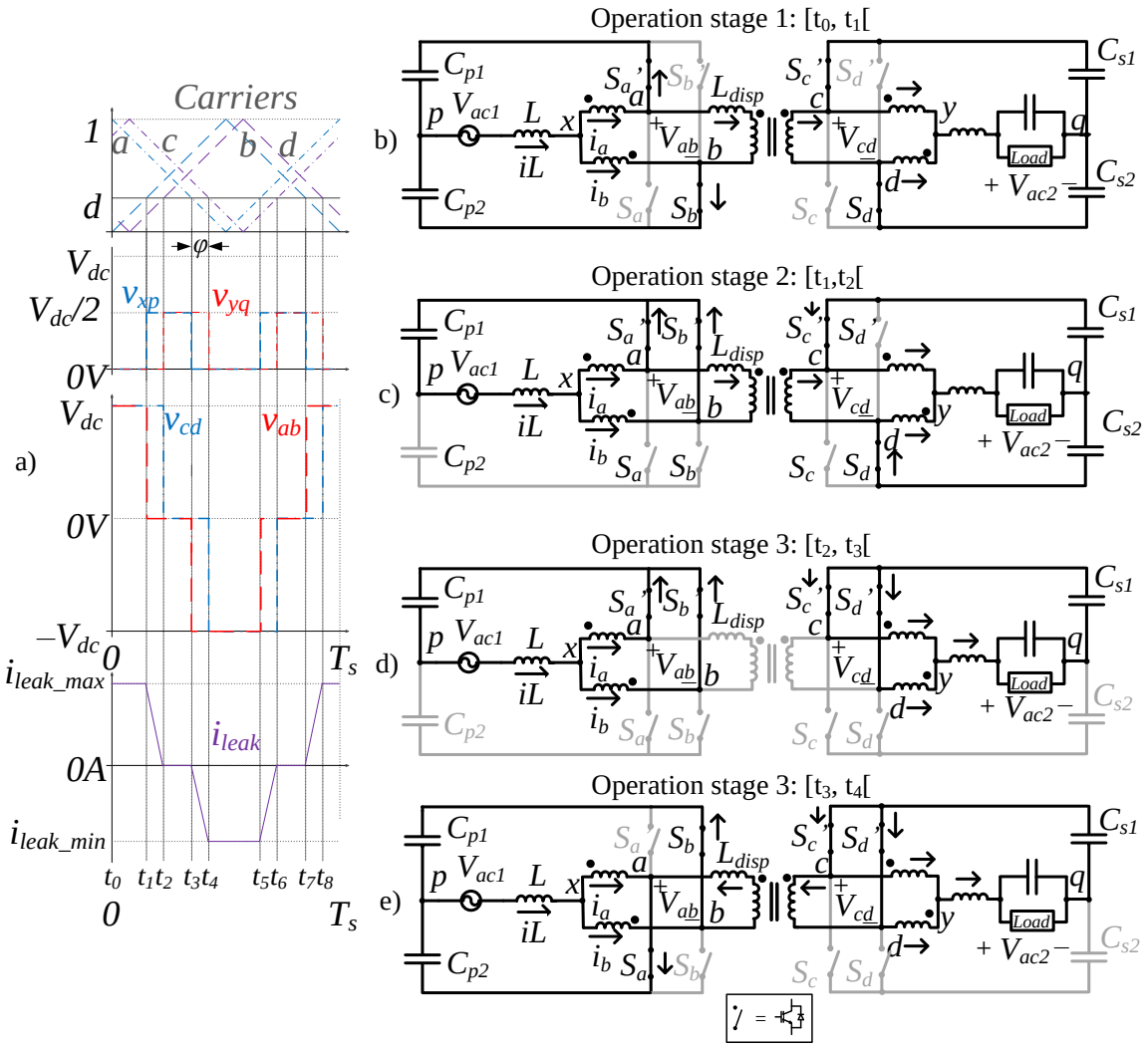
Source: Author.

Figure 13 presents a summary of the converter voltages. Figure 13a presents key voltages and currents waveforms of the converter for a duty cycle value *d*. Notice that the carriers 'a', 'b' and 'c' and 'd' of the primary and secondary sides, respectively, are phase-shifted by φ. There are eight distinct time intervals[1] but only four are analysed since the behaviour of the others is similar. It is considered that the current *iL* and the load current are positive and the initial current in the transformer is in its maximum. Each time interval defines an operational stage and they are described below:

- Operation stage 1 [t_0, t_1[(Figure 13b): the switches S_b and S_d are turned on, which applies zero voltage to the input (v_{xp}) and output (v_{yq}) of the converter. The primary and secondary windings of the transformer are submitted to V_{dc1} and V_{dc2}, respectively. The transformer current remains equal to the initial value.
- Operation stage 2 [t_1, t_2] (Figure 13c): during this stage the switch S_b is turned off, which short circuit the interleaved transformer of the primary side, imposing the voltage $V_{dc1}/2$ to the input. The transformer primary winding voltage becomes zero and its current start to decrease from its previous value. The converter output voltage remains zero.
- Operation stage 3 [t_2, t_3[(Figure 13d): the switch S_d is turned off. Now, the interleaved transformers of both sides are in short. Both input and output voltages are half of their DC-link voltage. The voltage in both transformer's windings is equal to zero and its current reaches zero.
- Operation stage 4 [t_3, t_4[(Figure 13e): in this stage the switch S_a turns on, which makes the converter input voltage zero again. The output voltage remains $V_{dc2}/2$ and the voltage v_{ab} becomes negative ($-V_{dc1}$) while the voltage v_{cd} remains zero. This increase the transformer current in the opposite direction.

[1] The dead time is not considered in this analysis or in any other analysis contained in this thesis.

Figure 13 – Operation of the converter: a) key voltages and currents of the converter; b) operation stage 1; c) operation stage 2; d) operation stage 3; e) operation stage 4.



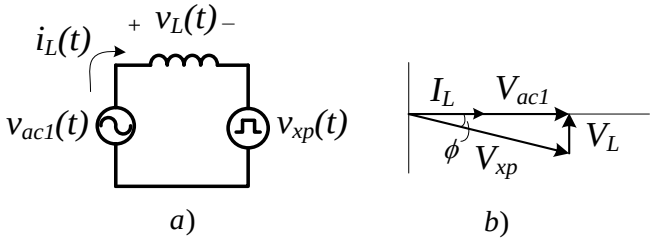
Source: Author.

3.2 Modelling input/output of the converter

The primary side of the converter is modelled, in a simplified way, as two voltage sources connected to each other through an inductor L (Figure 14), where $v_{ac1}(t)$ is the grid voltage, $v_{xp}(t)$ is the converter input voltage and $v_L(t)$ is the voltage applied to the inductor L. This approach follows the procedure adopted in (ORTMANN, 2012). The modelling of the secondary side is similar to the primary side due to the symmetry and thus will be omitted.

The analysis considers steady state, where converter input voltage and current are in phase, as presented in Figure 14b. which is only possible if the converter input voltage is

Figure 14 – Simplified model: a) circuit; b) phasor diagram.



Source: Author.

delayed from the grid voltage by the phase ϕ. Based on this, the duty cycle function can be determined.

3.2.1 Duty cycle function

The duty cycle function defines the variation with time of the duty cycle applied to the switches. In this regard, one needs to determine the mean value of the converter input voltage in one switching period. Applying circuit analysis to the Figure 12 and considering all magnetic elements ideal, the instantaneous converter input voltage $v_{xp}(t)$ is written based on gating functions (a function variating with time, which is 1 when the switch is on and 0 when it is off) of each switch.

$$v_{xp}(t) = \frac{V_{dc1}}{4} \cdot \left(\delta_{Sa'}(t) + \delta_{Sb'}(t) - \delta_{Sa}(t) - \delta_{Sb}(t) \right) \tag{1}$$

The mean value in one switching period is given as:

$$\overline{v_{xp}} = \frac{1}{Ts} \int_{o}^{Ts} v_{xp}(t) \cdot \mathrm{dt} = \frac{V_{dc1}}{2} \cdot \left(1 - D_a - D_b\right) \tag{2}$$

Considering that the duty cycle varies with time, the mean value can be written as:

$$\overline{v_{xp}}(t) = \frac{V_{dc1}}{2} \cdot \left(1 - d_a(t) - d_b(t)\right) \tag{3}$$

It is considered that the duty cycle functions applied to the pair of legs is equal, so $d_a(t) = d_b(t) = d_{ab}(t)$. Thus, (3) is simplified to:

$$\overline{v_{xp}}(t) = \frac{V_{dc1}}{2} \cdot \left(1 - 2 \cdot d_{ab}(t)\right) \tag{4}$$

The grid voltage and current are in phase and are defined in (5)**,** where ω_g is the angular velocity of the grid voltage (v_{ac1}).

$$v_{ac1}(t) = V_{ac1} \cdot \sin(\omega_g \cdot t)$$
$$i_L(t) = I_L \cdot \sin(\omega_g \cdot t) \quad (5)$$

Figure 14b presents a simplified phasor diagram of the circuit. Considering unitary power factor the converter input voltage is given by:

$$\overline{v_{xp}}(t) = V_{xp} \cdot \sin(\omega_g \cdot t + \phi) \quad (6)$$

With,

$$V_{xp} = \sqrt{V_{ac1}^2 + \left(\omega_g \cdot L \cdot I_L\right)^2}$$
$$\phi = tg^{-1}\left(\frac{-\omega_g \cdot L \cdot I_L}{V_{ac1}}\right) \quad (7)$$

Making (4) equal to (6), one obtains:

$$d(t) = \frac{1}{2} - \frac{M_f \cdot \sin(\omega_g \cdot t + \phi)}{2} \quad (8)$$

Where M_f is the modulation index given by:

$$M_f = \frac{V_{ac1}}{V_{dc1}/2} \quad (9)$$

3.2.2 Modulation

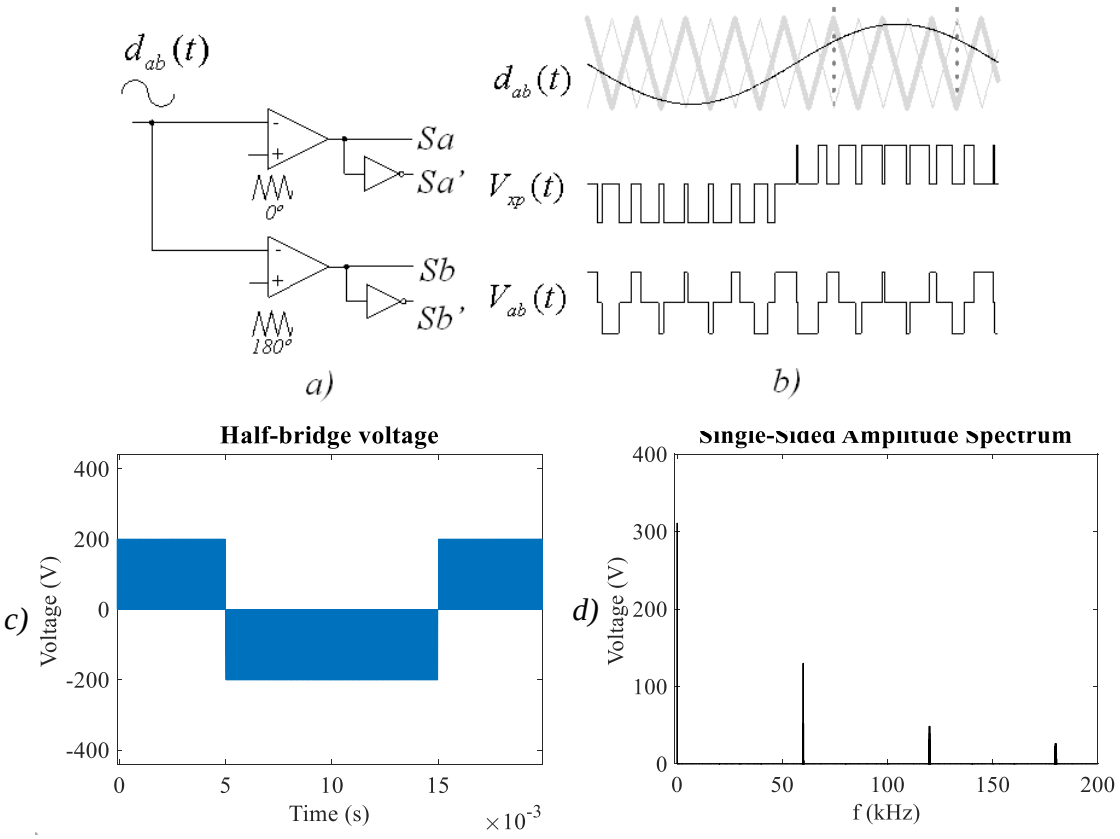
The modulation uses two triangular carriers shifted 180º to achieve interleaving operation. Figure 15a presents the duty cycle function (8) as input to the comparators. Figure 15b presents the carriers, the duty cycle function and the generated voltages (v_{xp} and v_{ab}) in one grid period. The voltage v_{xp} has three levels with 2 times the switching frequency. The voltage v_{ab} is defined from the duty cycle function but it assumes V_{dc1}, 0 e $-V_{dc1}$ in every switching period forming a quasi-square wave as presented in Figure 15b**.**

Figure 15c shows the voltage waveform generated by the Half-bridge arrangement obtained through simulation in open loop, with a DC-link voltage of 800V and a modulation index of 0.7778. The adopted switching frequency is 30 kHz and the fundamental component frequency is 50 Hz.

The harmonic distortion of the generated voltage has been evaluated by calculating the Weighted Total Harmonic Distortion (WTHD). The WTHD is defined as:

$$WTHD = \frac{100}{V_1} \cdot \sqrt{\sum_{n=2}^{Nn}\left(\frac{V_n}{n}\right)^2} \quad (10)$$

Figure 15 – Modulation applied to the primary side of the converter: a) modulation arrangement; b) waveforms (from top to bottom) of the duty cycle and carriers, the converter input voltage and the transformer winding voltage.



Source: Author.

Where V_1 is the amplitude of the fundamental component, V_n is the amplitude of the harmonic n and Nn is the number of harmonics considered in the summation. Figure 15d shows the single-sided amplitude spectrum of the voltage of Figure 15c with harmonics located at 60 kHz, 120 kHz, and 180 kHz. The WTHD was calculate considering Nn = 10000, which resulted in 0.0574.

3.2.3 Current ripple

Considering an ideal interleaved transformer with unitary coupling factor, the input current filtering comes solely from the inductor L. From Figure 14a**,** one determines the input current rate:

$$\frac{diL(t)}{dt} = \frac{v_{ac1}(t) - v_{xp}(t)}{L} \tag{11}$$

One determines ΔiL for the time intervals Δt_1 = [t1,t3] and Δt_2 = [t3,t5] of Figure 6a as:

$$\frac{\Delta iL}{\Delta t_1} = \frac{V_{ac1} - V_{dc1}/2}{L}$$
$$\frac{\Delta iL}{\Delta t_2} = \frac{V_{ac1}}{L} \tag{12}$$

Deriving Δt_1 and Δt_2, and knowing that their summation is half of the switching period, one obtains:

$$\Delta t_1 + \Delta t_2 = \frac{T_s}{2} = \frac{L \cdot \Delta iL}{-V_{ac1} + \frac{V_{dc1}}{2}} + \frac{L \cdot \Delta iL}{v_{ac1}} \tag{13}$$

Deriving ΔiL, one obtains:

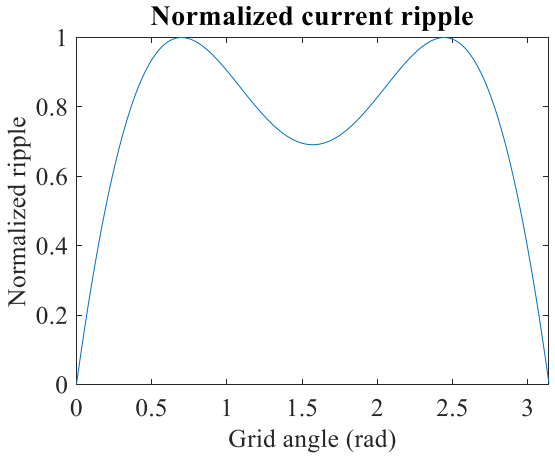
$$\Delta iL = \frac{v_{ac1}\frac{V_{dc1}}{2} - {v_{ac1}}^2}{2 \cdot fs \cdot L\frac{V_{dc1}}{2}} \tag{14}$$

Applying grid voltage definition (5) to (14), one obtains the current ripple after some simplification:

$$\Delta iL(t) = \frac{V_{dc1}}{4 \cdot fs \cdot L}\left(M_f \cdot \sin(\omega_g \cdot t) - M_f^2 \cdot \sin^2(\omega_g \cdot t)\right) \tag{15}$$

The current variation given in (15) is presented in Figure 16.

Figure 16 – Current ripple variation per unit.



Source: Author.

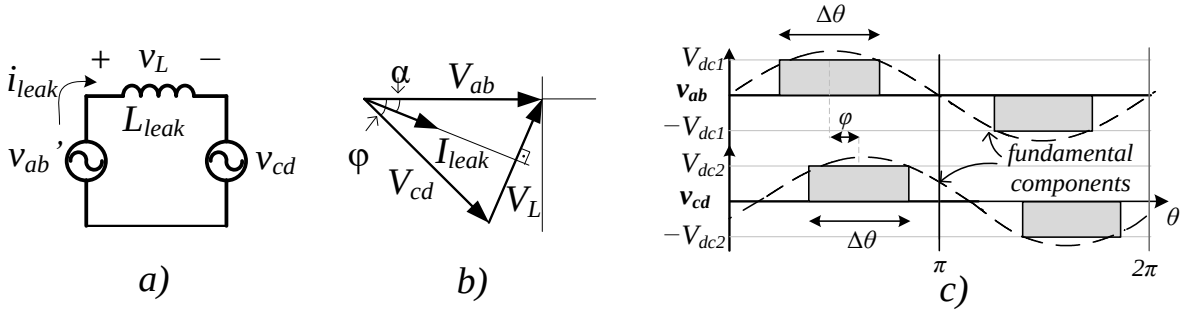
One determines the maximum current deriving (15) with relation to the variable $\omega_g.t$. The maximum current ripple is obtained when $\omega_g \cdot t = \theta_{\max} = \sin^{-1}\left(1/(2 \cdot M_f)\right)$ such that the following inequality holds:

$$\Delta iL \underset{\omega_g \cdot t = \theta_{\max}}{\leq} \frac{V_{dc1}}{16 \cdot fs \cdot L} \tag{16}$$

3.3 Transformer power flow analysis

The transformer's windings are submitted to the voltages v_{ab} and v_{cd} in the primary and secondary respectively. Figure 17a presents the simplified circuit, which considers two sinusoidal voltage sources connected by the leakage inductance of the transformer. To control the power flow between both voltage sources, the phase-shift between v_{ab}' and v_{cd} is used, where v_{ab}' is the primary voltage source reflected to the secondary side through the number of turns N.

Figure 17 – Fundamental transformer model: a) simplified circuit; b) phasor diagram; c) voltage waveforms.



Source: Author.

Considering only the fundamental component of the Fourier series expansion, the voltages $v_{ab}(t)$ and $v_{cd}(t)$ are written as follows:

$$\begin{aligned} v_{ab1}(t) &= \frac{4 \cdot V_{dc1} \cdot \sin\left(\frac{\Delta\theta}{2}\right)}{\pi} \sin(\omega_s \cdot t) \\ v_{cd1}(t) &= \frac{4 \cdot V_{dc2} \cdot \sin\left(\frac{\Delta\theta}{2}\right)}{\pi} \sin(\omega_s \cdot t + \varphi) \end{aligned} \tag{17}$$

Where ω_s is the angular switching frequency and $\Delta\theta$ is presented in Figure 17c**,** which shows the instantaneous transformer windings voltages and their fundamental component with phase-shift φ. The relation between $\Delta\theta$ and the duty cycle function is:

$$\Delta\theta(d) = \begin{cases} 2\pi d & if \quad 0 < d \le 0,5 \\ 2\pi(1-d) & if \quad 0,5 < d \le 1 \end{cases} \tag{18}$$

From (17) and using (18), one obtains the *rms* voltage value for the fundamental component:

$$V_1 = \frac{2\sqrt{2}\cdot V_{dc}\cdot\sin(\pi d)}{\pi} \tag{19}$$

Where V_{dc} assumes the values V_{dc1} or V_{dc2} for v_{ab} and v_{cd}, respectively. The phasor diagram of Figure 17b presents the *rms* values of the voltage fundamental components and specifies an angle α to the current. The mean power is given by:

$$P = V_{ab}\cdot I_{\text{leak}}\cdot\cos(\alpha) \tag{20}$$

The following trigonometric relation is obtained from Figure 17b, where $X_L = \omega_s \cdot L_{leak}$ is the reactance of the leakage inductance.

$$V_L\cdot\cos(\alpha) = V_{cd}\cdot\sin(\varphi) = X_L\cdot I_{\text{leak}}\cdot\cos(\alpha) \tag{21}$$

Applying (21) in (20), one obtains the mean power:

$$P = \frac{V_{ab}\cdot V_{cd}}{X_L}\sin(\varphi) \tag{22}$$

The transformer current is:

$$\dot{I}_{leak} = \frac{V_{ab}\angle 0 - V_{cd}\angle\varphi}{j\cdot\omega_s\cdot L_{leak}} = \frac{N\cdot\frac{2\sqrt{2}\cdot V_{dc1}}{\pi}\sin(\pi\cdot d_{ab}) - \frac{2\sqrt{2}\cdot V_{dc2}}{\pi}\sin(\pi\cdot d_{cd})\cdot e^{j\varphi}}{j\cdot\omega_s\cdot L_{disp}} \tag{23}$$

Notice in (22) and (23) that both mean power and current depends on the duty cycle functions applied to the transformer's windings. Considering then equal, i.e. $d_{ab} = d_{cd}$, using (8) in (19) and applying the result to (22), one obtains the mean power changing with time:

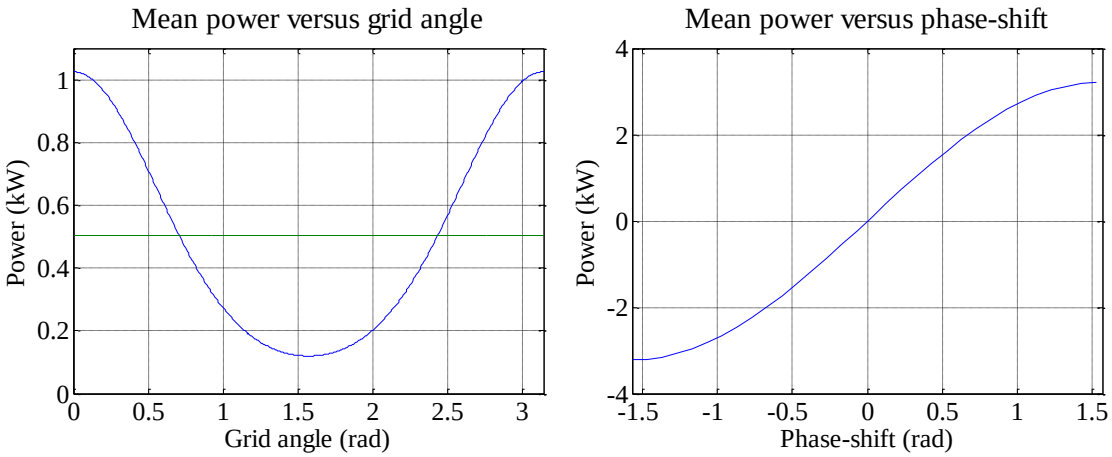
$$P_{hb}(\omega_g\cdot t,\varphi) = \frac{8\cdot N\cdot V_{dc1}\cdot V_{dc2}\cdot\sin(\varphi)}{\pi^2\cdot L_{leak}\cdot\omega_s}\cos^2\left(\frac{\pi\cdot M_f\cdot\sin(\omega_g\cdot t)}{2}\right) \tag{24}$$

Where ω_g is the grid angular frequency. The mean power transferred in one grid period is given by:

$$P_{mean\_hb}(\varphi) = \frac{1}{\pi}\int_0^{\pi} P_{hb}(\omega_r \cdot t, \varphi)\, d\omega_r t \tag{25}$$

Given a required power flow in one grid period and the phase-shift angle φ, one determines numerically with (25) the required leakage inductance. Figure 18 an example of how the power changes with the grid period (Figure 18a) and with the phase-shift (Figure 18b).

Figure 18 – Example of power flow variation for the Symmetric half-bridge converter with V_{dc1} = V_{dc2} = 400V, fs = 30 kHz, M_f = 0.778 and L_{leak} = 108 µH, for 500W mean power: a) according to the grid voltage θ for φ = 9º showing the mean value in one grid period (straight line); b) according to the phase-shift.



a) b)

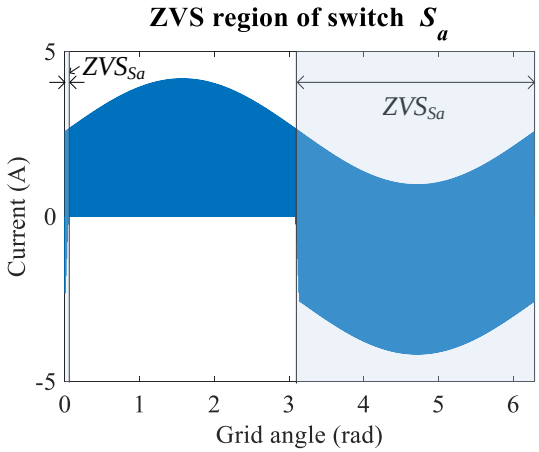
Source: Author.

3.4 ZVS analysis

The high-frequency current of the transformer circulates through the switches of legs ‘a’, ‘b’, ‘c’ and ‘d’, which influences the ZVS. From Figure 12, the current that enters the node ‘a’ is given by $i_a = iL_a - i_{leak}$. Where iL_a is half of the current iL.

Considering an ideal analysis where d_{ab} = d_{cd} and considering the input current purely sinusoidal the ZVS region of the switch S_a is presented in Figure 19 together with the current in the switch S_a given by $i_{Sa} = g_a \cdot i_a$. Where g_a is the gate signal applied to the switch. The ZVS region for the Sa switch is ~3.25 rad (186º), i.e., slightly higher than half of the input grid period. The ZVS regions of the other switches are similar.

Figure 19 – Current and ZVS region of switch S_a of the SHB converter.



Source: Author.

3.5 Design

This section presents a general design, which is used by different converters, not only the Symmetric Half-bridge. Table 3 presents the main requirements used to design the passive elements needed by the converters.

Table 3 – Design parameters of the prototype.

Parameters	**Value**
Nominal power	
With half-bridge arrangement	0.5 kW
With only Full-bridge and I-full-bridge arrangements	1 kW
Input/output rms voltage V_{ac1}/V_{ac2}	
Half-bridge arrangement	110 V
Full-bridge and I-full-bridge arrangements	220V
Switching frequency	30 kHz
Load	24.4 Ω/0.5 kW 48.4 Ω/1 kW
Grid frequency	50 Hz
DC-link voltages (V_{dc1}, V_{dc2})	400 V

Source: Author.

3.5.1 Input inductor

The input inductor is defined in order to have the required current ripple. Considering (16) as a basis and 20% current input ripple, the required input inductance is 683 µH. The core adopted was AMCC-6.3 manufactured with iron-based Metglas® amorphous alloy 2605SA1. Table 4 presents a summary of the inductor design. The output inductor, which composes the *LC* filter is designed using the same parameters.

Table 4 – Design parameters of the input inductor.

Parameter	**Value**
Core	AMCC-6.3
Material	2605SA1- Hitachi
Peak flux density (B_{peak})	0.67 T
Flux density ripple (ΔB)	0.12 T
Inductance (L)	645 µH
Ripple frequency	60 kHz
Inductance fator (A_L)	350 nH/turns^2
Current density	350 A/cm^2
Wire diameter	1.4 mm
Air gap	0.4 mm
Number of turns	41 turns

Source: Author.

3.5.2 Interleaved transformer

The interleaved transformer is designed in order to have a coupling factor near the unity. Therefore, it does not contribute to the input/output inductance. A ring ferrite core (B64290L0082X087) with N87 material is used.

Table 5 – Design parameters of the interleaved transformer.

Parameter	**Value**
Core	B64290L0082X087
Material	N87 - TDK
Max. flux density B_{max}	0.13 T
Ripple frequency	30 kHz
Inductance fator (A_L)	4460 nH/turns^2
Current density	400 A/cm^2
Wire diameter	0.8 mm
Number of turns	128 turns

Source: Author.

3.5.3 Transformer

The transformer is designed to transfer 0.5 kW with 9º phase-shift with the parameters given in Table 3. Using (25), the calculated leakage inductance is 108 µH. This inductance is integrated into the transformer, as detailed explained in Section 9.3. An E 55/28/21 core was used. The adopted core material was N87 from EPCOS.

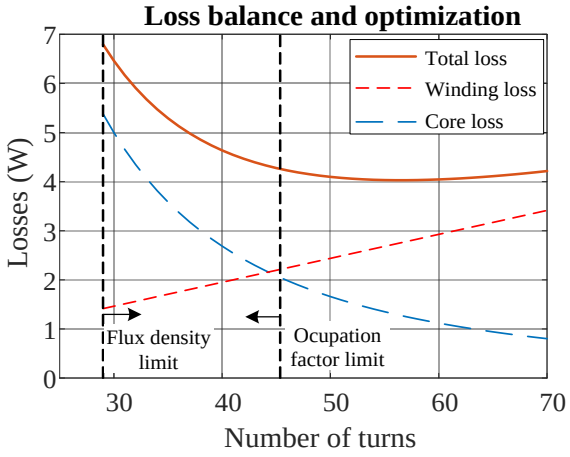
Table 6 – Design parameters of the transformer.

Parameter	**Value**
Core	E 55/28/21
Material	N87 - TDK
Flux density	0.19 T
Number of turns	45/45
Current density	450 A/cm^2
Leakage inductance	108 µH
Occupation fator (ku)	0.4
Litz wire	25 x 0.2

Source: Author.

Figure 20 presents the loss balance of the designed transformer with the core, winding and total losses ((ZACHARIAS, 2020). The minimum number of turn to avoid core saturation is 29 turns. At this point, the core losses dominate the winding losses. The minimum losses are obtained with 55 turns, but this design point exceeds the occupation factor limit of 0.4, which occurs with 45 turns. The transformer is then manufactured with 45 turns.

Figure 20 – Transformer loss balance and optimization.



Source: Author.

3.5.4 Output LC filter

The LC filter was designed following (DAHONO; PURWADI; QAMARUZZAMAN, 1995) procedure. Given the already designed inductance of 645 µH and assuming an output voltage ripple of 7 V, the required filter capacitance is 220 nF. Table 7 presents a summary of the LC filter parameters.

Table 7 – LC filter design summary.

Parameter	**Value**
Filter inductance (L_f)	646 µH
Output voltage ripple (Δv_{ac2})	10V
Calculated filter capacitance	154 nF
Adopted filter capacitance (C_f)	220 nF - B3202 MKP TDK

Source: Author.

3.6 Losses estimation

This section presents the losses estimation of the Symmetric Half-bridge converter in order to determine its theoretical efficiency. The estimated losses sources are switches, magnetic devices, and DC-link capacitors.

3.6.1 Conduction and switching losses determination

The SCT3120AL switch, from Rohm, was used to obtain the experimental results. It is a SiC MOSFET with a typical R_{DSon} of 120 mΩ, blocking voltage of 650V and continuous drain current of 21A. Based on the datasheet information and using the simulation software PLECS®, one determines the conduction and switching losses of the semiconductor devices, which are summarized in Table 8.

Table 8 – Losses of the SHB converter with SCT3120AL switch.

Losses	**Value**
Conduction losses	6.86 W
Switching losses	9.08 W
Total losses	**15.94 W**

Source: Author.

3.6.2 Magnetic devices losses

Regarding the input/output inductors and the both interleaved transformers, the losses calculation considered the ohmic losses in the windings and the core losses. The core losses were calculated using the Steinmetz equation, where the coefficients were obtained from the respective materials datasheets.

In addition to the ohmic part, the transformer core losses were calculated using the i^2GSE (*improved-improved generalized Steinmetz equation*). This method takes relaxation losses into account and improves DAB transformer losses estimation (MUHLETHALER *et al.*, 2011).

Table 9 – Magnetic devices losses.

Device	**Losses value**
Input/output indutor	3.50 W / 3.50 W
Input/output interleaved transformer	4.23 W / 4.23 W
Transformer	3.14 W
Total	**18.60 W**

Source: Author.

3.6.3 Electrolytic capacitor losses

The losses of the DC-link can be calculated considering the ESR (Equivalent Series Resistance) of the capacitor and the current that flows through it. Each DC-link of the experimental platform is composed of three ELH687M450AT8 (680µF/450V) capacitors. Two of them are connected in series exposing the central point of the DC-link. The other capacitor is connected in parallel to this association. The grid current is divided between the series association, which makes 50Hz current circulate through the capacitors. In addition, high current with double the switching frequency is present. Through the parallel capacitor circulates 100 Hz current component as well as the high-frequency component.

As the ESR is frequency dependent, its value is estimated from datasheet graphs. The result of the ESR estimative form the datasheet is presented for each frequency in Table 10. The total calculated power loss is 11 W.

Table 10 – Current values for the SHB converter and the estimated ESR values for the ELH687M450AT8 capacitor.

Capacitor	RMS current value	Estimated ESR value
Series associated capacitor	2.33 A @ 50 Hz	0.468 Ω
	0.54 A @ 60 kHz	0.012 Ω
Parallel associated capacitor	1.06 A @ 100 Hz	0.351 Ω
	1.09 A @ 60 kHz	0.012 Ω

Source: Author.

3.7 Experimental results

3.7.1 Experimental setup

The family of the proposed converters has nine different topologies. It is desirable to test all topologies using a single prototype, which would save the time to design, mount and test one exclusive board for each converter as well as reduce costs.

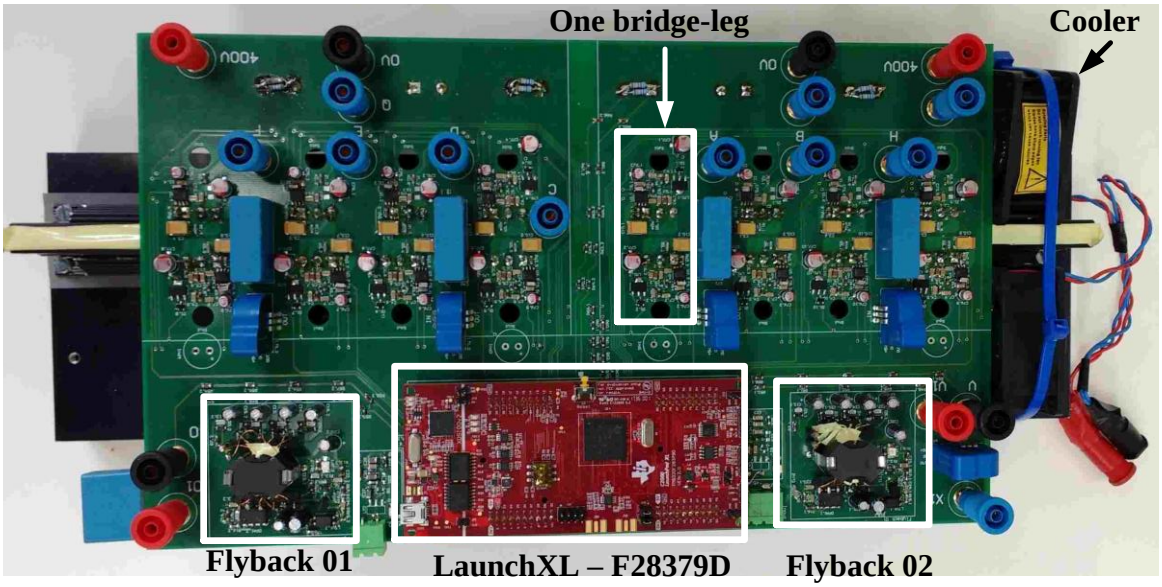
For this reason, one experimental platform was designed with which all converters can be tested. Figure 21 presents the constructed experimental platform highlighting its main parts. The PCB is divided into two parts, the primary side, and the secondary side, which are isolated. Each side is composed of four legs. Each switch is driven by one isolated UCC5350MC single-channel gate driver. As the gate-drain voltages of the upper switches of each leg must be isolated, two separate Flyback are provided, each with five isolated outputs. The PWM signals, as well as the controllers, run in the DSP-based platform LaunchXL-F28379D. The main components employed in the experimental platform are listed in Table 11.

Table 11 – Main experimental platform components.

Component	Specification
SiC switches	SCT3120AL
	SCT3030AL
Isolated gate driver	UCC5350MC
DC-link primary side (1.02mF)	3x680µF/450V - ELH687M450AT8
	2x1.5µF/630V - B32774P6155K000
DC-link secondary side (1.02mF)	3x680µF/450V - ELH687M450AT8
	2x1.5µF/630V - B32774P6155K000
Current sensor	1xLTS 15-NP - LEM

Source: Author.

Figure 21 – Experimental platform



Source: Author.

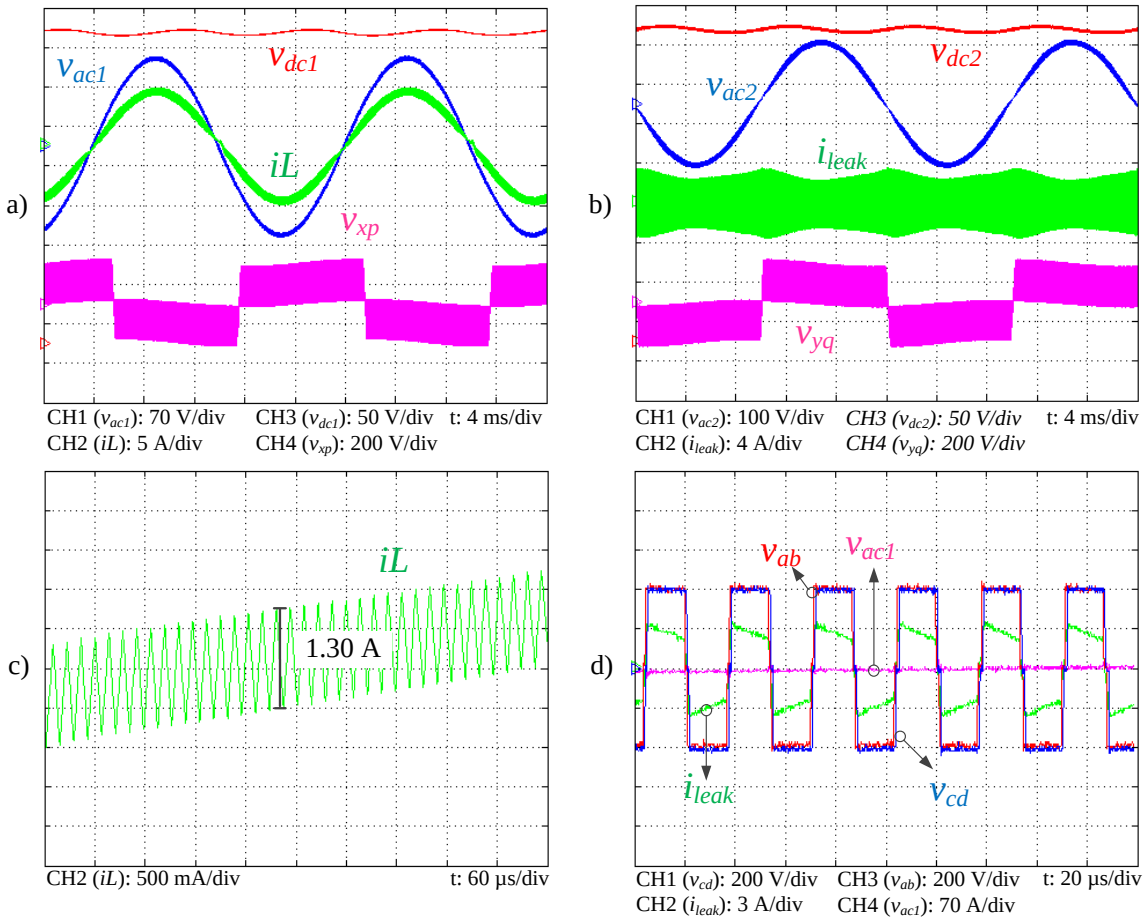
The HERO Power Amplifier (model PFL-2250-28-UDC415-IDC375) was used as a voltage source combined with a function generator (DS345 – Stanford Research Systems). To measure the efficiency the Norma D Wideband Power Analyser D6000 (LEM) was used. The results were collected with two Tektronix oscilloscopes DPO7104 and DPO5104.

3.7.2 Results of the Symmetric Half-bridge

This converter was tested with SCT3120AL switches only. Figure 22a shows the primary side variables at nominal power (0.5 kW). The converter input voltage v_{xp} has three levels as mentioned before. The grid voltage and the input current are in phase with 0.996 power factor. The DC-link voltage v_{dc1} is controlled in 400V. Figure 22c shows the maximal input current ripple of 1.30A. The calculated THD of the input current was 6.89%. Figure 22b presents the secondary side variables at nominal power. The DC-link voltage is controlled in 400V. The load voltage v_{ac2} is sinusoidal with a THD of 4.07%. Figure 22d presents in detail the transformer windings voltages v_{ab} and v_{cd} as well as the transformer current i_{leak}. The duty cycle at this time instant is approximately 0.5.

Figure 23 shows the converter dynamic response in two scenarios: the load step from 0.5 p.u. to 1.0 p.u. (at time instant t_0) and return to 0.5 p.u. (at time instant t_1); voltage sag to 0.7 p.u. (at time instant t_0) and return to 1.0 p.u. (at time instant t_1). Figure 23a presents the load step response of the primary side variables. The perturbation of the DC-link voltage v_{dc1} is

Figure 22 – Experimental results at nominal power: a) converter primary side variables; b) secondary side variables; c) input current ripple; d) transformer variables.



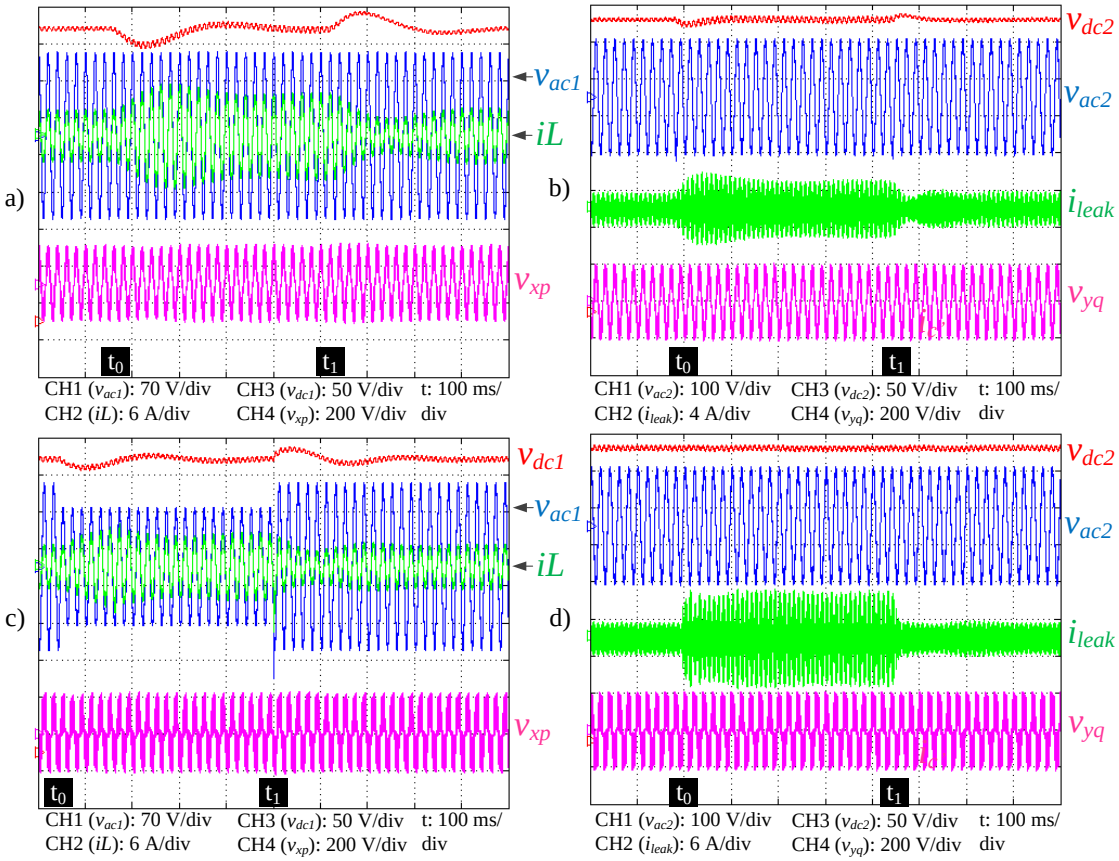
Source: Author.

controlled within ~300 ms. Notice the increase of the input current in response to the load increase. Figure 23b shows the variables of the converter secondary side. The load increase causes the increase of the transformer current. The perturbation is also noticed in the secondary DC-link v_{dc2}, but at a reduced extent. Notice that the load voltage v_{ac2} is unaffected by the load step.

Figure 23c shows the primary side variables during a voltage sag to 0.7 p.u[2]. Notice the grid voltage drop at time instant t_0. This perturbation affects the DC-link, which is controlled in less than 300 ms. The input current increases to compensate the power reduction due to the voltage sag. The grid voltage returns to 1.0 p.u. at time instant t_1. The generated perturbation on the DC-link is again controlled within 300 ms. Figure 23d shows the secondary side variables

[2] Due to current limit imposed by the voltage source, this test was performed with reduced power (400W).

Figure 23 – Experimental results: a) and b) input/output variables; c) input current ripple; d) transformer variables; e) and f) step response (0.5 p.u. - 1.0 p.u) of the input/output; g) and h) grid voltage sag response of the input/output to 0.7 p.u.

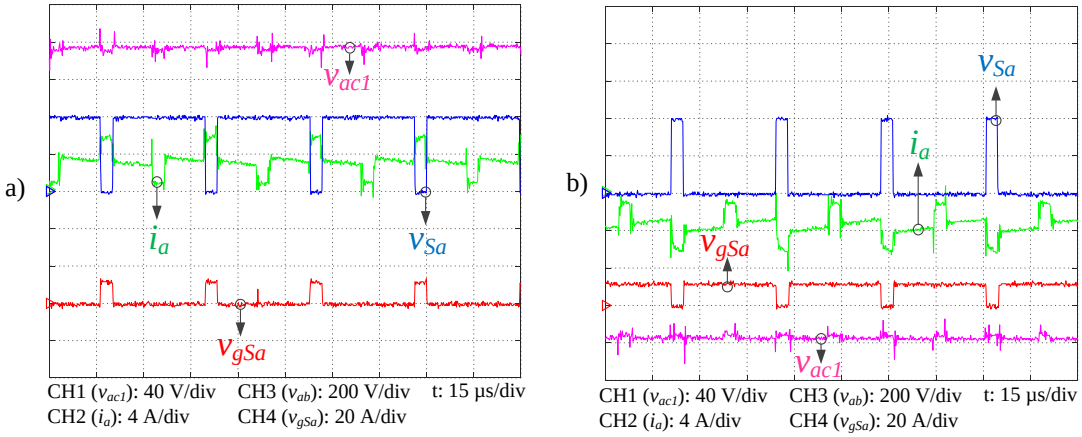


Source: Author.

during the voltage sag. One notices the increase of the transformer current. During the sag, the modulation index applied to the primary side reduces from 0.775 to 0.543, while in the secondary side it remains unchanged. The modulation index change affects the duty cycle function d_{ab}, which becomes different from the one applied to the secondary side (d_{cd}) increasing the transformer current. Notice that as the load remains unchanged, the current increase is completely reactive.

Figure 24 shows the converter in two operating points from which one observes the switching behavior of S_a. The grid voltage (v_{ac1}), the switch voltage and gate signal and the node ‘a’ current are presented. Figure 24a shows the switch S_a operating outside the ZVS region with a positive grid voltage. Figure 24b shows the same variables for a negative grid voltage. In this case, the switch S_a operates inside the ZVS region.

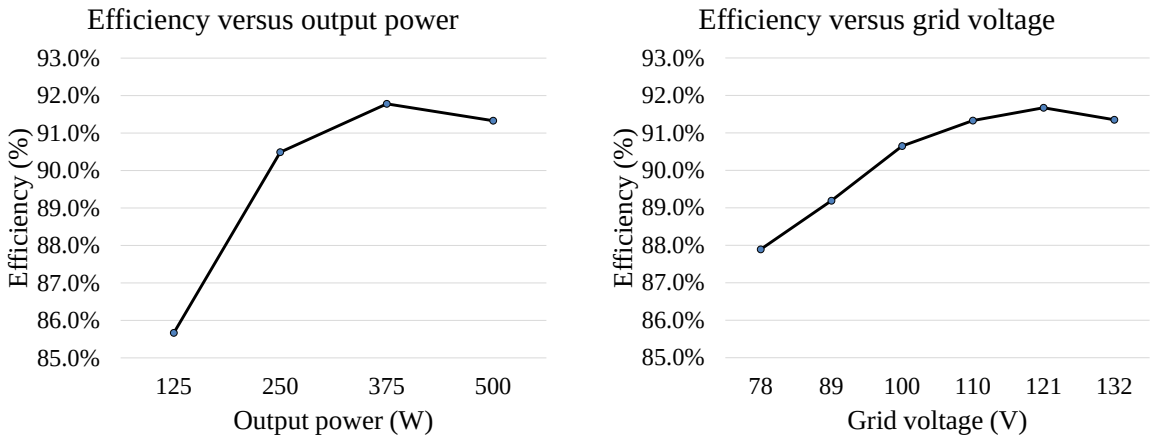
Figure 24 – Switching characteristics of S_a: a) converter operating outside the ZVS region; b) converter operating inside the ZVS region.



Source: Author.

Figure 25 shows the obtained efficiencies. Figure 25a shows the efficiency changing with the load. The peak efficiency value, 91.73%, is achieved under 375W load. The efficiency profile with the grid voltage is presented in Figure 25b.

Figure 25 – Efficiency results: a) efficiency with changing output power; b) efficiency changing grid voltage.



Source: Author.

4 SYMMETRIC FULL-BRIDGE CONVERTER

This Chapter describes the operation of the Symmetric Full-bridge converter. The power flow equations are derived from the new duty cycle function used by this converter. The adopted modulation is presented and operates the additional legs at low frequency. The input current ripple is determined. In addition, a ZVS analysis is performed and the converter losses are estimated. The experimental results for nominal power are presented together with the converter dynamic response to a load step and a voltage sag.

4.1 Converter operation

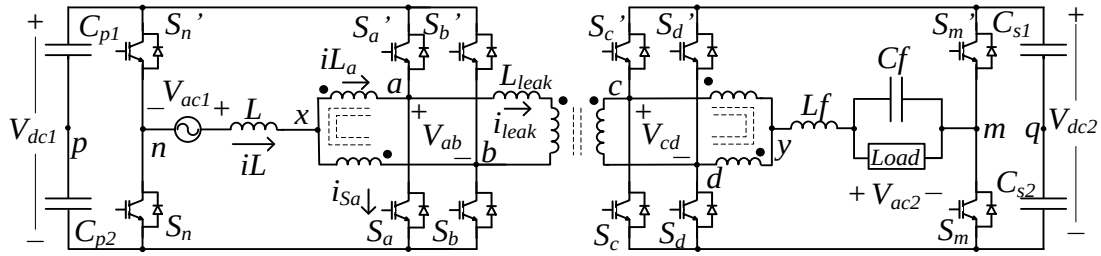
The Symmetric Full-bridge topology is presented in Figure 26. The primary and secondary sides of the converter are composed each by Full-bridge arrangements. The difference between this converter and the Symmetric Half-bridge is the addition of two new legs composed by switches S_n, S_n', S_m' and S_m. The transformer's windings voltages v_{ab} and v_{cd} are defined in the same way as the SHB, i.e., they are independent of the states of the introduced switches. However, the converter input voltage v_{xn} is defined by the switches S_a, S_b and S_n, as well as the converter output voltage (v_{ym}) is defined by the switches S_c, S_d and S_m. Table 2 shows both converter sides switching states.

Table 12 –SFB converter voltages.

Switching state			**Voltages**	
Sn/Sm	***Sa/Sc***	***Sb/Sd***	v_{ab} | v_{cd}	v_{xn} | v_{ym}
0	0	0	0	0
0	0	1	V_{dc1} | V_{dc2}	$-V_{dc1}/2$ | $-V_{dc2}/2$
0	1	0	$-V_{dc1}$ | $-V_{dc2}$	$-V_{dc1}/2$ | $-V_{dc2}/2$
0	1	1	0	$-V_{dc1}$ | $-V_{dc2}$
1	0	0	0	V_{dc1} | V_{dc2}
1	0	1	V_{dc1} | V_{dc2}	$V_{dc1}/2$ | $V_{dc2}/2$
1	1	0	$-V_{dc1}$ | $-V_{dc2}$	$V_{dc1}/2$ | $V_{dc2}/2$
1	1	1	0	0

Source: Author.

Figure 26 – Symmetric Full-bridge topology.



Source: Author.

Notice that the input/output voltages can assume five different levels including the full DC-link voltage. Looking at the S_n and S_m switching states in Table 2, one notices that when such switches are turned on, the respective input/output voltages are positive, and when they are turned off, the respective voltages are negative. This suggests a low-frequency operation of such switches. However, they can be operated at high frequency as well.

Figure 27 presents a summary of the converter operation stages with the switches S_n and S_m operating at low frequency. Only the positive half cycle of the current is presented for both input and output of the converter, which mean $S_n = S_m = 1$. Figure 28a presents voltages and currents waveforms of the converter. Notice the change of the converter input/output voltage when compared to the SHB. The carriers ‘a’, ‘b’ and ‘c’, and ‘d’ of the primary and secondary sides, respectively, are phase-shifted by φ. Only four time intervals are analyzed since the behavior of the others is similar. The operational stages defined by the time intervals are described below:

- Operation stage 1 [t_0, t_1[(Figure 27Figure 6a): the switches S_b and S_d are turned on, which applies half of the DC-link voltage to the input (v_{xp}) and output (v_{yq}) of the converter. The primary and secondary windings of the transformer are submitted to V_{dc1} and V_{dc2}, respectively. The transformer current remains equal to the initial value.
- Operation stage 2 [t_1, t_2] (Figure 27b): during this stage the switch Sb is turned off, which short circuit the interleaved transformer of the primary side, imposing the voltage V_{dc1} to the input. The transformer primary winding voltage becomes zero and its current start to decrease from its previous value. The converter output voltage remains half of its DC-link.
- Operation stage 3 [t_2, t_3[(Figure 27c): the switch S_d is turned off. Now, the interleaved transformers of both sides are in short. Both input and output voltages

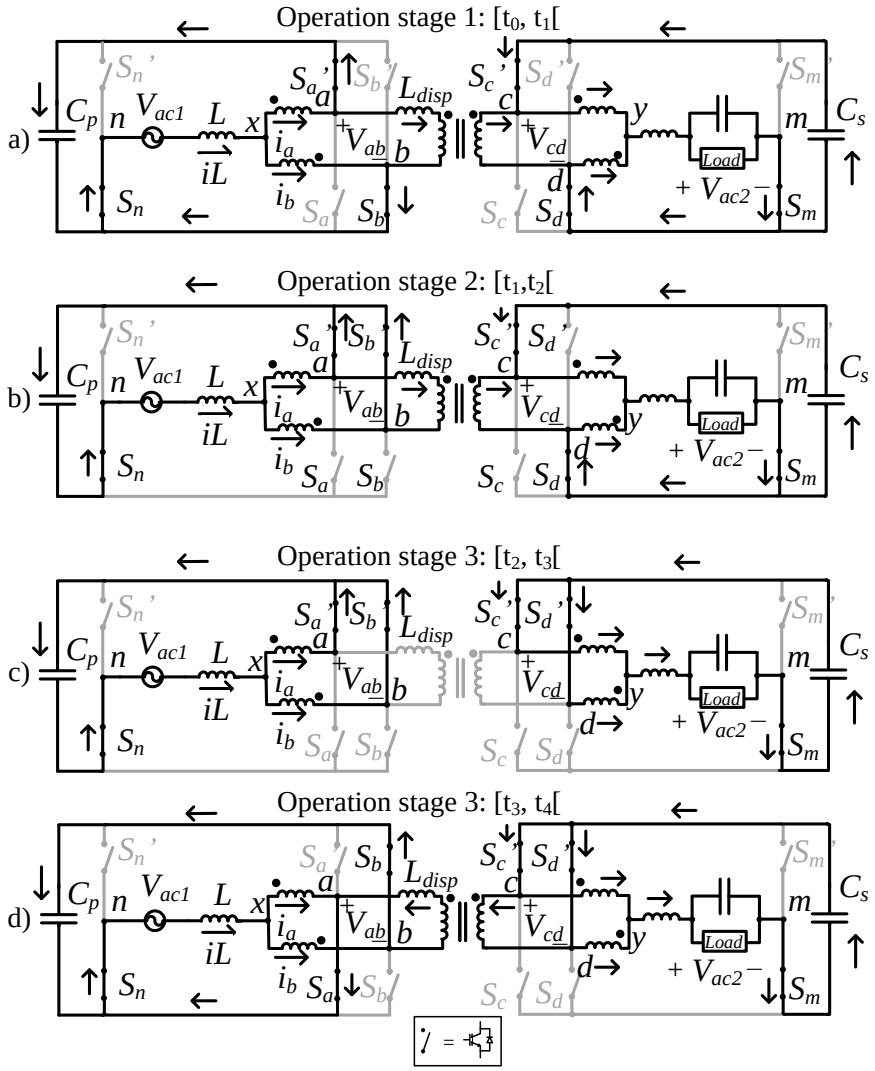
assume their full DC-link voltage. The voltage in both transformer's windings are equal to zero and its current reaches zero.

- Operation stage 4 [t_3, t_4[(Figure 27d): in this stage the switch S_a turns on, which makes the converter input voltage half of its DC-link again. The output voltage remains V_{dc2} and the voltage v_{ab} becomes negative ($-V_{dc1}$) while the voltage v_{cd} remains zero. This increase the transformer current in the opposite direction.

4.2 Modeling input/output of the converter

As the converter works similarly, the converter modeling presented in this section follows the procedures adopted in Section 3.2.

Figure 27 – Symmetric Full-bridge converter operation: a) operation stage 1; b) operation stage 2; c) operation stage 3; d) operation stage 4.



Source: Author.

4.2.1 Duty cycle function

The model presented in Figure 14 also represents the input circuit of this converter. Applying the circuit analysis to Figure 26, the converter input voltage is:

$$v_{xn}(t) = \frac{V_{dc1}}{2}\left(\delta_{Sa'}(t) + \delta_{Sb'}(t) - 2\cdot\delta_{Sn'}(t)\right) \tag{26}$$

The converter input voltage mean value in one switching period and its variation with the time are:

$$\begin{aligned} \overline{v_{xn}} &= \int_0^{Ts} v_{xn}(t)\cdot dt = \frac{V_{dc1}}{2}\left(2\cdot S_n - D_a - D_b\right) \\ \overline{v_{xn}}(t) &= \frac{V_{dc1}}{2}\left(2\cdot s_n(t) - d_a(t) - d_b(t)\right) \end{aligned} \tag{27}$$

Assuming that the duty cycles d_a and d_b are equal and making (27) equal to $\overline{v_{xn}}(t) = V_{xn}\cdot\sin(\omega_g\cdot t+\phi)$, the duty cycle function is obtained.

$$d_{ab}(t) = s_n(t) - M_f\cdot\sin\left(\omega_g\cdot t+\phi\right) \tag{28}$$

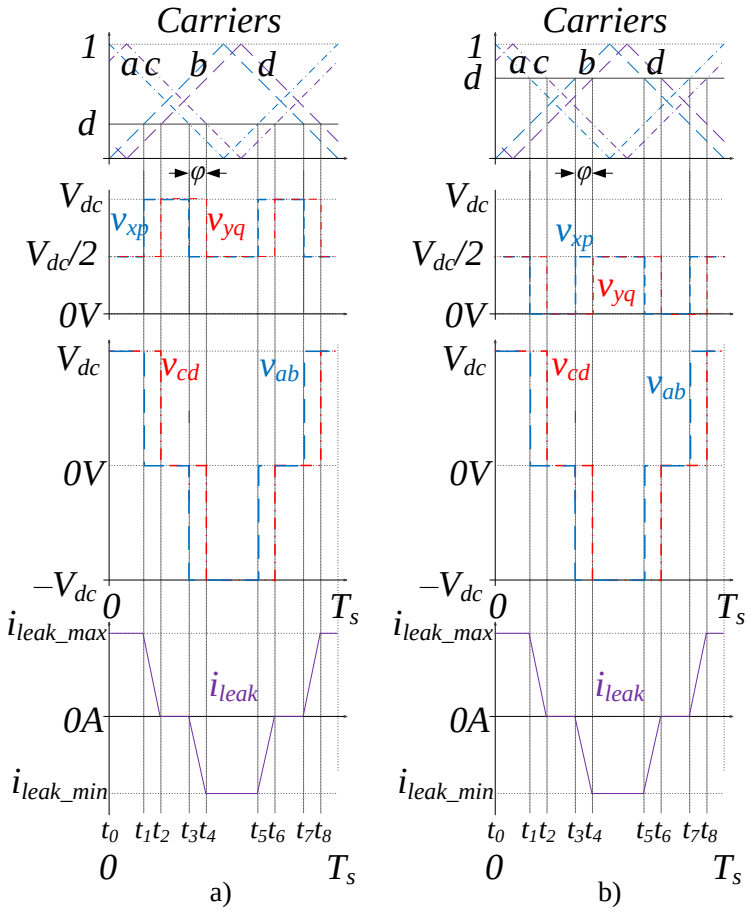
The function $s_n(t)$ is equal to one when the switch is turned on and zero when it is turned off, which means that the resultant duty cycle function is discontinuous.

4.2.2 Modulation

The discontinuous duty cycle function (28) is presented in Figure 29a. Figure 29b shows the voltages v_{xp}, v_{np}, v_{xn} and v_{ab}. The voltage v_{np}, which is defined by the switch S_n alternates between $V_{dc1}/2$ and $-V_{dc1}/2$ every half grid cycle. Notice the five-level of the converter input voltage, v_{xn}. The non-continuous nature of the duty cycle function increases the control effort since the controller would have to output the modulating function of Figure 29a. The controller output becomes sinusoidal if the s_n switch state is fed into the controller output generating the required modulating waveform.

The Figure 28a presents the main converter voltage waveforms for $0 < d_{ab} < 0.5$. Notice the input/output voltages alternate between half and the total DC-link voltage When the duty cycle lies between 0.5 and 1.0 (Figure 28b), the input/output voltage alternates between zero and half of the respective DC-link. In both cases, the input/output converter voltages change two times in one switching period, which enforces current ripple frequency to be twice the switching frequency.

Figure 28 – Modulation of the Symmetric Full-bridge arrangement with key voltages: a) duty cycle smaller than 0.5; b) duty cycle greater than 0.5.



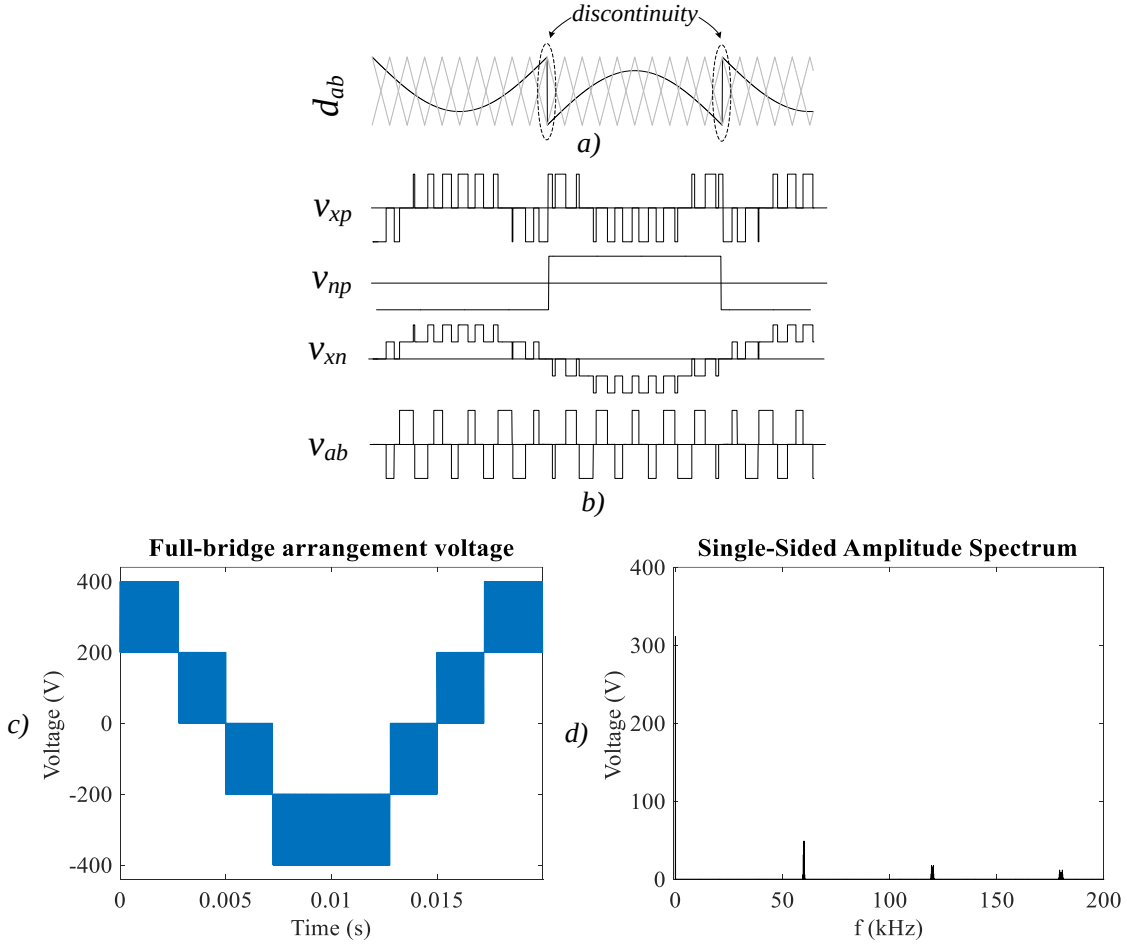
Source: Author.

Figure 29c shows the voltages the Full-bridge arrangement, generated by simulation with the same parameters adopted in the Half-bridge arrangement of the last Chapter, except the DC-link voltage, which is 400V. Notice the increased number of voltage levels when compared to the voltage produced by the Half-bridge arrangement. The spectrum of this voltage is observed in Figure 29d. The harmonics are located at the same positions of the voltage generated by the Half-bridge arrangement (60 kHz, 120 kHz, 180 kHz, …), but with a smaller amplitude. The obtained WTHD is 0.0281.

4.2.3 Current ripple

Considering an ideal interleaved transformer, the input current rate is determined as:

Figure 29 – Modulation of the Symmetric Full-bridge arrangement variating with the grid period: a) carriers and duty cycle function as modulating signal; b) generated voltages; c) generated waveform; d) single-sided amplitude spectrum of the generated voltage.



Source: Author.

$$\frac{diL(t)}{dt} = \frac{v_{ac1}(t) - v_{xn}(t)}{L} \tag{29}$$

One determines ΔiL for the time intervals Δt_1 = [t3, t5] of Figure 28a and Δt_2 = [t1, t3] of Figure 28b.

$$\frac{\Delta iL}{\Delta t_1} = \frac{V_{ac1} - V_{dc1}/2}{L}$$
$$\frac{\Delta iL}{\Delta t_2} = \frac{V_{ac1}}{L} \tag{30}$$

Applying Δt_1 = DTs, Δt_2 = (D- 0.5)Ts and (28) to (30) and considering v_{ac1} = V_{ac1}.sin(ω_g.t), one obtains:

$$\Delta iL = \frac{V_{dc1}}{2 \cdot fs \cdot L}\left(S_n - M_f \cdot \sin(\omega_g \cdot t)\right) \cdot \left(2 \cdot M_f \cdot \sin(\omega_g \cdot t) - 1\right) \tag{31}$$

$$\Delta iL = \frac{V_{dc1}}{2 \cdot fs \cdot L}\left(2 \cdot S_n - 1 - 2 \cdot M_f \cdot \sin(\omega_g \cdot t)\right) \cdot M_f \cdot \sin(\omega_g \cdot \mathrm{t}) \tag{32}$$

Considering the positive cycle and $S_n = 1$, the current ripple is:

$$\Delta iL = \begin{cases} \frac{V_{dc1}}{2 \cdot fs \cdot L}\left(1 - 2 \cdot M_f \cdot \sin(\omega_g \cdot t)\right) \cdot M_f \cdot \sin(\omega_g \cdot \mathrm{t}) & if \quad 0 \le \omega_g \cdot t < \theta 1 \\ \frac{V_{dc1}}{2 \cdot fs \cdot L}\left(1 - M_f \cdot \sin(\omega_g \cdot t)\right) \cdot \left(2 \cdot M_f \cdot \sin(\omega_g \cdot t) - 1\right) & if \quad \theta 1 \le \omega_g \cdot t < \pi - \theta 1 \\ \frac{V_{dc1}}{2 \cdot fs \cdot L}\left(1 - 2 \cdot M_f \cdot \sin(\omega_g \cdot t)\right) \cdot M_f \cdot \sin(\omega_g \cdot \mathrm{t}) & if \quad \pi - \theta 1 \le \omega_g \cdot t < \pi \end{cases} \tag{33}$$

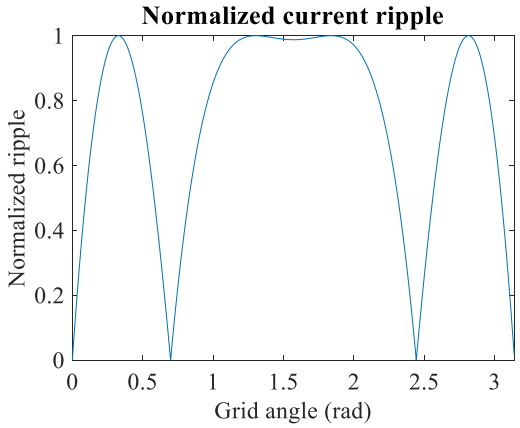
Where $\theta 1 = \sin^{-1}\left(1/(2 \cdot M_f)\right)$.

The maximal current ripple is:

$$\Delta iL \underset{\omega_g \cdot t = \theta_{\max}}{\le} \frac{V_{dc1}}{16 \cdot fs \cdot L} \tag{34}$$

Where $\theta_{\max} = \sin^{-1}\left(\frac{1}{4 \cdot M_f}\right)$ inside the interval $0 \le \omega_g t < \theta 1$. Figure 30 shows the variation of (33) per unit.

Figure 30 – Per unit current ripple variation with the grid.



Source: Author.

4.3 Transformer power flow analysis

The transformer is modeled following the same procedures found in Section 3.3. The duty cycle function applied in this converter differs from the one applied to the SHB, which modifies the transformer power flow. The following analysis considers the same duty cycle

function applied to the primary and secondary side of the converter. The model presented in Figure 17 is valid. Applying (28) to (22) one obtains the mean power varying with time.

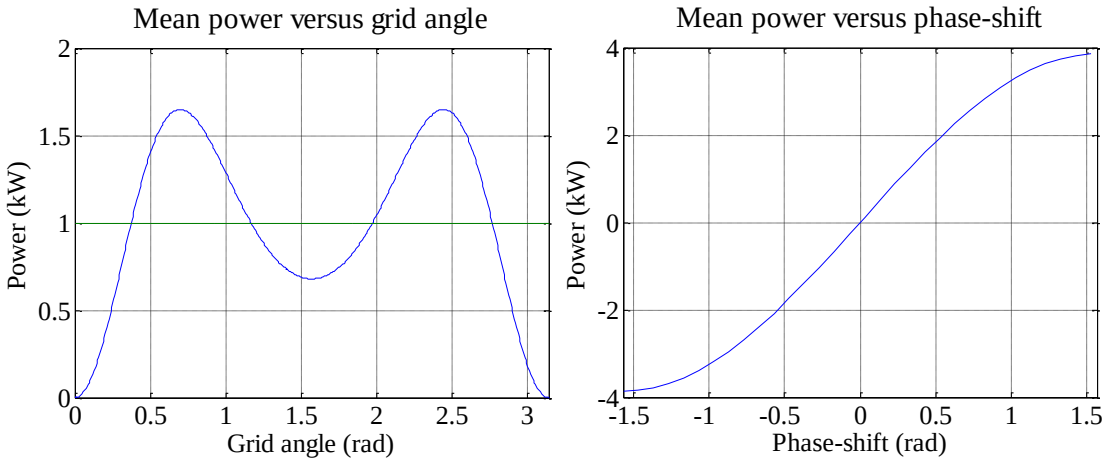
$$P_{fb}\left(\omega_g \cdot t, \varphi\right) = \frac{8 \cdot N \cdot V_{dc1} \cdot V_{dc2} \cdot \sin(\varphi)}{\pi^2 \cdot L_{leak} \cdot \omega_s}\left(\cos^2(\pi \cdot M_f \cdot \sin(\omega_g \cdot t)) - 1\right) \tag{35}$$

The mean power transferred in one grid period is given by:

$$P_{mean\_fb}\left(\varphi\right) = \frac{1}{\pi}\int_0^{\pi} P_{fb}\left(\omega_g \cdot t, \varphi\right) d\omega_g t \tag{36}$$

Figure 18 presents the power flow variation with the grid phase and with the phase-shift. Figure 18a is determined using (35) for φ = 0.26 (15º) while Figure 18b is determined using (25).

Figure 31 – Example of power flow variation for the Symmetric full-bridge converter with V_{dc1} = V_{dc2} = 400V, fs = 30 kHz, M_f = 0.778 and L_{leak} = 108 µH, for 1000W mean power: a) according to the grid voltage θ for φ = 0.26 (15º) showing the mean value in one grid period (straight line); b) according to the phase-shift.



a) b)

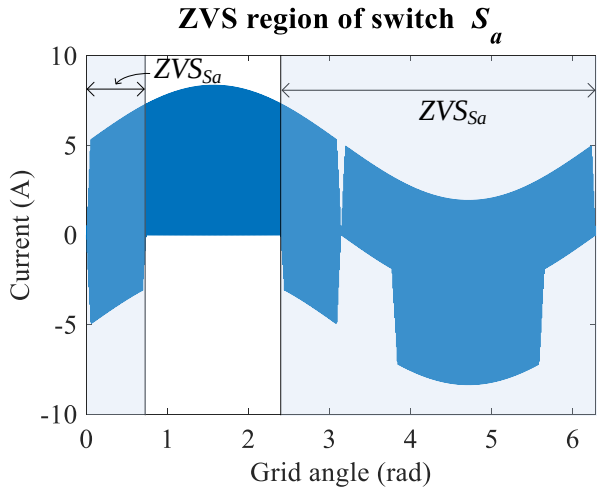
Source: Author.

4.4 ZVS analysis

Following the analysis performed in the previous Chapter, the ZVS region of the SFB converter can be determined considering the current that enters node ‘a’ (given by $i_a = iL_a - i_{leak}$) (Figure 26) and the gate signal (g_a). The current in the interleaved transformer

winding iL_a is considered sinusoidal and equal to half of the converter input current. In addition, the duty cycle functions applied to both transformer's windings are considered equal, i.e, $d_{ab} = d_{cd}$. The current that flows through the switch S_a, given by $i_{Sa} = g_a \cdot i_a$, is presented in Figure 32. The ZVS region is also presented and it is equal to 4.62 rad (265º), being longer than the obtained with the SHB converter. The ZVS regions of the other switches are similar.

Figure 32 – Current and ZVS region of switch S_a. of the SFB.



Source: Author.

4.5 Losses estimation

The losses estimation are very similar to the one performed to the SHB converter since the same magnetic devices are used. There are differences though, regarding the switches and the electrolytic capacitors.

4.5.1 Conduction and switching losses determination

In Figure 26, the switches S_n, S_m and their complementary work at low frequency. For these switches, the conduction losses are responsible for the majority of the losses and a switch with a smaller $R_{DS(on)}$ can be used. The switch SCT3030AL was applied. It presents a $R_{DS(on)}$ of 30 mΩ, with 650V blocking voltage and 70A of continuous drain current. Table 13 presents the conduction and switching losses obtained with the simulation software PLECS® and datasheet information.

Table 13 – Losses of the SFB converter with SCT3120AL and SCT3030AL switches.

Losses	**Value**
Conduction losses	19.35 W
Switching losses	10.49 W
Total losses	**29.84 W**

Source: Author.

4.5.2 Magnetic devices losses

The estimated losses of the inductors and interleaved transformers are quite similar to the one calculated for the SHB. The estimated losses of the transformer are higher due to the increased current needed to flow 1 kW from the primary to the secondary side. Table 14 presents a summary of the magnetic devices losses.

Table 14 – Magnetic devices losses.

Device	**Losses value**
Input/output inductor	3.47 W / 3.47 W
Input/output interleaved transformer	4.23 W / 4.23 W
Transformer	5.29 W
Total	**18.60 W**

Source: Author.

4.5.3 Electrolytic capacitor losses

The same capacitor number and layout of the SHB converter is used here. However, the central connection of the DC-link is not used, which reduces the low-frequency current circulating in the DC bank. Table 10 shows the currents with their frequency as well as the estimated ESR value. Notice there is no 50Hz component circulating in the DC-link. The estimated power loss for the whole converter is 2.4W.

Table 15 – Current values for the SFB converter and the estimated ESR values for the ELH687M450AT8 capacitor.

Capacitor	**RMS current value**	**Estimated ESR value**
Series associated capacitor	0.66 A @ 100 Hz	0.351 Ω
	0.42 A @ 200 Hz	0.234 Ω
	0.18 A @ 300 Hz	0.156 Ω
	0.75 A @ 60 kHz	0.012 Ω
Parallel associated capacitor	1.35 A @ 100 Hz	0.351 Ω

	0.86 A @ 200 Hz	0.234 Ω
	0.36 A @ 300 Hz	0.156 Ω
	1.51 A @ 60 kHz	0.012 Ω

Source: Author.

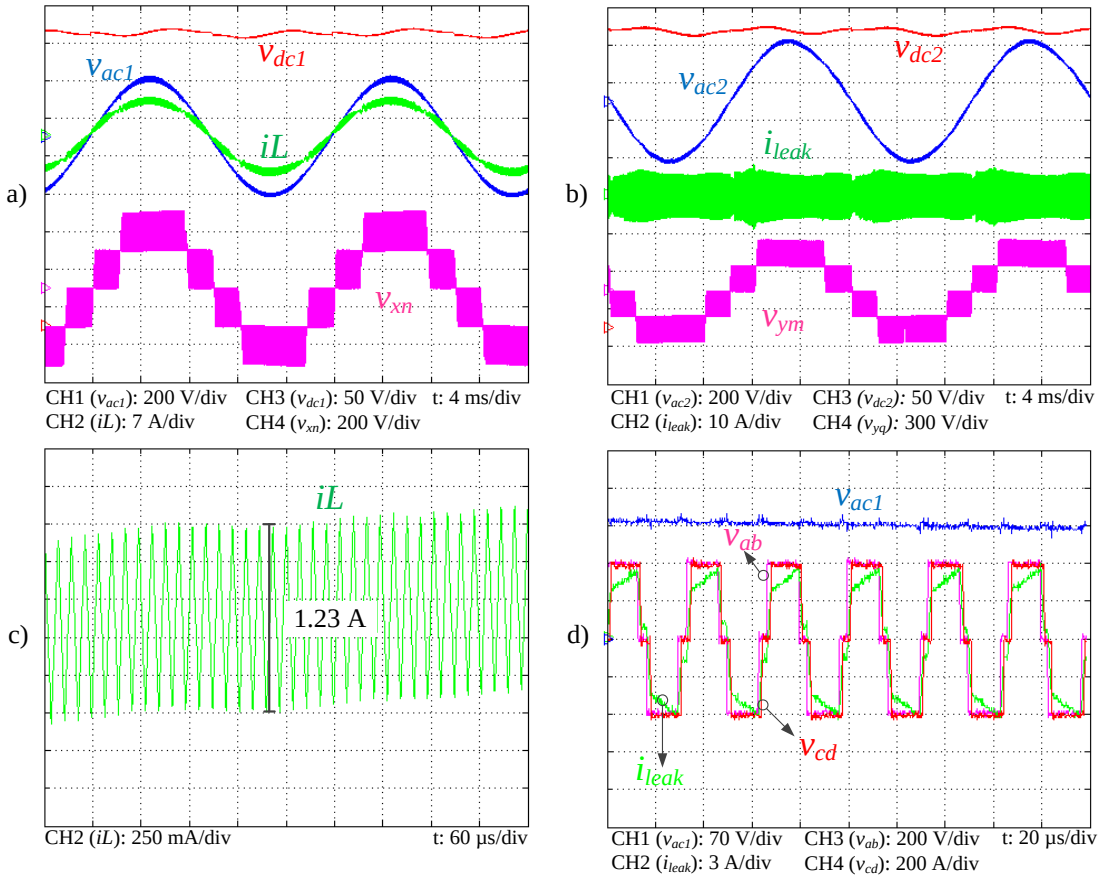
4.6 Experimental results

Figure 33 presents the SFB converter operating at nominal power (1 kW). Figure 33a presents the grid voltage and the input current in phase with PF = 0.995.

The input current *iL* presented a THD of 7.70%. The converter input voltage (v_{xn}) can be observed with its five levels. The DC-link voltage is controlled in 400V. A maximal input current ripple of 1.23 A is determined from Figure 33c.

Figure 33b shows the secondary side variables, which includes the output voltage of the converter, v_{ym}. The load voltage (v_{ac2}) is sinusoidal, controlled in 220V and has THD of

Figure 33 – Experimental results at nominal power: a) converter primary side variables; b) secondary side variables; c) input current ripple; d) transformer variables.



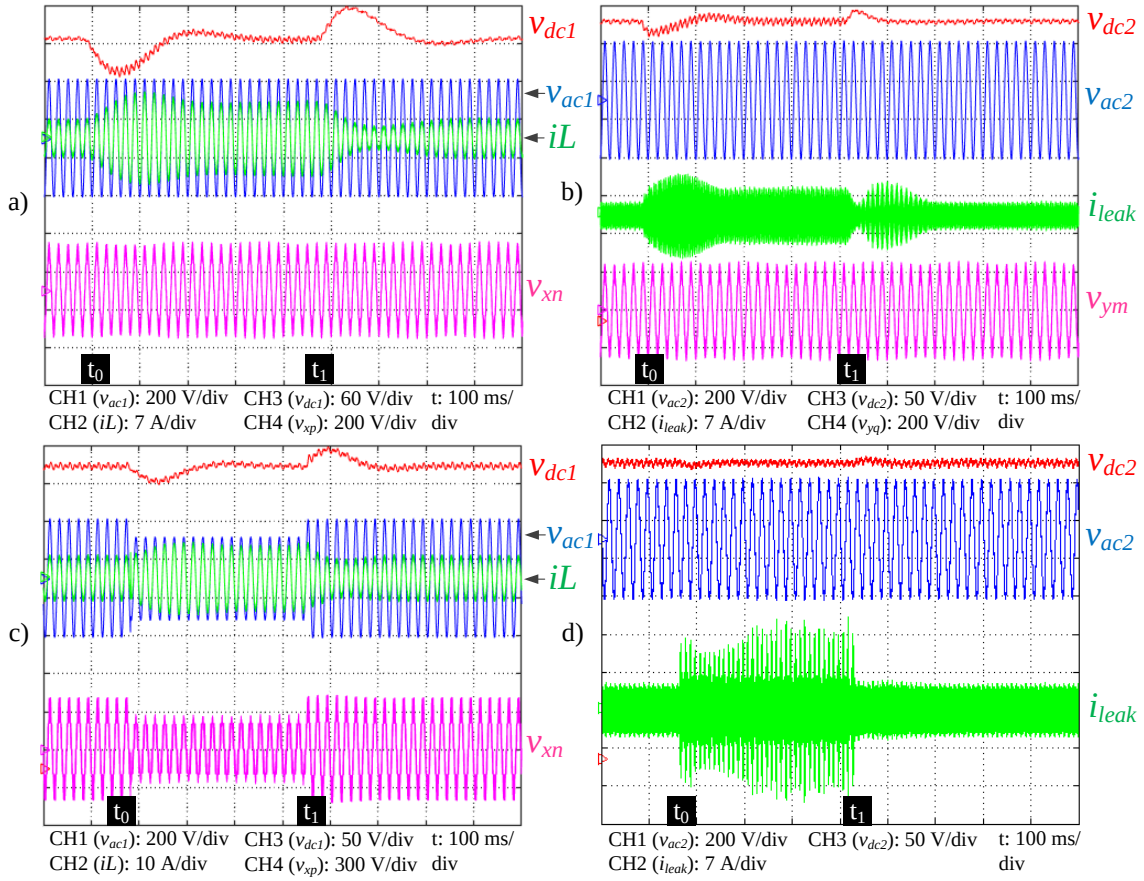
Source: Author.

2.94%. The DC-link voltage is also controlled in 400V. The transformer current is also presented. Figure 22d shows in details the transformer voltages and current with a duty cycle near 0.5. Notice the small phase-shift between the primary winding voltage and the secondary winding voltage.

Figure 34 presents the converter dynamic response to load step and voltage sag. Figure 34a shows the primary side variables when a load step from 0.5 p.u to 1.0 p.u. occurs at t_0 and returns to 0.5 p.u. at t_1.

Notice the input current increase and the DC-link voltage perturbation, which is controlled within 300 ms. In the secondary side (Figure 34b), one observes the natural increase of the transformer current due to the load increase. The DC-link voltage is also disturbed, but it is controlled in ~200 ms. Notice that the load voltage (v_{ac2}) is immune to the perturbation.

Figure 34 – Experimental results (dynamic response): a) and b) primary and secondary sides variables, respectively, during a step response (0.5 p.u. - 1.0 p.u); c) and d) primary and secondary sides variables, respectively, during a voltage sag to 0.7 p.u.

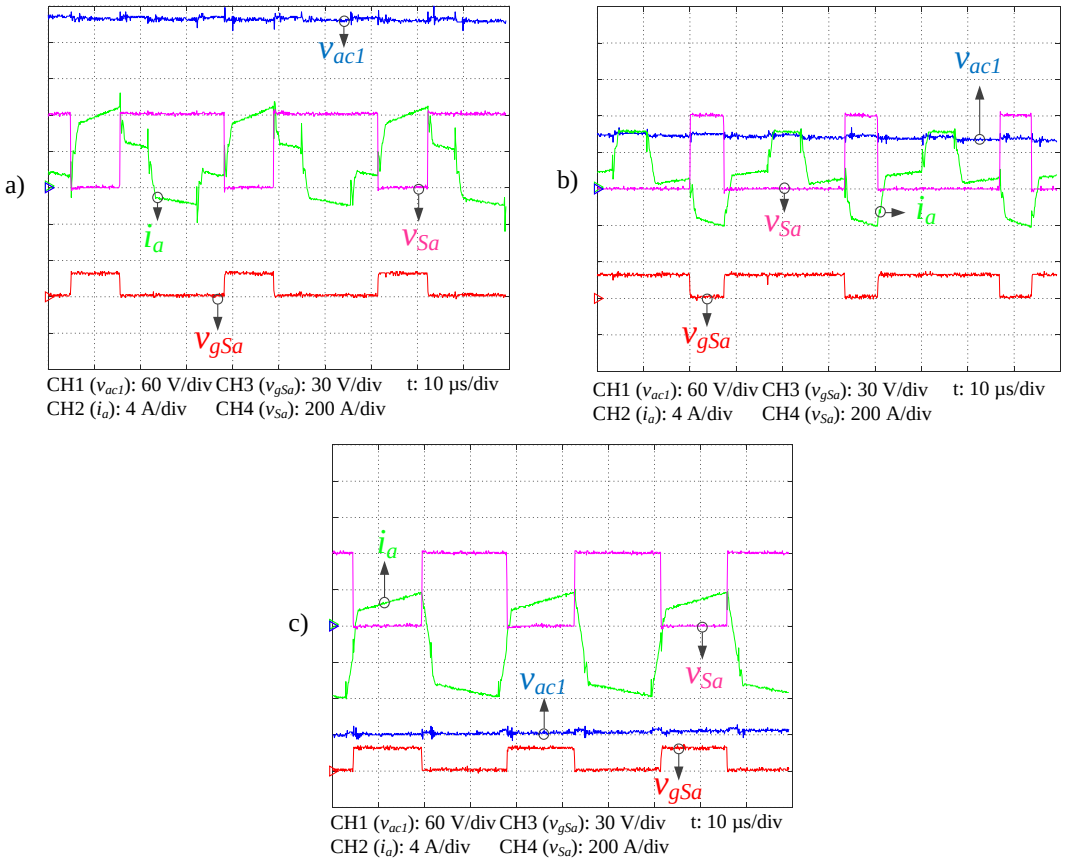


Source: Author.

Figure 34c shows the primary side variables response to a voltage sag to 0.7 p.u. occurring at t_0 and removed at t_1. Notice the grid voltage decrease during the sag as well as the converter voltage (v_{xn}). The input current increases in response to the reduced grid voltage. The perturbation on the DC-link voltage is quickly recovered. Figure 34d shows the secondary side variables during the sag. There is no disturbance on the load voltage (v_{ac2}) and a small perturbation of the DC-link is observed. Notice the increase of the transformer current caused by the increased difference between the duty cycle applied to the primary side of the transformer and the duty cycle applied to the secondary side. Figure 35 presents the switching characteristic of S_a in three different time instants.

Figure 35a shows the switch voltage, gate signal and node current for a positive grid voltage. Notice that when the switch is turned on, the node current is positive, which means 'hard' switch. In this region, the switch operates outside the ZVS region. In Figure 35b, the grid voltage is still positive but during the turn on the current in the switch is negative, which mean

Figure 35 – Switching characteristics of S_a: a) converter operating outside the ZVS region; b) and c) converter operating inside the ZVS region.

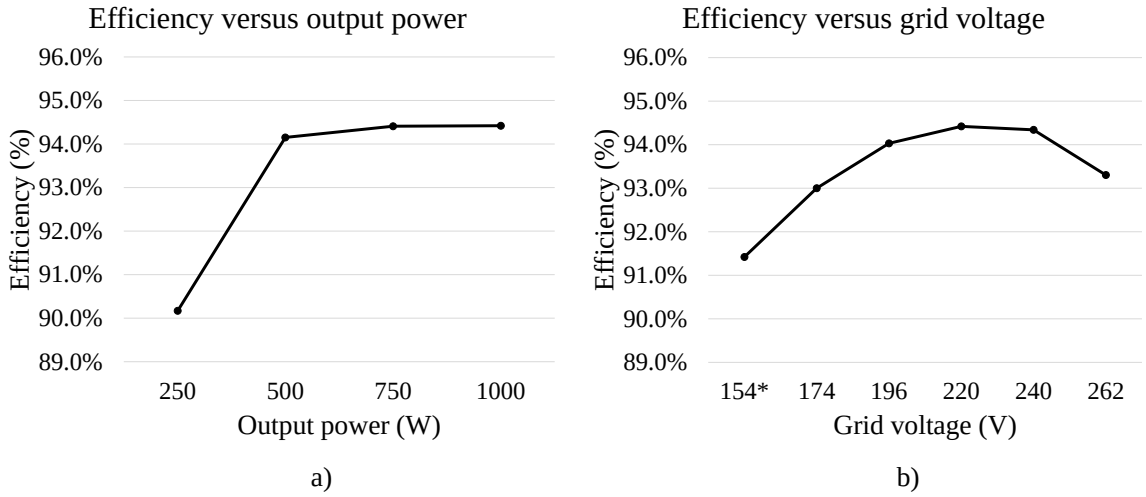


Source: Author.

it flows through the diodes enabling ZVS. In Figure 35c, the voltage is negative and the switch operates inside the ZVS region.

Figure 36 presents the obtained efficiencies for different load levels and different grid voltage values. Figure 36a shows that the efficiency increase with the load reaching its peak value (94.42%) at 1 kW. Figure 36b[3] shows that the converter reaches the highest efficiency at nominal voltage.

Figure 36 – Efficiency results: a) efficiency with changing output power; b) efficiency changing grid voltage.



a) b)

Source: Author.

[3] At 154V the converter had to be derated to 850W because the input current demand reached the voltage source current limit.

5 SYMMETRIC INTERLEAVED FULL-BRIDGE CONVERTER

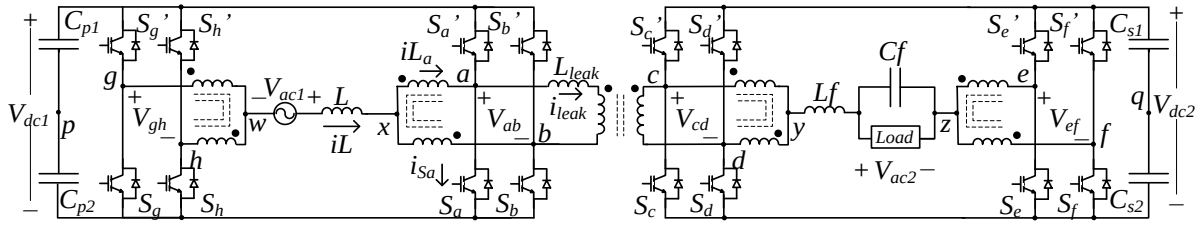
This Chapter presents the Symmetric Interleaved Full-bridge converter. This converter presents several advantages from the converter presented previously as a higher effective switching frequency in the converter input/output, no grid frequency current component through the DC-link, smaller requirements of inductances and filter. However, such advantages come at the expense of the highest number of switches and magnetic devices between all converters of the proposed family.

This Chapter presents the converter operation, input/output current ripple determination, the transformer power flow equations, and a ZVS analysis. In addition, this the concept of actuator types is introduced, which enables the transformer current reduction through the use of the same duty cycle function in both transformer windings. The experimental results are presented showing the converter dynamic response to a voltage sag and a load step.

5.1 Converter operation

The Interleaved Full-bridge converter is presented in Figure 37. Both primary and secondary sides are composed by Interleaved Full-bridge arrangements, being classified as a Symmetric Interleaved Full-bridge converter (SIFB). When one compares this converter to the SFB, the bridge-legs ‘m’ and ‘n’ are replaced by Interleaved Full-bridge arrangements, creating the connection points ‘w’ and ‘z’ with the source and load, respectively. The input/output voltage levels are the same but the effective frequency is double. A list of switching states of both sides of the converter is given in Table 16.

Figure 37 – Symmetric Interleaved Full-bridge topology.



Source: Author.

Table 16 – Switching states of the Symmetric Interleaved Full-bridge converter side and the respective voltages V_{ab}, V_{cd}, V_{xw} e V_{yz}.

Switching states				**Voltages**	
Sg/Se	***Sh/Sf***	***Sa/Sc***	***Sb/Sd***	V_{ab} | V_{cd}	V_{xw} | V_{yz}
0	0	0	0	0	0
0	1	0	1	V_{dc1} | V_{dc2}	
0	1	1	0	V_{dc1} | V_{dc2}	
1	0	0	1	$-V_{dc1}$ | $-V_{dc2}$	
1	0	1	0	$-V_{dc1}$ | $-V_{dc2}$	
1	1	1	1	0	
0	0	0	1	0	$V_{dc1}/2$ | $V_{dc2}/2$
0	0	1	0	0	
0	1	1	1	V_{dc1} | V_{dc2}	
1	0	1	1	$-V_{dc1}$ | $-V_{dc2}$	
0	1	0	0	V_{dc1} | V_{dc2}	$-V_{dc1}/2$ | $-V_{dc2}/2$
1	0	0	0	$-V_{dc1}$ | $-V_{dc2}$	
1	1	0	1	0	
1	1	1	0	0	
0	0	1	1	0	V_{dc1} | V_{dc2}
1	1	0	0	0	$-V_{dc1}$ | $-V_{dc2}$

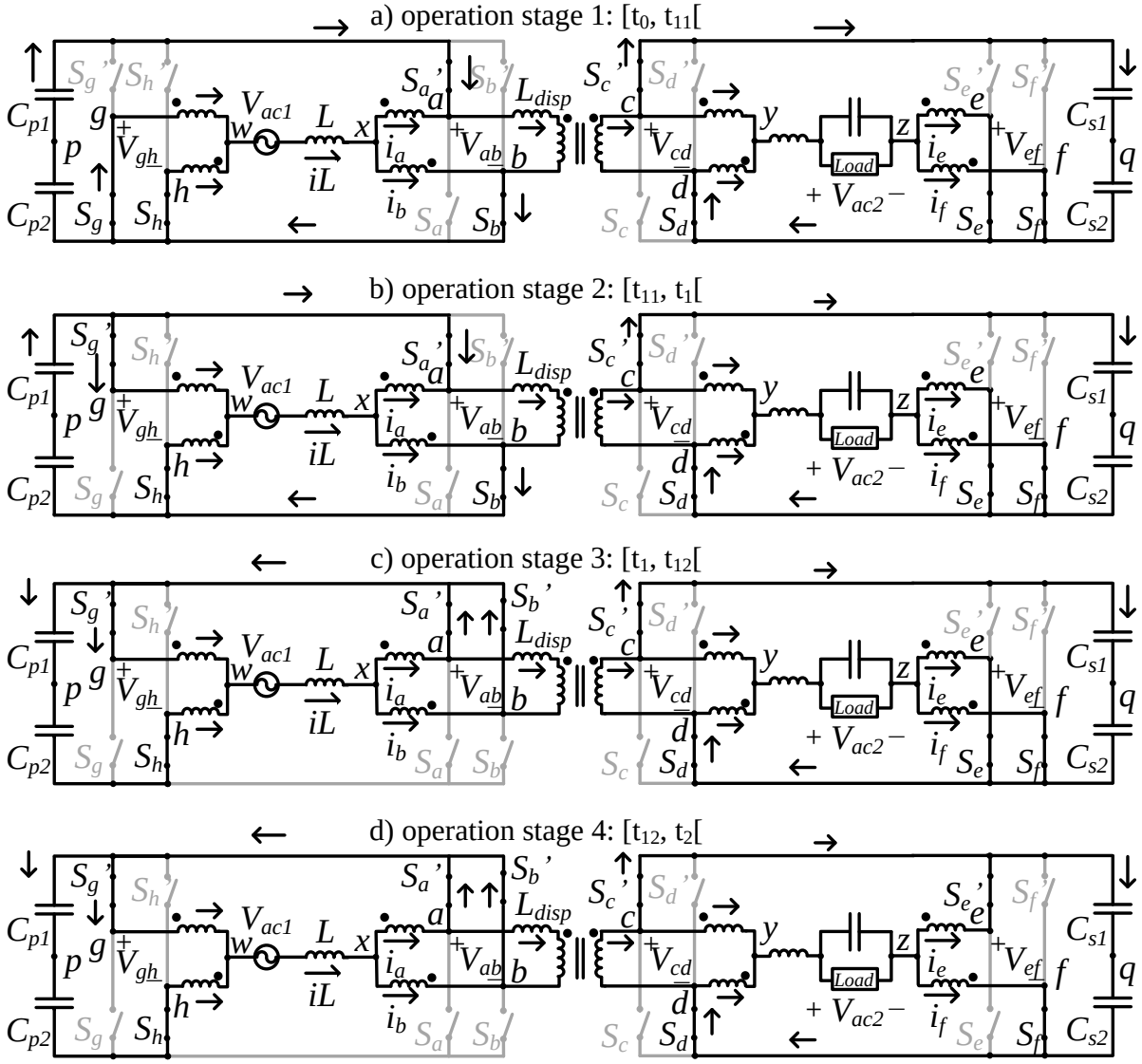
Source: Author.

Given the switching states, one determines sixteen different operation stages for this converter. Figure 38 and Figure 39 present only eight operation stages, since the others are similar. Figure 40a shows the time intervals divisions that define each operating stage, as well as the involved carriers and duty cycle functions. Four news carriers are introduced: ‘e’, ‘f’, ‘g’ and ‘h’. Each new carrier is responsible for the associated switch signal. The operating stages are described below:

- Operating stage 1 [t_0, t_{11}[(Figure 38a): at this point, it is considered that positive current circulates through the transformer. In the primary side, the switches S_b, S_g, and S_h are turned on, while in the secondary side the switches S_d, S_e, and S_f are on. The respective DC-link voltage is applied to the primary and secondary sides of the transformer. The converter’s input and output voltage are half their DC-link voltage,

- Operating stage 2 [t_{11}, t_1[(Figure 38b): the switch S_g is turned off in this stage. This turns the input voltage zero. The transformer's variables do not change.
- Operating stage 3 [t_1, t_{12}[((Figure 38c): the switch S_b is turned off, which applied zero voltage to the primary winding of the transformer. This decreases the transformer current. The converter input voltage is again half of its DC-link voltage.

Figure 38 – Interleaved Symmetric Full-bridge converter operation: a) operation stage 1; b) operation stage 2; c) operation stage 3; d) operation stage 4.



Source: Author.

- Operating stage 4 [t_{12}, t_2[(Figure 38d): the switch S_e is turned off, which applies zero voltage to the converter's output. The transformer's variables remain unchanged.
- Operating stage 5 [t_2, t_3[(Figure 39a): the switch S_d is turned off and the transformer secondary voltage is zero. The transformer current reaches zero and the converter output voltage is half of its DC-link.
- Operating stage 6 [t_3, t_{34}[(Figure 39b): at this stage the switch S_a is turned on. The transformer primary voltage is negative ($-V_{dc1}$) and the current becomes negative. The converter input voltage becomes zero.
- Operating stage 7 [t_{34}, t_4[(Figure 39c): during this stage, the switch S_g is turned on and the converter input voltage returns to half of the DC-link. Notice that the transformer current is negative.
- Operating stage 8 [t_4, t_{45}[(Figure 39d): the switch S_c is turned on, which set $-V_{dc2}$ as the transformer secondary voltage. As there is no voltage applied to the leakage inductance, the transformer current remains unchanged. The converter output voltage is set to zero.

5.2 Converter modelling

As the converter works similarly, the converter modeling presented in this section follows the procedures adopted in Section 3.2.

5.2.1 Duty cycle function

The model presented in Figure 14 also represents the input circuit of this converter. Applying the circuit analysis to Figure 26, the converter input voltage is:

$$v_{xw}(t) = \frac{V_{dc1}}{2}\left(\delta_{Sa'}(t) + \delta_{Sb'}(t) + \delta_{Sg'}(t) + \delta_{Sh'}(t)\right) \tag{37}$$

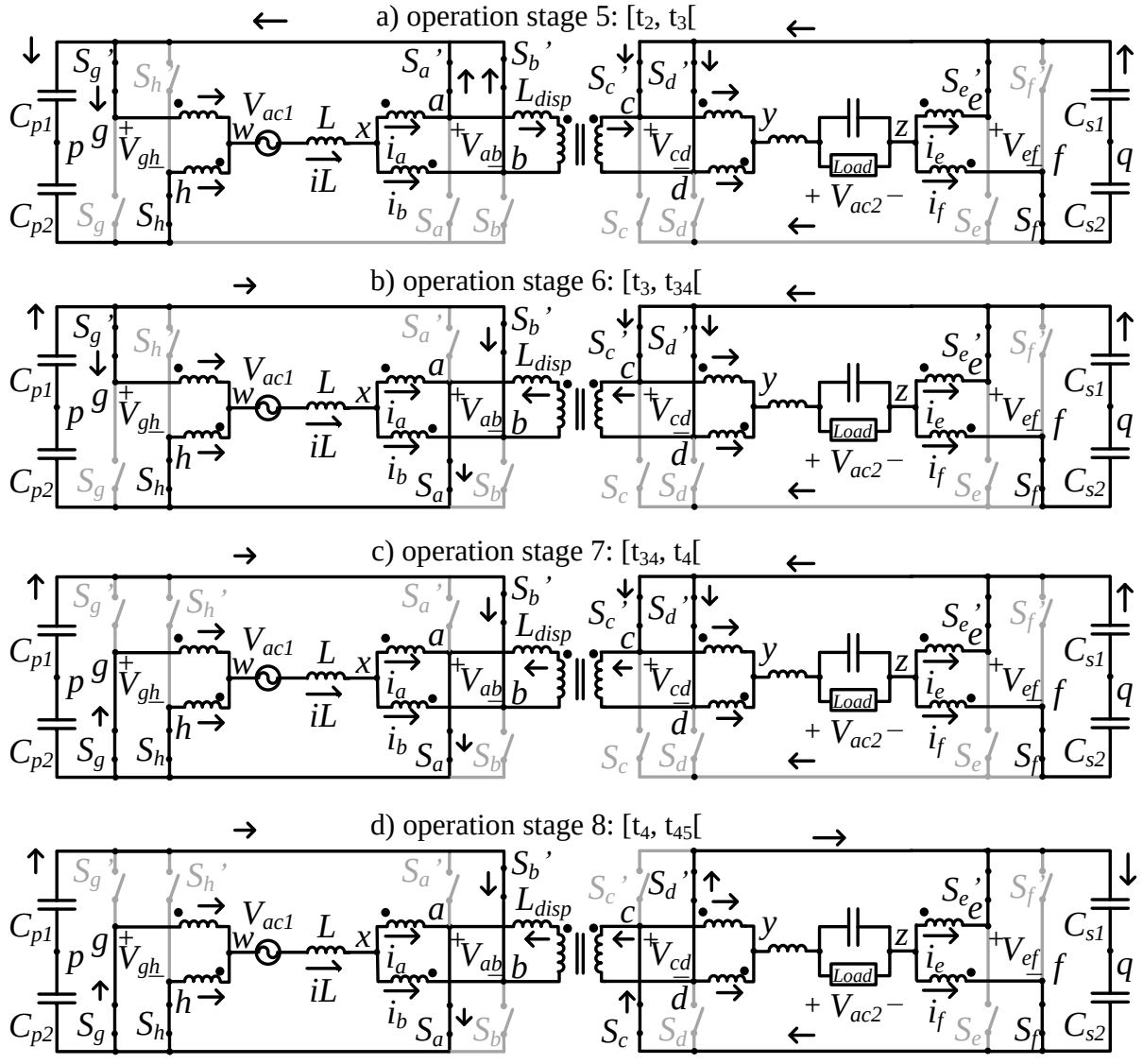
It is considered that $d_a(t) = d_b(t) = d_{ab}(t)$e $d_g(t) = d_h(t) = d_{gh}(t)$. Thus, the mean value is and its variation with time are give:

$$\overline{v_{xw}} = \int_0^{Ts} v_{xw}(t)\cdot dt = \frac{V_{dc1}}{2}\left(D_{gh} - D_{ab}\right)$$
$$\overline{v_{xw}}(t) = V_{dc1}\left(d_{gh}(t) - d_{ab}(t)\right) \quad (38)$$

Making the time-varying medium value found in (38) equal to $\overline{v_{xw}}(t) = V_{xw}\cdot\sin(\omega_g \cdot t + \phi)$, the duty cycle function is obtained.

$$d_{gh}(t) - d_{ab}(t) = M_f \cdot \sin\left(\omega_g \cdot t + \phi\right) \quad (39)$$

Figure 39 – Interleaved Symmetric Full-bridge converter operation: a) operation stage 5; b) operation stage 6; c) operation stage 7; d) operation stage 8.



Source: Author.

The adopted duty cycle function is the same used by the Half-bridge arrangement with 180º phase-shift between d_{ab} and d_{gh}:

$$d_{gh}(t) = \frac{1}{2} + \frac{M_f}{2} \cdot \sin\left(\omega_g \cdot t + \phi\right)$$
$$d_{ab}(t) = \frac{1}{2} - \frac{M_f}{2} \cdot \sin\left(\omega_g \cdot t + \phi\right) \quad (40)$$

5.2.2 Modulation

Figure 40 shows the converter input and output voltages formation as well as the transformer voltages and current. There are eight different carriers, one for each bridge-leg. The phase-shift between the carriers of the bridge-legs ‘a’ and ‘b’ is 180º, as well as between ‘g’ and ‘h’. In order to provide the correct modulation, a 90º phase-shift is applied between the carriers of the bridge-legs ‘a’ and ‘g’. Figure 41a shows used carrier-based modulation scheme for the primary side of the converter.

The Figure 40a shows the waveforms for $d_{ab} > 0.25$ and $d_{gh} < 0.75$. Notice that the input and output voltage (v_{xw} and v_{yz}) of the converter has a period four times smaller than the switching period. In addition, it varies between zero and half of the DC-link voltage. The transformer voltage and current present the same behavior of the SHB converter since the duty cycle function used is equal. Figure 40b shows the same waveforms for $d_{ab} < 0.25$ and $d_{gh} > 0.75$. The converter input and output voltages (v_{xw} and v_{yz}) have four times the switching frequency as well, and they alternate between half of the DC-link and the DC-link voltages.

The behavior of the duty cycle functions d_{ab} and d_{gh} in one grid period is presented in Figure 41b, which also shows how the primary side related voltages behave in one grid period.

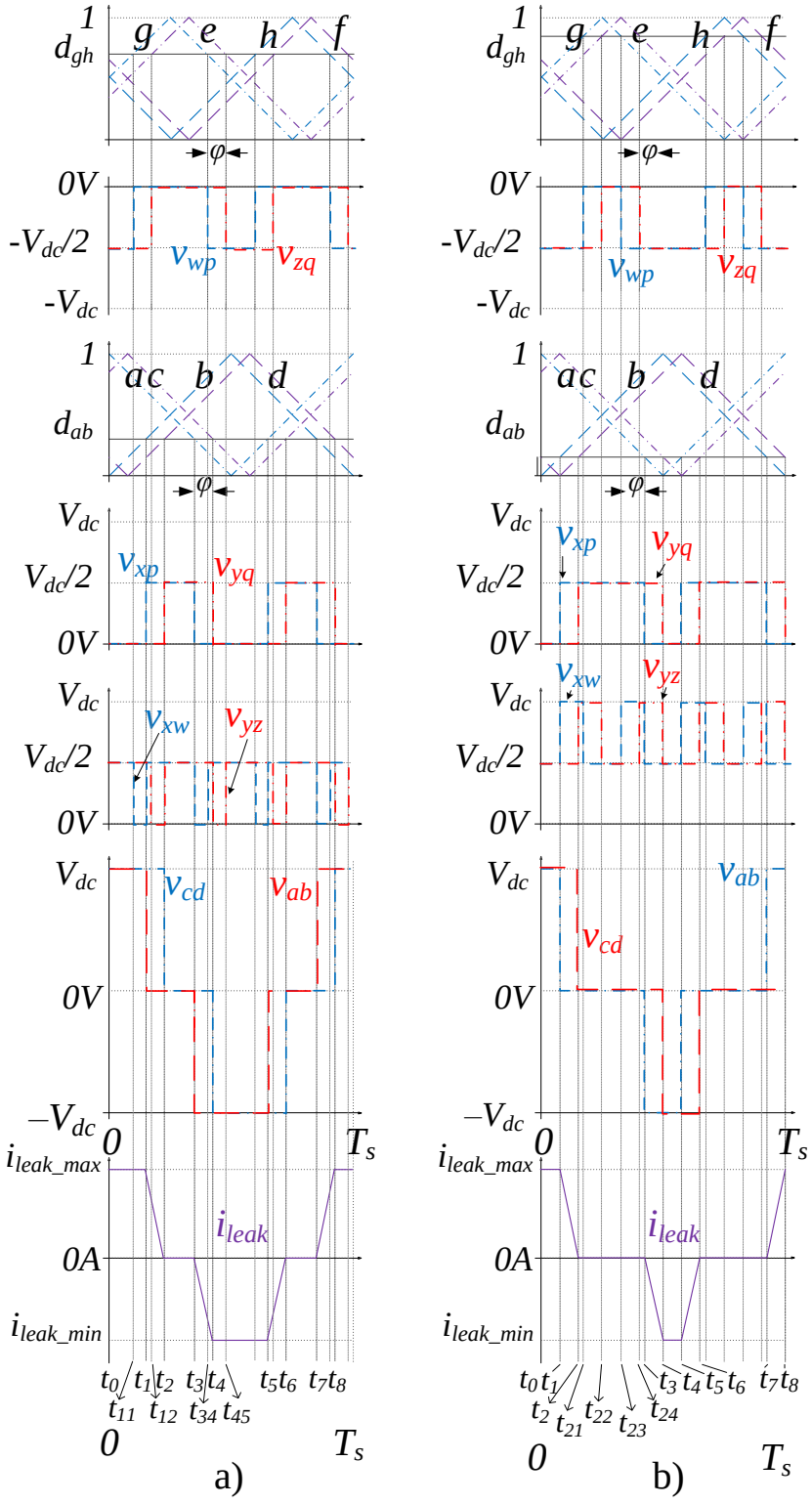
Figure 41c presents the IFB voltage generated through simulation following the values adopted in Chapter 3. The spectrum of this voltage is presented in Figure 41d, where one observes the harmonics starting from 120 kHz. The calculated WTHD is 0.0159.

5.2.3 Current ripple

Considering an ideal interleaved transformer, the input current rate is determined as:

$$\frac{diL(t)}{dt} = \frac{v_{ac1}(t) - v_{xw}(t)}{L} \tag{41}$$

Figure 40 – Modulation of the Symmetric Interleaved Full-bridge converter presenting the key voltages: a) $d_{ab} > 0.25$ and $d_{gh} < 0.75$; b) $d_{ab} < 0.25$ and $d_{gh} > 0.75$.



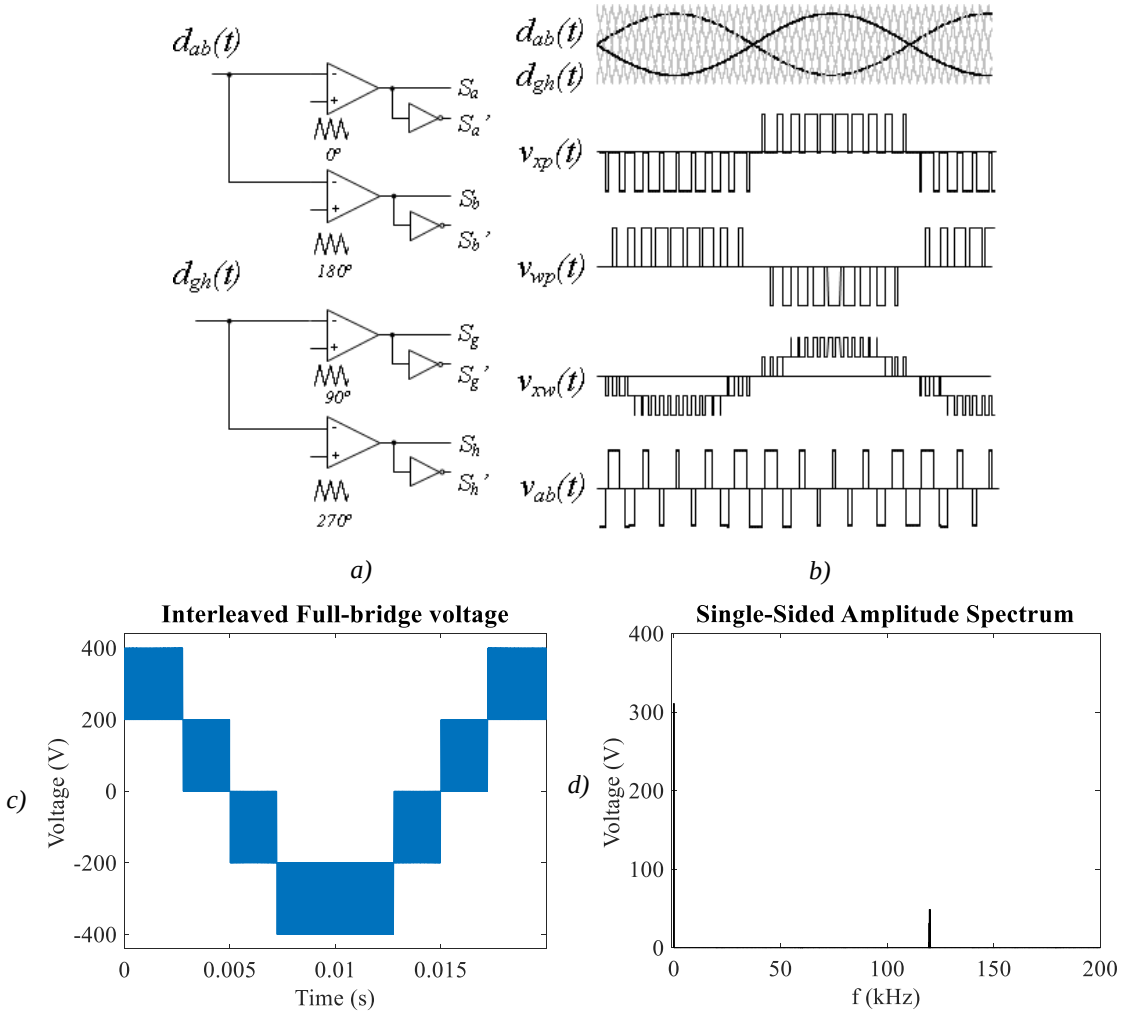
Source: Author.

One determines ΔiL for the time intervals $\Delta t_1 = [t11, t1]$ of Figure 40a and $\Delta t_2 = [t1, t21]$ of Figure 40b.

$$\frac{\Delta iL}{\Delta t_1} = \frac{V_{ac1}}{L}$$
$$\frac{\Delta iL}{\Delta t_2} = \frac{V_{ac1} - V_{dc1}}{L} \quad (42)$$

Applying $\Delta t_1 = DTs - Ts/4$, $\Delta t_2 = Ts/4 - DTs$ and (40) to (30) and considering $v_{ac1} = V_{ac1}.\sin(\omega_g.t)$, one obtains:

Figure 41 – Modulation of the Symmetric Full-bridge arrangement variating with the grid period: a) carriers and duty cycle function as modulating signal; b) carriers, duty cycle functions and generated voltages; c) converter input voltage; d) spectrum of the converter input voltage.



Source: Author.

$$\Delta iL = \frac{V_{dc1}}{4 \cdot fs \cdot L}\left(1 - 2 \cdot M_f \cdot \sin(\omega_g \cdot t)\right) \cdot M_f \cdot \sin(\omega_g \cdot \mathrm{t}) \tag{43}$$

$$\Delta iL = \frac{V_{dc1}}{4 \cdot fs \cdot L}\left(2 \cdot M_f \cdot \sin(\omega_g \cdot t) - 1\right) \cdot \left(M_f \cdot \sin(\omega_g \cdot \mathrm{t}) - 1\right) \tag{44}$$

Considering the positive cycle, the current ripple is:

$$\Delta iL = \begin{cases} \frac{V_{dc1}}{4 \cdot fs \cdot L}\left(1 - 2 \cdot M_f \cdot \sin(\omega_g \cdot t)\right) \cdot M_f \cdot \sin(\omega_g \cdot \mathrm{t}) & if \quad 0 \le \omega_g \cdot t < \theta 1 \\ \frac{V_{dc1}}{4 \cdot fs \cdot L}\left(1 - M_f \cdot \sin(\omega_g \cdot t)\right) \cdot \left(2 \cdot M_f \cdot \sin(\omega_g \cdot t) - 1\right) & if \quad \theta 1 \le \omega_g \cdot t < \pi - \theta 1 \\ \frac{V_{dc1}}{4 \cdot fs \cdot L}\left(1 - 2 \cdot M_f \cdot \sin(\omega_g \cdot t)\right) \cdot M_f \cdot \sin(\omega_g \cdot \mathrm{t}) & if \quad \pi - \theta 1 \le \omega_g \cdot t < \pi \end{cases} \tag{45}$$

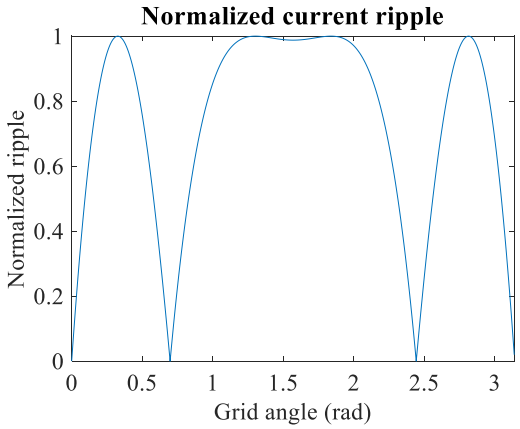
Where $\theta 1 = \sin^{-1}\left(1/(2 \cdot M_f)\right)$.

The maximal current ripple is:

$$\Delta iL \underset{\omega_g \cdot t = \theta_{\max}}{\le} \frac{V_{dc1}}{32 \cdot fs \cdot L} \tag{46}$$

Where $\theta_{\max} = \sin^{-1}\left(\frac{1}{4 \cdot M_f}\right)$ inside the interval $0 \le \omega_g.t < \theta 1$. Figure 42 shows the variation of (45) per unit.

Figure 42 – Per unit current ripple variation with the grid.



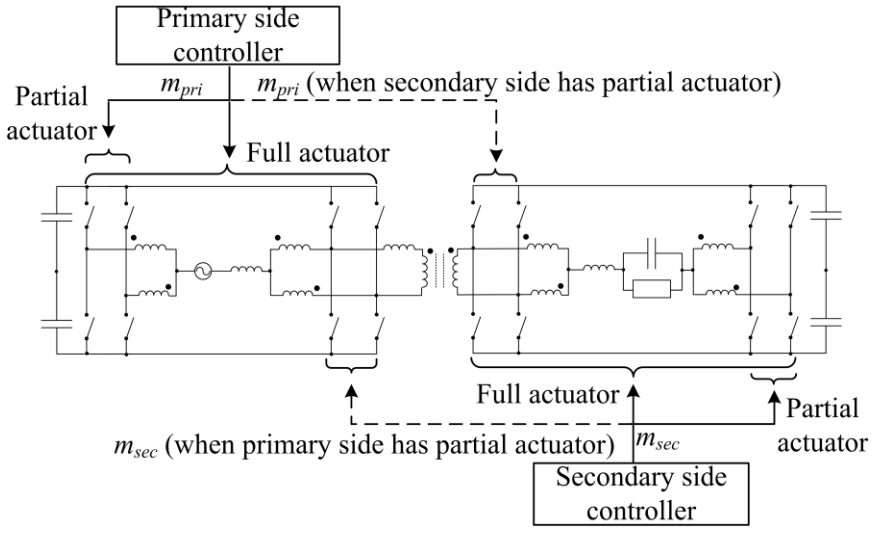
Source: Author.

5.2.4 Actuators types

As presented in Section 2.4, among other requirements, the input current and output voltage of the converter must be controlled. In addition, as can be noticed from the simplified transformer model presented Figure 17, the transformer current is related to the voltage applied to the leakage inductance, which in turn, is defined by the difference between the voltage applied to the primary and secondary windings, v_{ab} and v_{cd}, respectively. It is clear that making $d_{ab}(t) = d_{cd}(t)$ reduces the transformer current since the *rms* windings voltages depend on the duty cycle applied to the related switches.

Suppose m_{pri} is the output of the current controller on the primary side and m_{sec} the output of the AC voltage controller on the secondary side. In order to reduce the transformer current and control the input current and output voltage, the primary side current controller output is used to define the duty cycle function applied to the bridge-legs ‘a’, ‘b’, ‘g’, ‘h’, ‘c’, and ‘d’. The output of the AC voltage controller is then applied to bridge-legs ‘e’ and ‘f’. This way, the duty cycle applied to both sides of the transformer is the same and its current is minimized. The secondary side controller has a *partial actuator*, since it only controls one part of the switches of its side, while the primary side controller has *full actuator*, as presented in Figure 43. Similarly, one obtains reduced transformer current also by applying the output of the AC voltage controller (m_{sec}) to the bridge-legs ‘a’ and ‘b’, which results in *full actuator* in the secondary side and *partial actuator* in the primary side.

Figure 43 – Proposed actuator scheme allowing the same duty cycle function to be applied to both transformer’s windings.



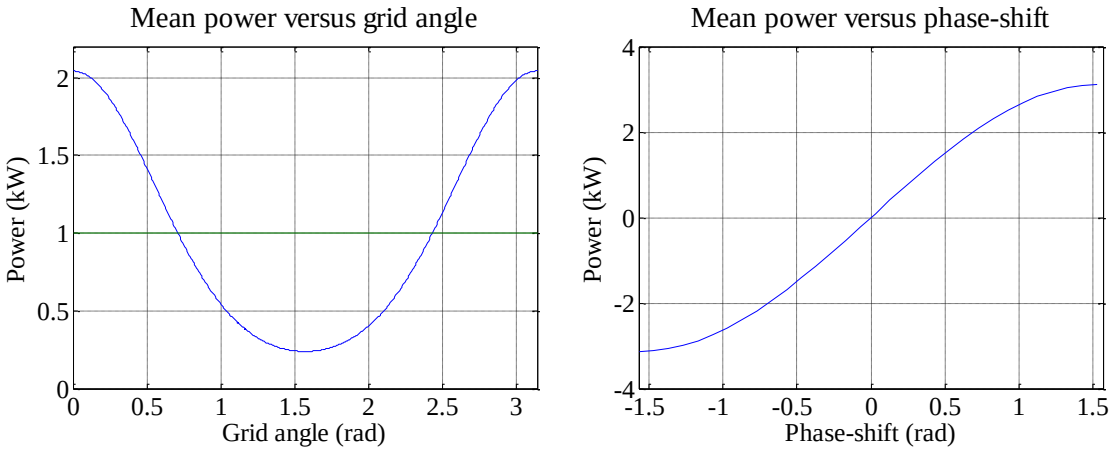
Source: Author.

5.3 Magnetics power flow analysis

As mentioned before, the duty cycle functions used by this converter are the same used by the SHB. Therefore, the transformer modeling is the same (Section 3.3).

Figure 44 shows the power flows Symmetric Interleaved Full-bridge variating according to the grid phase and the phase-shift. This example assumes the same parameters used in Section 3.3. Notice that the phase-shift required to obtain 1kW of mean power is 18.7º.

Figure 44 – Example of power flow variation for the Interleaved symmetric full-bridge converter with V_{dc1} = V_{dc2} = 400V, fs = 30 kHz, M_f = 0.778 and L_{leak} = 108 µH, for 1000W mean power: a) according to the grid voltage θ for φ = 0.33 (18.7º) showing the mean value in one grid period (straight line); b) according to the phase-shift.



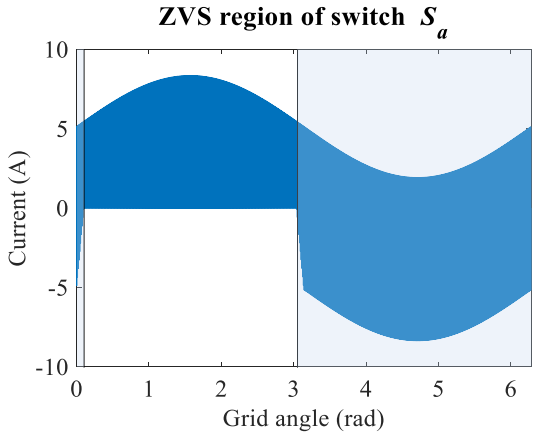
a) b)

Source: Author.

5.4 ZVS analysis

The SIFB converter applies the same duty cycle functions to the transformer's windings as the SHB does. This means that the ZVS analysis of both converters is similar. From Figure 37, the current in node 'a' is given by the difference between the interleaved transformer current and the transformer current. The switch current iS_a is obtained multiplying the node current by the gate signal. The result is presented in Figure 45, which shows the ZVS region as a function of the grid angle. The ZVS region comprises 3.35 rad (192º) of the grid voltage.

Figure 45 – Current and ZVS region of switch $S_{a.}$ of the SIFB converter.



Source: Author.

5.5 Losses estimation

5.5.1 Conduction and switching losses determination

The SIFB converter presents the highest number of switches of the proposed family. As all switches operate at high frequency, only the device SCT3120AL was used. Table 17 presents the conduction and switching losses obtained with the simulation software PLECS® and datasheet information.

Table 17 – Losses of the SFB converter with SCT3120AL.

Losses	**Value**
Conduction losses	17.04 W
Switching losses	15.21 W
Total losses	**32.25 W**

Source: Author.

5.5.2 Magnetic devices losses

The estimated losses of the inductors and interleaved transformers are similar to the one calculated for the SHB. The estimated losses of the transformer are higher due to the increased current needed to flow 1 kW from the primary to the secondary side. Table 14 presents a summary of the magnetic devices losses.

Table 18 – Magnetic devices losses.

Device	Losses value
Input/output inductor	3.09 W / 3.09 W
Input/output interleaved transformers	2 x 3.46 W / 2 x 3.46 W
Transformer	4.26 W
Total	**24.28 W**

Source: Author.

5.5.3 Electrolytic capacitor losses

Table 19 shows the biggest currents and their frequency as well as the estimated ESR value. Notice highest current component occurs at 100Hz and the estimated power loss for the whole converter is 4.77W.

Table 19 – Current values for the SFB converter and the estimated ESR values for the ELH687M450AT8 capacitor.

Capacitor	RMS current value	Estimated ESR value
Series associated capacitor	2.15 A @ 100 Hz	0.351 Ω
	0.21 A @ 200 Hz	0.234 Ω
	1.19 A @ 60 kHz	0.012 Ω
Parallel associated capacitor	1.08 A @ 100 Hz	0.351 Ω
	0.10 A @ 200 Hz	0.234 Ω
	0.59 A @ 60 kHz	0.012 Ω

Source: Author.

5.6 Experimental results

The experimental results for this converter were obtained using a different setup. A step-down transformer (1:0.566) was used with a primary DC-link voltage of 400V and a secondary DC-link voltage of 229V. The AC voltages were 220V and 100V for the grid and load, respectively. The switching frequency was 50 kHz and the output power 500W. Table 20 presents a summary of the parameters.

Table 20 – Converter experimental parameters.

Parameter	Value
Grid /load voltages	220V / 100V
Primary/secondary DC-link voltages	400V/ 229V
Output power	500 W
Input current ripple percentual	20%
Output voltage ripple	2.6V
Switching frequency	50 kHz

Source: Author.

The prototype used in this experiment was adapted from the prototype developed by (ALMEIDA; OLIVEIRA JÚNIOR, 2016) and employed SiC modules from Cree. Notice that the leakage inductance was not integrated into the transformer, requiring another core. The summary of the prototype specification is given in Table 21.

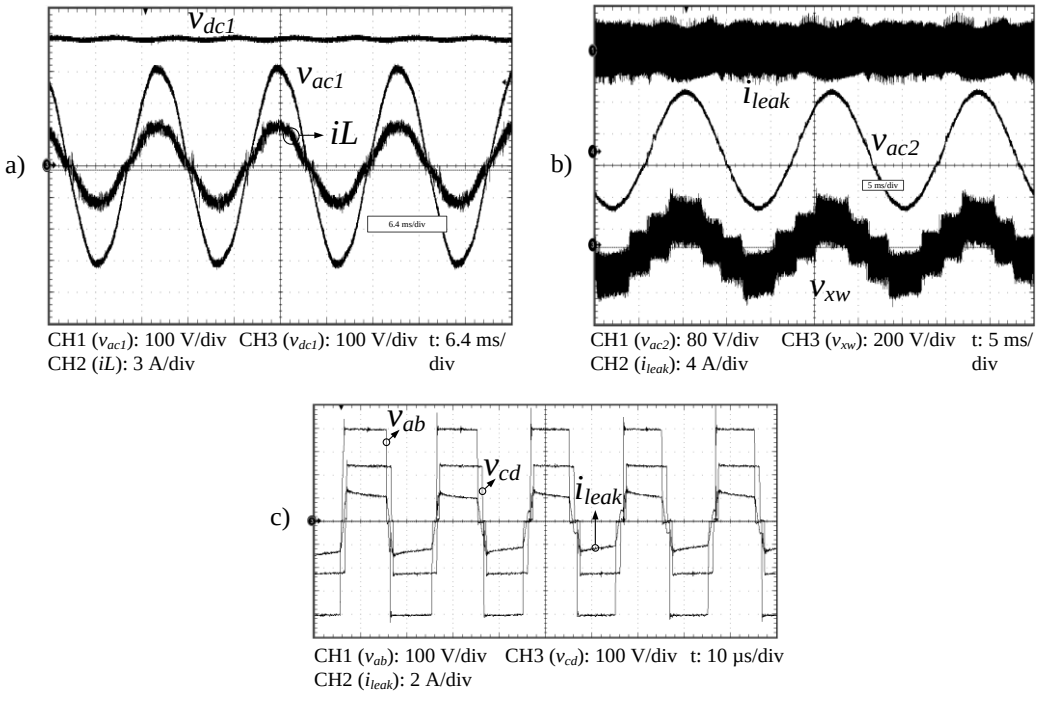
Figure 46 shows the experimental results obtained with the Symmetric Interleaved Full-bridge converter at 0.5 kW.

Table 21 – Prototype specification summary.

Prototype characteristics	**Value**
SiC modules (Cree/CCS0220M12CM2)	1.2kV/20A
Primary side DC-link (Epcos)	8x470µF/450V
Secondary side DC-link (Epcos)	6x680µF/400V
Input inductor (Magmatec - MMT034T7713)	400µH
Leakage inductance (Magmatec - MMT140T5020**)**	48µH
Transformer (Magmatec - MMT139T6325**)**	76 turns/43 turns
Output filter capacitor (KEMET)	0.44µF/250V
Output inductor (Magmatec - MMT034T7713)	250µH

Source: Author.

Figure 46 – Experimental results of the SIFB: a) grid voltage v_{ac1}, input current iL and primary DC-link voltage; b) transformer current in the secondary side i_{leak}, voltage v_{xw} and load voltage v_{ac2}; c) transformer voltages v_{ab}, and v_{cd}, and the current i_{leak};



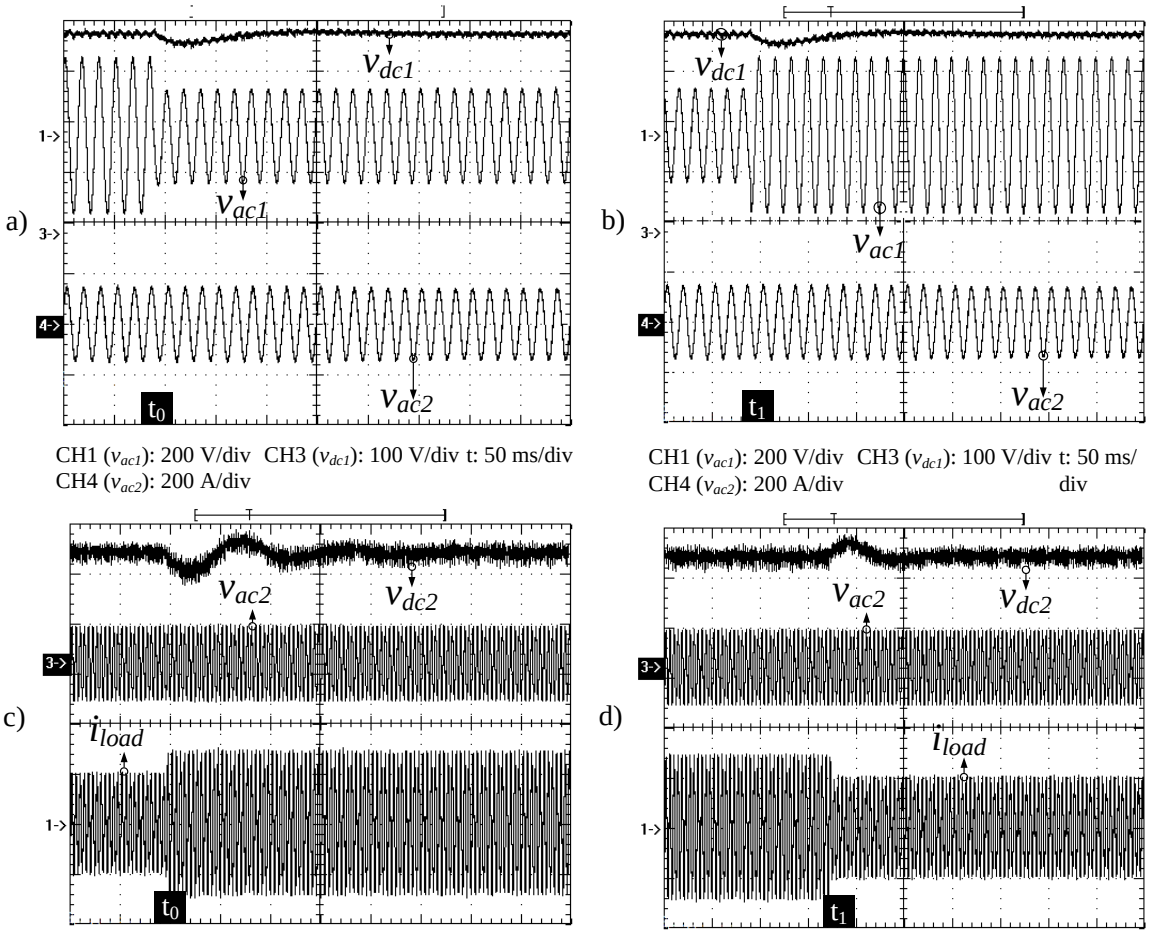
Source: Author.

Figure 46a presents the grid voltage and the input current in phase with PF = 0.99. The primary side DC-link is controlled in 400V.

Figure 46b presents the transformer current behavior (i_{leak}) and the controlled load voltage (v_{ac2}). The five-level converter input voltage (v_{xw}) is presented. Figure 46c presents in detail the transformer windings voltages v_{ab} and v_{cd} as well as the transformer current i_{leak}.

Figure 47 shows the converter dynamic response to a load step from 0.7 p.u. to 1.0 p.u. at time instant t_0 and back to 0.7 p.u. at time instant t_1, as well as a voltage sag to 0.6 p.u at time t_0 and back to 1.0 p.u. at t_1. Figure 47a and Figure 47b show the grid voltage during the voltage sag to 0.7.

Figure 47 – Experimental results (dynamic response): a) primary DC-link, grid and output voltages during a voltage sag to 0.6 p.u. b) return to nominal voltage; c) and d) load step from 0.7 p.u. to 1.0 p.u. and return.



Source: Author.

The primary side DC-link within 100ms, while the load voltage v_{ac2} is not disturbed. Figure 47c and Figure 47d depict the secondary DC-link, the load current, and voltage during a load step from 0.7p.u. to 1.0p.u. and back to 0.7p.u. The disturbance of the secondary DC-link is controlled within 100ms while the load voltage remains immune despite the load current change.

6 ASYMMETRIC CONVERTERS WITH HALF-BRIDGE AND INTERLEAVED FULL-BRIDGE ARRANGEMENTS

This Chapter presents the asymmetric converters that combine Half-bridge and Interleaved-Full-bridge arrangements. The converters presented are the HB-IFB and the IFB-HB converters. Part of the analysis required in this Chapter is present in previous Chapters and is not repeated. This is the case of the duty cycle determination of the Half-bridge arrangement (Section 3.2) and the Interleaved Full-bridge arrangement (Section 5.2). In addition, the current ripple for the HB and IFB arrangements are determined in Section Current ripple3.2.3 and 5.2.3, respectively.

Another important aspect to notice is the actuator type adopted by each converter. The IFB arrangement in both converter combinations, assume the partial actuator type and apply to its transformer connected winding, the same duty cycle function of the other transformer's winding. The result is that both converters have $d_{ab} = d_{cd}$ to minimize the transformer current. As the duty cycle function of the HB arrangement is used, the transformer power flow and ZVS analysis are the same presented in Chapter 3.

6.1 HB-IFB

6.1.1 Converter operation

The asymmetric topology Half-bridge – Interleaved Full-bridge (HB-IFB) is presented in Figure 48. The primary side of the converter is formed by a Half-bridge arrangement, while the secondary side is formed by an Interleaved Full-bridge arrangement. Therefore, this converter has a mix of characteristics, which include three-level input voltage and use of half of the DC-link voltage in the primary side. In the secondary side, it is worth to mention the presence of a five-level output voltage, current ripple frequency four times higher than the switching frequency and full use of the DC-link voltage. Table 22 shows the summarized converter switching states considering that switches S_a and S_c and switches S_b and S_d assume the same state.

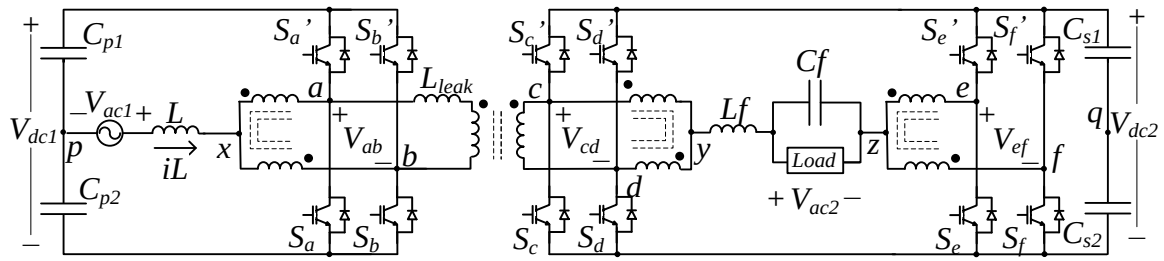
Table 22 – Switching states of the converter.

Switching state				Voltages		
S_e/S_g	S_f/S_h	S_a/S_c	S_b/S_d	$v_{ab} \mid v_{cd}$	$v_{xp} \mid v_{yp}$	$v_{xw} \mid v_{yz}$
0	0	0	0	0	$V_{dc1}/2$	0
0	0	0	1	$V_{dc1} \mid V_{dc2}$	0	$V_{dc2}/2$
0	0	1	0	$-V_{dc1} \mid -V_{dc2}$	0	$V_{dc2}/2$
0	0	1	1	0	$-V_{dc1}/2$	V_{dc2}
0	1	0	0	0	$V_{dc1}/2$	$-V_{dc2}/2$
0	1	0	1	$V_{dc1} \mid V_{dc2}$	0	*0*
0	1	1	0	$-V_{dc1} \mid -V_{dc2}$	0	*0*
0	1	1	1	0	$-V_{dc1}/2$	$V_{dc2}/2$
1	0	0	0	0	$V_{dc1}/2$	$-V_{dc2}/2$
1	0	0	1	$V_{dc1} \mid V_{dc2}$	0	*0*
1	0	1	0	$-V_{dc1} \mid -V_{dc2}$	0	*0*
1	0	1	1	0	$-V_{dc1}/2$	$V_{dc2}/2$
1	1	0	0	0	$V_{dc1}/2$	$-V_{dc2}$
1	1	0	1	$V_{dc1} \mid V_{dc2}$	0	$-V_{dc2}/2$
1	1	1	0	$-V_{dc1} \mid -V_{dc2}$	0	$-V_{dc2}/2$
1	1	1	1	0	$-V_{dc1}/2$	*0*

Source: Author.

Figure 49 presents a summary of the converter operation stages with the switches. Only the positive half cycle of the current is presented for both the input and output of the converter. Figure 51a presents the main voltages and currents waveforms of the converter. The carriers ‘a’, ‘b’ and ‘c’, and ‘d’ of the primary and secondary sides, respectively, are phase-shifted by φ. Only six time intervals are analyzed since the behavior of the others is similar. The operational stages defined by the time intervals are described below:

Figure 48 – Asymmetric topology HB-IFB.



Source: Author.

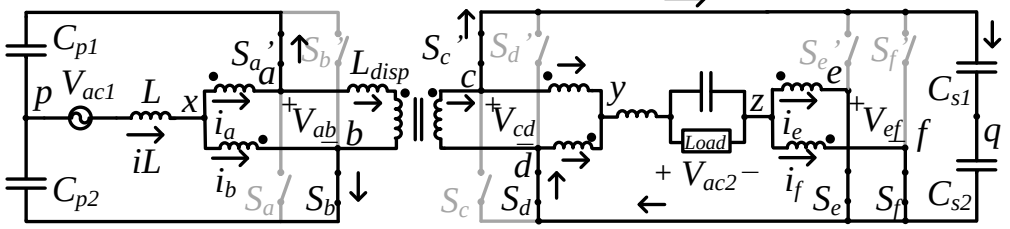
- Operation stage 1 [t_0, t_1[(Figure 49a): the switches S_b and S_d are turned on, which applies zero voltage to the input (v_{xp}) and half of the DC-link voltage to the output (v_{yq}) of the converter. The primary and secondary windings of the transformer are submitted to V_{dc1} and V_{dc2}, respectively. The transformer current remains equal to the initial value.
- Operation stage 2 [t_1, t_{12}] (Figure 49b): during this stage the switch S_b is turned off, which short circuit the interleaved transformer of the primary side, imposing the voltage $V_{dc1}/2$ to the input. The transformer primary winding voltage becomes zero and its current start to decrease. The converter output voltage remains half of its DC-link.
- Operation stage 3 [t_{12}, t_2[(Figure 49c): the switch S_e is turned on and the converter output voltage becomes zero. The converter input voltage remains the same as well as the transformer current, which continues to decrease.
- Operation stage 4 [t_2, t_3[(Figure 49d): in this stage, the switch S_d turns off, which sets zero voltage to the transformer secondary winding (v_{cd}) and the transformer current reaches zero. The converter input and output voltages are equal to half of their DC-link voltages.
- Operation stage 5 [t_3, t_4[(Figure 49d): in this stage, the switch S_a turns on, which makes the converter input voltage zero again. The output voltage remains $V_{dc2}/2$ and the voltage v_{ab} becomes negative ($-V_{dc1}$) while the voltage v_{cd} remains null. This increase the transformer current in the opposite direction.
- Operation stage 6 [t_4, t_{45}[(Figure 49d): in this stage, the switch S_c turns on, which sets equal voltages to the transformer's windings and stops its current decrease. The converter output voltage becomes zero, while the input voltage is also zero.

6.1.2 Modulation

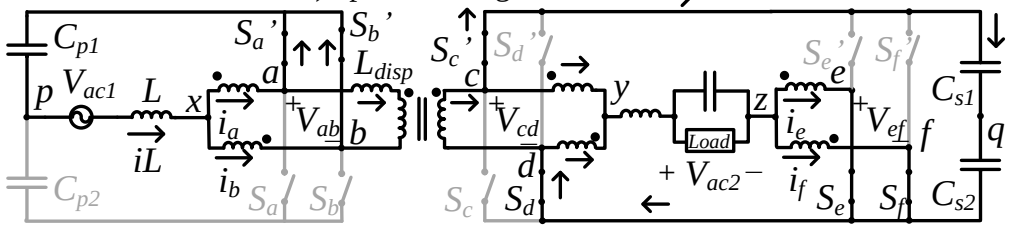
Figure 51 shows the input and output voltage formation and the transformer voltages and currents. There are six carriers involved, two are on the primary side and the other four on the secondary side. The carriers phase displacement follows the standard used by the Half-bridge and Interleaved Full-bridge arrangements mentioned in previous Chapters.

Figure 49 – Half-bridge - Interleaved Full-bridge converter operation: a) operation stage 1; b) operation stage 2; c) operation stage 3; d) operation stage 4; e) operation stage 5; e) operation stage 6.

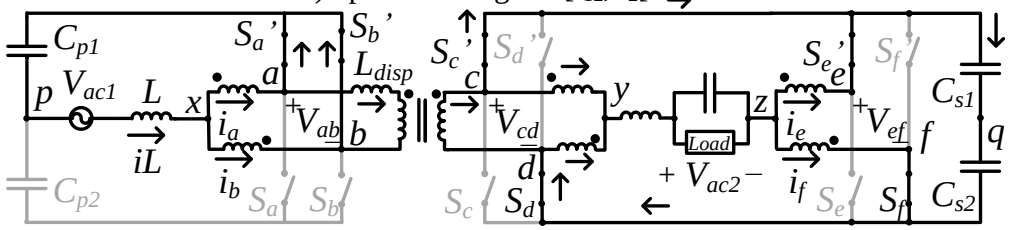
a) operation stage 1: [t_0, t_1[



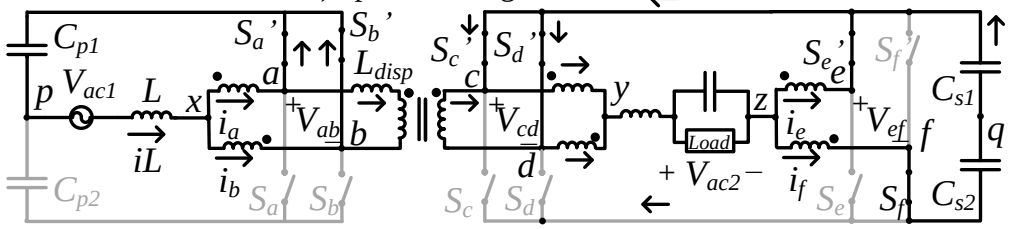
b) operation stage 2: [t_1, t_{12}[



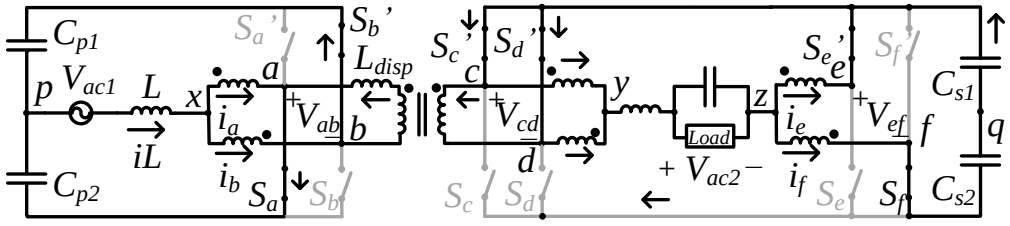
c) operation stage 3: [t_{12}, t_2[



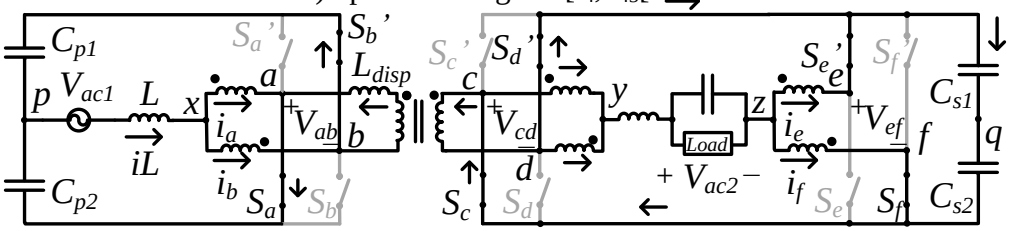
d) operation stage 4: [t_2, t_3[



e) operation stage 5: [t_3, t_4[



d) operation stage 6: [t_4, t_{45}[



Source: Author.

Figure 51a shows the waveforms for $d_{ab} > 0.25$ and $d_{ef} < 0.75$. In this duty cycle range, the converter output voltage alternates between zero and half of the secondary DC-link voltage, while the converter input voltage assumes zero or half of its DC-link voltage. Figure 51b presents the same waveforms but for $d_{ab} < 0.25$ and $d_{ef} > 0.75$. In this case, the converter output voltage alternates between half and the total DC-link voltage, while the input voltage is limited to half of its DC-link voltage. Notice in both cases the converter input voltage frequency is half of the output voltage frequency.

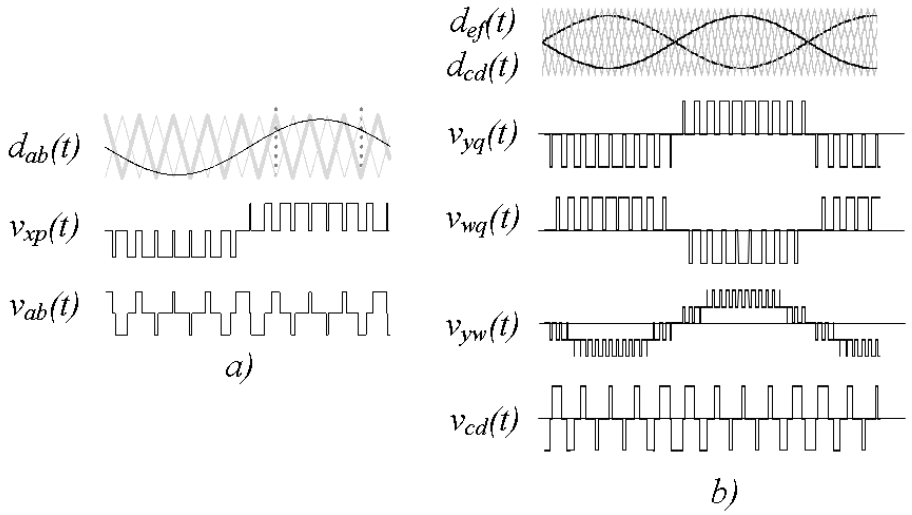
The same duty cycle function is used to define the transformer's winding voltages as occurred with the symmetric converters. In this case, the duty cycle function of Half-bridge arrangement is adopted by the bridge-legs 'c' and 'd', defining a partial actuator in the converter secondary side. For this reason, the transformer voltage and current waveforms are the same.

Figure 50 depicts the main converter voltages variating in the time scale of one grid voltage period. The primary side voltages are presented in Figure 50a while the secondary side voltages are presented in Figure 50b.

6.1.3 Losses estimation

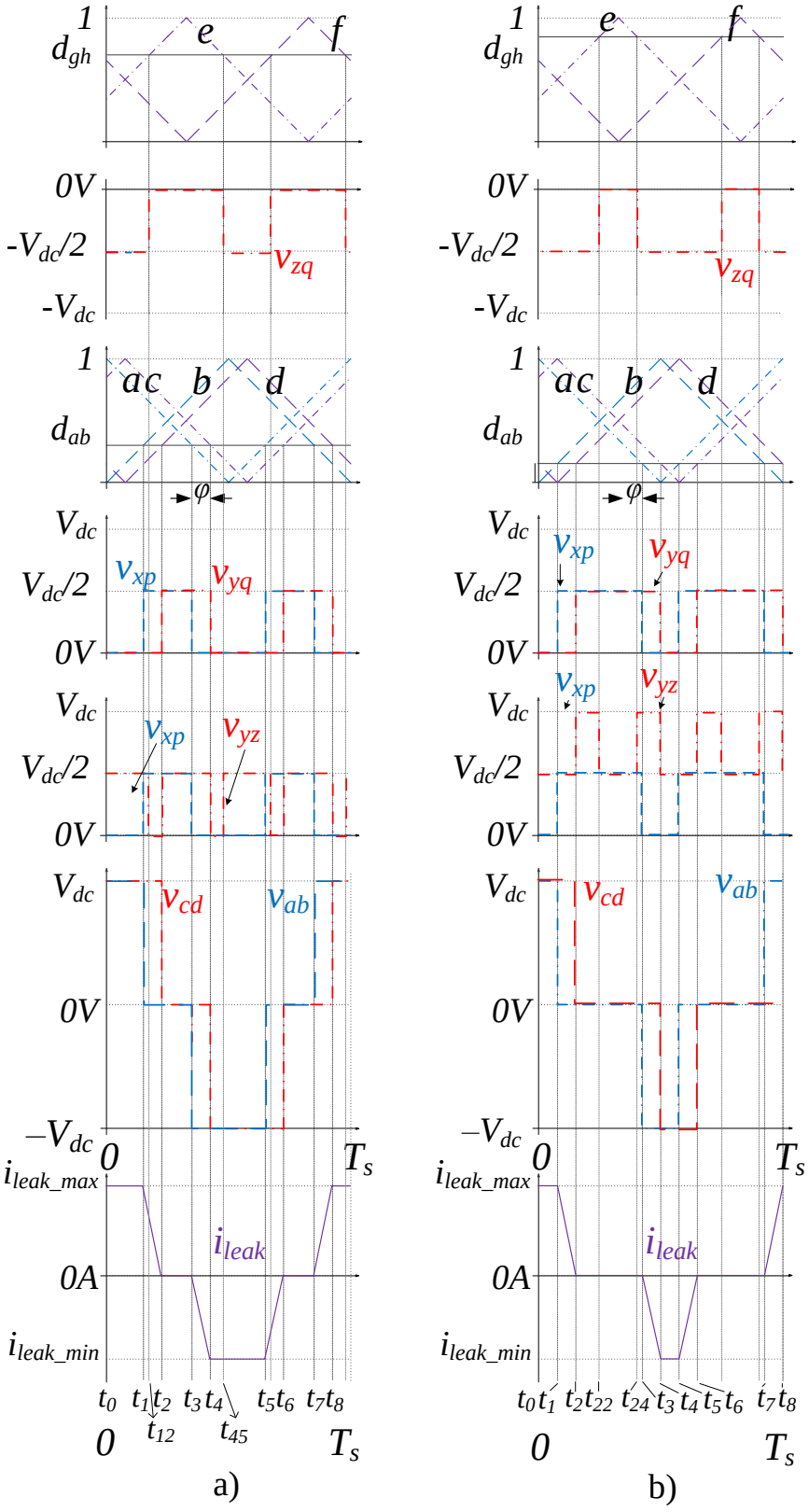
The losses estimation are very similar to the one performed to the SHB converter since the same magnetic devices are used. There are differences though, regarding the switches and the electrolytic capacitors.

Figure 50 – Carriers and generated voltages variating with the grid period: a) Half-bridge arrangement modulation; b) Interleave Full-bridge arrangement modulation..



Source: Author.

Figure 51 – Modulation of the HB-IFB arrangement with key voltages for: a) $d_{ab} > 0.25$ and $d_{ef} < 0.75$; b) $d_{ab} < 0.25$ and $d_{ef} > 0.75$.



Source: Author.

6.1.3.1 Conduction and switching losses determination

In this topology, only high-frequency modulation was applied. Therefore, the switch SCT3120AL from Rohm was used in all legs. Table 23 presents the conduction and switching losses obtained with the simulation software PLECS® and datasheet information.

Table 23 – Losses of the SFB converter with SCT3120AL switches.

Losses	**Value**
Conduction losses	8.41 W
Switching losses	5.12W
Total losses	**13.53 W**

Source: Author.

6.1.3.2 Magnetic devices losses

This converter works with different voltage and current levels in the primary and secondary sides. In addition, the load power used is the same as the SHB (0.5 kW), which reduces the current in the secondary side due to higher voltage employed in the Interleaved Full-bridge arrangement. This reduces the losses of the inductor and interleaved transformer placed on the secondary side. The transformer loses are the same experienced by the SHB.

Table 24 – Magnetic devices losses.

Device	**Losses value**
Input/output inductor	3.50 W / 2.4 W
Input/output interleaved transformer	4.23 W / 2 x 2.10 W
Transformer	3.14 W
Total	**17.47 W**

Source: Author.

6.1.3.3 Electrolytic capacitor losses

The layout of both DC-link capacitors is the same used previously. In the primary side, the HB arrangement is used with the connection of the DC-link. In the secondary side, this connection is not present due to the IFB arrangement. Table 25 shows the most significant currents and their frequency as well as the estimated ESR value. Notice that there is no 50Hz

component circulating in the DC-link only on the primary side. The estimated power loss for the whole converter is 6.0W.

Table 25 – Current values for the SFB converter and the estimated ESR values for the ELH687M450AT8 capacitor.

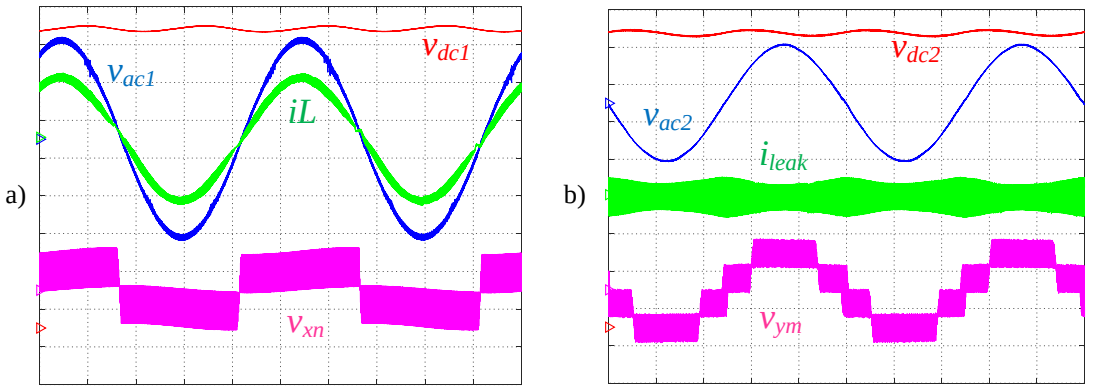
Converter side	Capacitor	RMS current value	Estimated ESR value
Primary	Series associated	2.33 A @ 50 Hz	0.468 Ω
		0.54 A @ 60 kHz	0.012 Ω
	Parallel associated	1.06 A @ 100 Hz	0.351 Ω
		1.09 A @ 60 kHz	0.012 Ω
Secondary	Series associated	1.04 A @ 100 Hz	0.351 Ω
		0.08 A @ 200 Hz	0.234 Ω
		0.86 A @ 60 kHz	0.012 Ω
	Parallel associated	1.03 A @ 100 Hz	0.351 Ω
		0.07 A @ 200 Hz	0.234 Ω
		0.83A @ 60 kHz	0.012 Ω

Source: Author.

6.1.4 Experimental results

Figure 52 presents the HB-IFB converter operating at nominal power (0.5 kW). The input voltage and current are presented in Figure 52a with the converter input voltage v_{xp} and the primary side DC-link voltage (v_{dc1}). The PF obtained was 0.996 and the current THD was 6.66%. Figure 52b shows the secondary side variables with the load voltage v_{ac2} controlled on 220V, and the secondary DC-link controlled on 400V. The load voltage THD was 1.67%.

Figure 52 – Experimental results at nominal power (0.5 kW): a) converter primary side variables; b) secondary side variables.



CH1 (v_{ac1}): 60 V/div CH3 (v_{dc1}): 50 V/div t: 4 ms/ div
CH2 (iL): 4 A/div CH4 (v_{xn}): 200 V/div

CH1 (v_{ac2}): 200 V/div CH3 (v_{dc2}): 50 V/div t: 4 ms/ div
CH2 (i_{leak}): 7 A/div CH4 (v_{yq}): 300 V/div

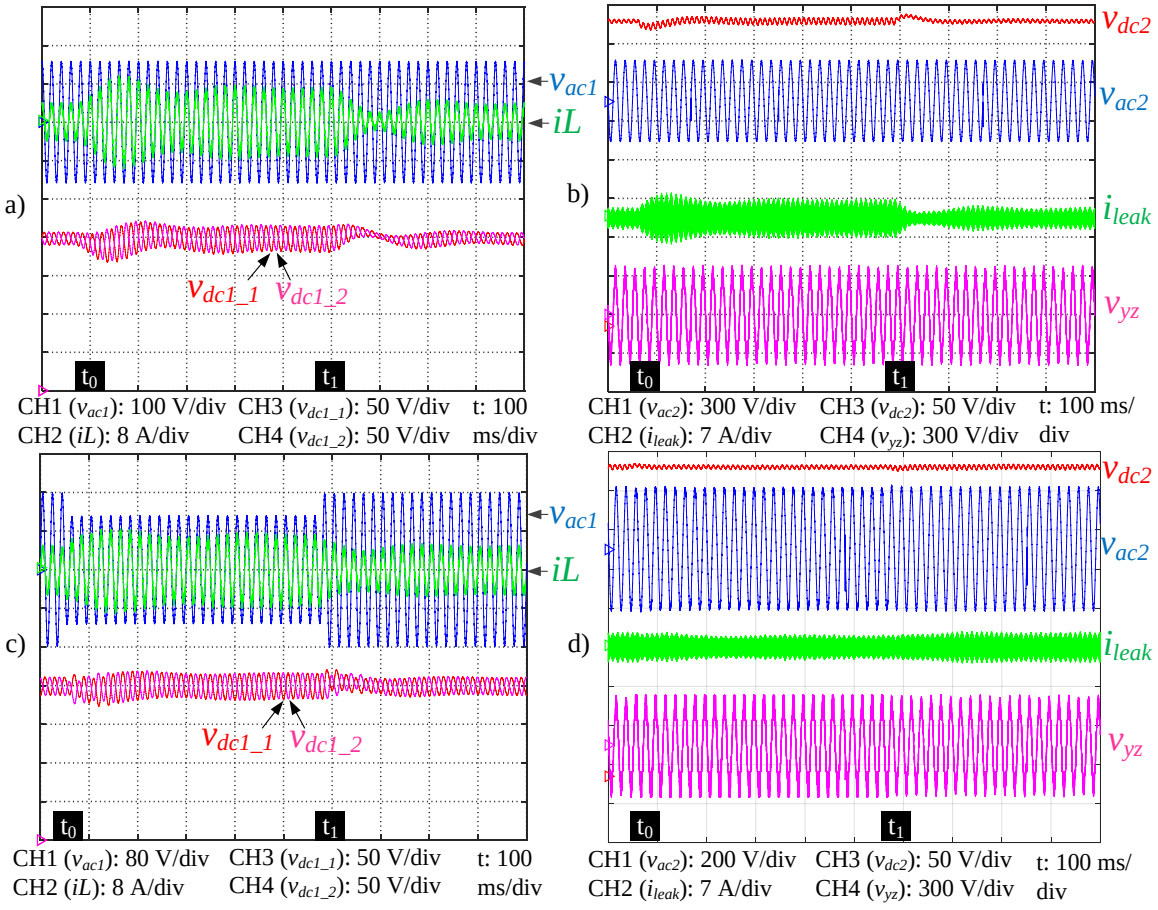
Source: Author.

As mentioned before, the duty cycle function applied to the transformer primary and secondary sides is the same, which leads to the same transformer voltages and current waveforms obtained with the SHB converter.

Figure 53 presents the dynamic response of the converter to a load step and a voltage sag. The load step from 0.5 p.u. to 1.0 p.u. occurs at t_0 and returns to 0.5 p.u.at t_1. The input voltage sink to 0.7 p.u. at t_0 and returns to 1.0 p.u. at t_1. Figure 53a shows the primary side variables during the load step.

Notice the increase in the input current caused by the increased load. As the primary side features an HB arrangement, it is important to verify the voltage share between the DC-link upper capacitor (v_{dc1_1}) and lower capacitor (v_{dc1_2}). One observes that the voltages of the capacitors maintained the equilibrium during the transitory, as well as in steady-state. Figure 53b shows the dynamic response of the secondary side variables. A small DC-link voltage

Figure 53 – Experimental results (dynamic response): a) and b) primary and secondary sides variables, respectively, during a step response (0.5 p.u. - 1.0 p.u); c) and d) primary and secondary sides variables, respectively, during a voltage sag to 0.7 p.u.



Source: Author.

perturbation can be observed at both time instants t_0 and t_1. The increased transformer current shows the increased power flow. The converter output voltage is also presented as well as the load voltage (v_{ac2}) which remains unchanged.

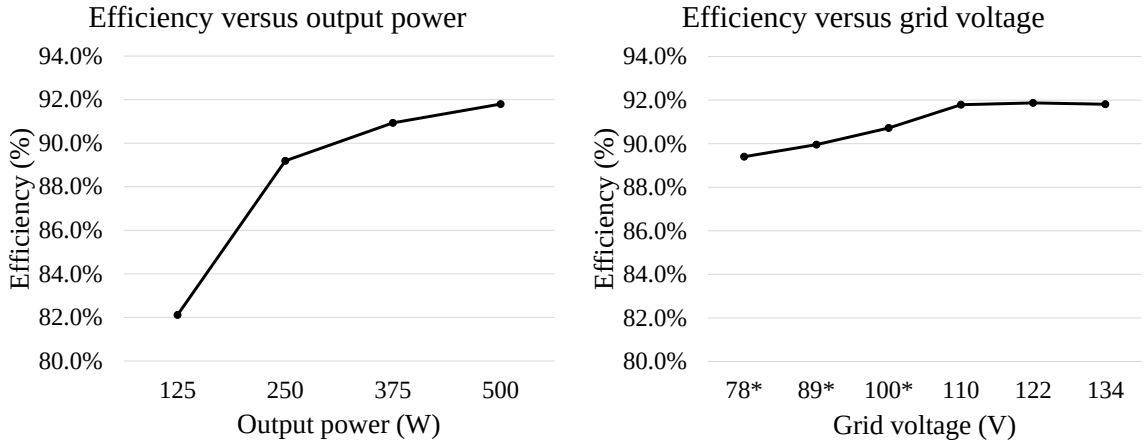
The same variables presented in Figure 53a are presented in Figure 53c, which depicts a voltage sag to 0.7 p.u[4]. The input current increases due to the voltage reduction and this perturb the DC-link voltage however, the voltage across the capacitors is split equally.

Figure 53d presents the secondary side variables during the voltage sag. Notice that the load voltage is not affected by the voltage sag. The DC-link voltage is marginally perturbed as well as the transformer current. When a voltage sag occurs, the modulation index of the primary side is reduced, exactly in the same way that occurred with the SHB converter. As the same duty cycle function is applied to both transformer's sides, the outcome is different from the obtained with the SHB and there is no transformer current increase, as it occurred with the SHB converter.

Figure 54 presents the obtained efficiencies for different load levels and different grid voltage levels.

Figure 54a shows that the efficiency increase with the load reaching its peak value (91.8%) at 0.5 kW. Figure 54b[5] shows the efficiency variation for different input voltages.

Figure 54 – Efficiency results: a) efficiency with changing output power; b) efficiency changing grid voltage.



Source: Author.

[4] Due to current limit imposed by the voltage source, this test was performed with reduced power (350W).

[5] Due to the voltage source current limit the converter had to be derated to 350 W (78V) and 400W (89V and 100V).

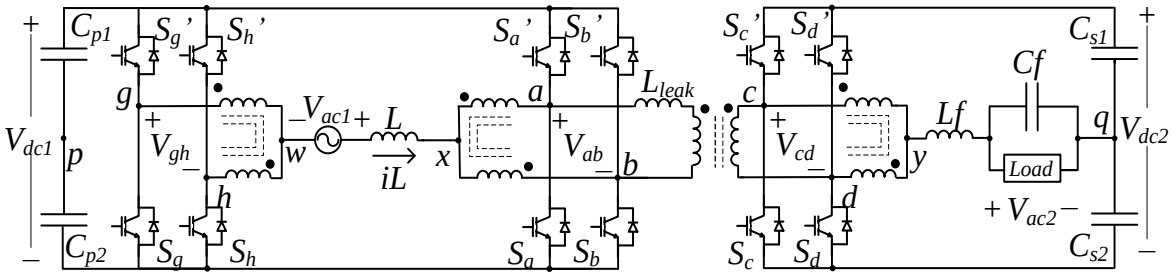
6.2 IFB-HB

In this topology, depicted in Figure 55, the Interleaved Full-bridge arrangement is placed on the primary side while the Half-bridge arrangement is placed on the secondary side. This converter is similar to the HB-IFB converter since it uses the same arrangements. The different characteristics of each arrangement are now applied to the opposite side of the converter. Therefore, it is straightforward to analyze this converter based on the analysis performed in the previous section.

One difference between the converters is that the duty cycle generated by the secondary side controller is now applied to the legs ‘a’ and ‘b’, which configures the primary side of the converter to have a partial actuator.

As both converters work similarly, only the simulation results are presented for this converter.

Figure 55 – Asymmetric topology IFB-HB.

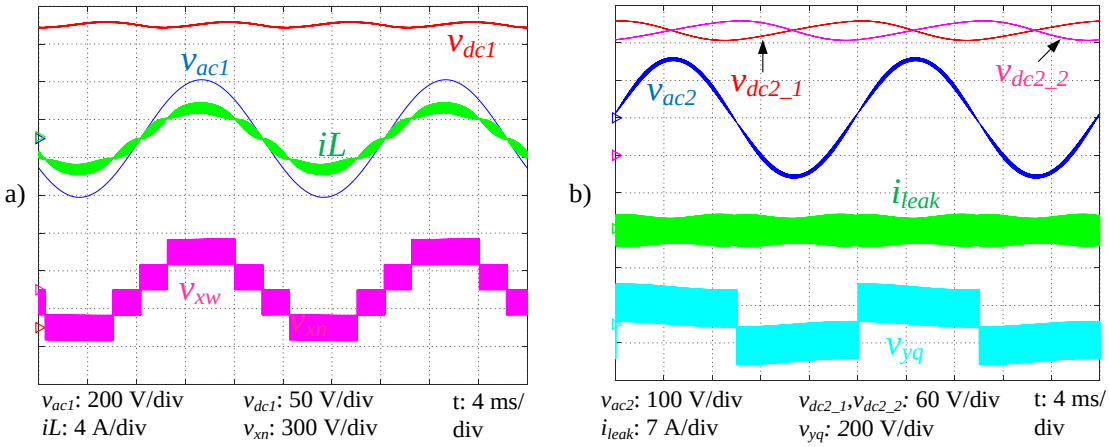


Source: Author.

6.2.1 Simulation results

Figure 56 presents the simulation results running at 0.5 kW. The primary side variables are presented in Figure 56a. The DC-link voltage is controlled in 400V while the grid voltage and input current are in phase with PF = 0.999. The input current presents a THD of 6.70%. The five-level converter input voltage (v_{xw}) is also presented. The secondary side variables are depicted in Figure 56b. The voltages of the upper (v_{dc2_1}) and lower (v_{dc2_2}) capacitors are controlled in 200V each. The load voltage is also controlled in 110V with a THD of 2.95%. The transformer current, as well as the three-level output voltage, are also presented.

Figure 56 – Simulation results at nominal power: a) converter primary side variables; b) secondary side variables.

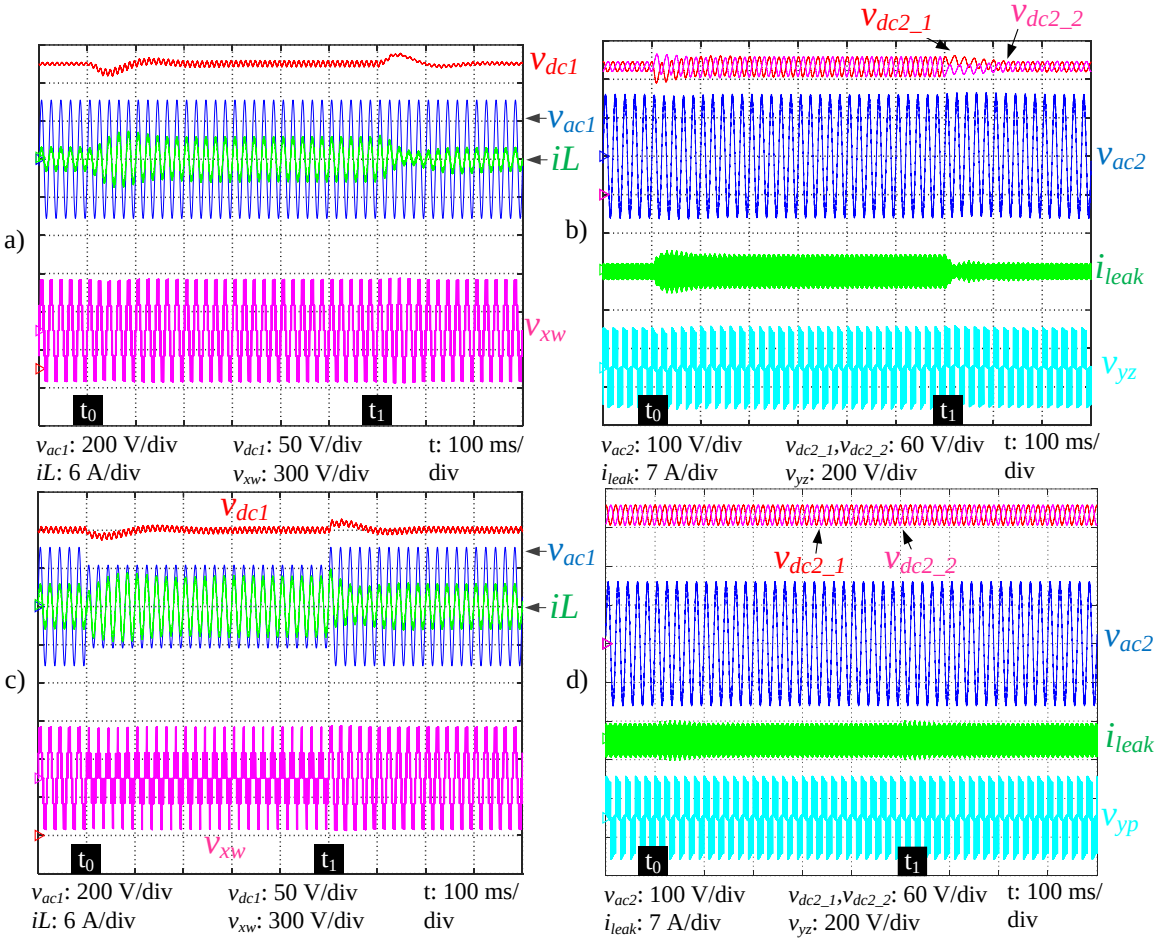


Source: Author.

The converter dynamic response is presented in Figure 57. The converter is submitted to a load step (0.5 p.u. to 1.0 p.u.) at time instant t_0 and back to 0.5 p.u. at time instant t_1. The converter is also submitted to a grid voltage decrease to 0.7 p.u. at time instant t_0 and back to 1.0 p.u. at t_1. Figure 57a shows the primary side variables during the load step. It shows the increase of the input current due to the increased load and that the DC-link voltage returns to the reference value in 200ms. Figure 57b depicts the transformer current increase during the load step. In addition, one notices the natural equilibrium between the voltages of the upper and lower capacitors. The load voltage is not disturbed during the load step.

Figure 57c shows the primary side variables during the voltage sag. During the sag, the input voltage reduces, which makes the input current increase. The modulation index is reduced, but this reduction is performed by the bridge-legs ‘g’ and ‘h’, since the duty cycle function applied to the bridge-legs ‘a’ and ‘b’ comes from the load voltage controller (v_{ac2}). The disturbance in the DC-link is controlled in around 200 ms. The secondary DC-link voltage is almost not affected by the voltage sag, as well as the equilibrium between the capacitors’ voltages of the link, as observed in Figure 57d. Notice that, as the same duty cycle function is used on both sides of the transformer, the voltage sag doesn’t affect the transformer current. The load voltage control is also not disturbed.

Figure 57 – Simulation results (dynamic response): a) and b) primary and secondary sides variables, respectively, during a step response (0.5 p.u. - 1.0 p.u); c) and d) primary and secondary sides variables, respectively, during a voltage sag to 0.7 p.u.



Source: Author.

7 ASYMMETRIC CONVERTERS WITH HALF-BRIDGE AND FULL-BRIDGE ARRANGEMENTS

This Chapter presents the asymmetric converters that combine Half-bridge and Full-bridge arrangements. The converters presented are the HB-FB and the FB-HB. As occurred in the previous Chapter, part of the analysis required was already presented previously. This is the case of the duty cycle determination of the Half-bridge arrangement (Section 3.2.1) and the Full-bridge arrangement (Section 4.2.1). In addition, the current ripple for the HB and FB arrangements are determined in Sections 3.2.3 and 4.2.3, respectively.

In order to reduce the transformer current one can apply the same duty cycle function in both transformer's windings. Regarding the converters analyzed in this Chapter, one possibility is to apply the modulation of the Half-bridge arrangement to the Full-bridge arrangement. The opposite is not possible since the Full-bridge modulation requires another leg, which the Half-bridge arrangement does not have.

Applying the Half-bridge primary side controller output to the Full-bridge arrangement on the secondary side, for instance, enforces the secondary side to have a partial actuator. Therefore, the modulation applied in Chapter 4 cannot be used since the low-frequency switching of the leg 'm' (Figure 58) is not be able to meet the control requirements of the converter side to which this arrangement is placed.

This Chapter presents a different modulation for the Full-bridge arrangement that allows the Half-bridge duty cycle function to be used on both sides of the transformer. Therefore, the analysis of the transformer power flow is the same presented in Section 3.3.

7.1 HB-FB

The topology Half-bridge – Full-bridge (HB-FB) is presented in Figure 58. This converter combines the Half-bridge arrangements characteristics on the primary side and the modified Full-bridge arrangement characteristic on the secondary side. The converter output voltage presents five-levels, but due to the new high-frequency modulation, its effective frequency is reduced to the switching frequency. Table 26 shows the summarized converter switching states considering that switches S_a and S_c and switches S_b and S_d assume the same state.

Table 26 – Switching states of the converter.

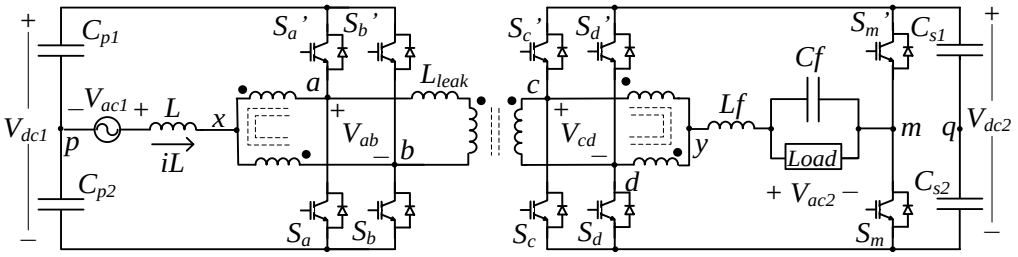
Switching state				Voltages	
S_m	S_a/S_c	S_b/S_d	$v_{ab} \mid v_{cd}$	v_{xp}	v_{ym}
0	0	0	0	$V_{dc1}/2$	0
0	0	1	$V_{dc1} \mid V_{dc2}$	0	$-V_{dc2}/2$
0	1	0	$-V_{dc1} \mid -V_{dc2}$	0	$-V_{dc2}/2$
0	1	1	0	$-V_{dc1}/2$	$-V_{dc2}$
1	0	0	0	$V_{dc1}/2$	V_{dc2}
1	0	1	$V_{dc1} \mid V_{dc2}$	0	$V_{dc2}/2$
1	1	0	$-V_{dc1} \mid -V_{dc2}$	0	$V_{dc2}/2$
1	1	1	0	$-V_{dc1}/2$	*0*

Source: Author.

7.1.1 Converter modulation

In this converter, the leg ‘m’ of the secondary side operates at the same frequency of the other legs, but due to the absence of the interleaved transformer, the voltage applied between the points ‘m’ and ‘q’ can only be positive ($v_{dc2}/2$) or negative ($-v_{dc2}/2$). The modulation of the legs ‘c’ and ‘d’ is tied to the Half-bridge arrangement of the primary side. Therefore, the leg ‘m’ should be modulated with a 180º opposed duty cycle function.

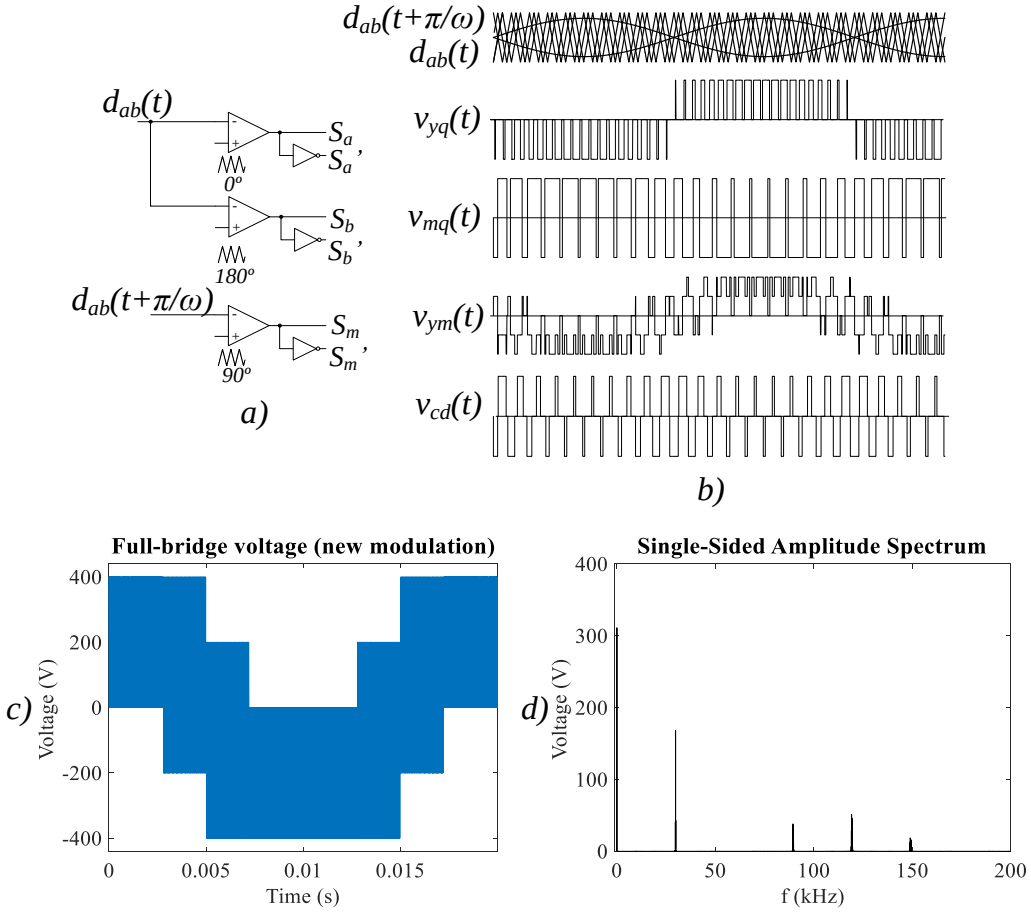
Figure 58 – Asymmetric topology HB-FB.



Source: Author.

The modulation arrangement, as well as an illustrative example of the generated waveforms for the Full-bridge arrangement, is presented in Figure 59. Notice that the carrier of the leg ‘m’ has a 90º phase-shift from the carrier of leg ‘c’ Figure 59a. Figure 59b presents the generated voltage waveforms. The frequency of the resulting converter output voltage (v_{ym}) (Figure 59c) waveform is the same as the switching, which increases the current ripple when compared to the previous modulations. This can be observed in the spectrum of the generated

Figure 59 – Carriers and generated voltages variating with the grid period of the HB-FB converter: a) modulation arrangement used; b) carriers and generated voltage waveform; c) generated voltage; d) spectrum of the generated voltage.

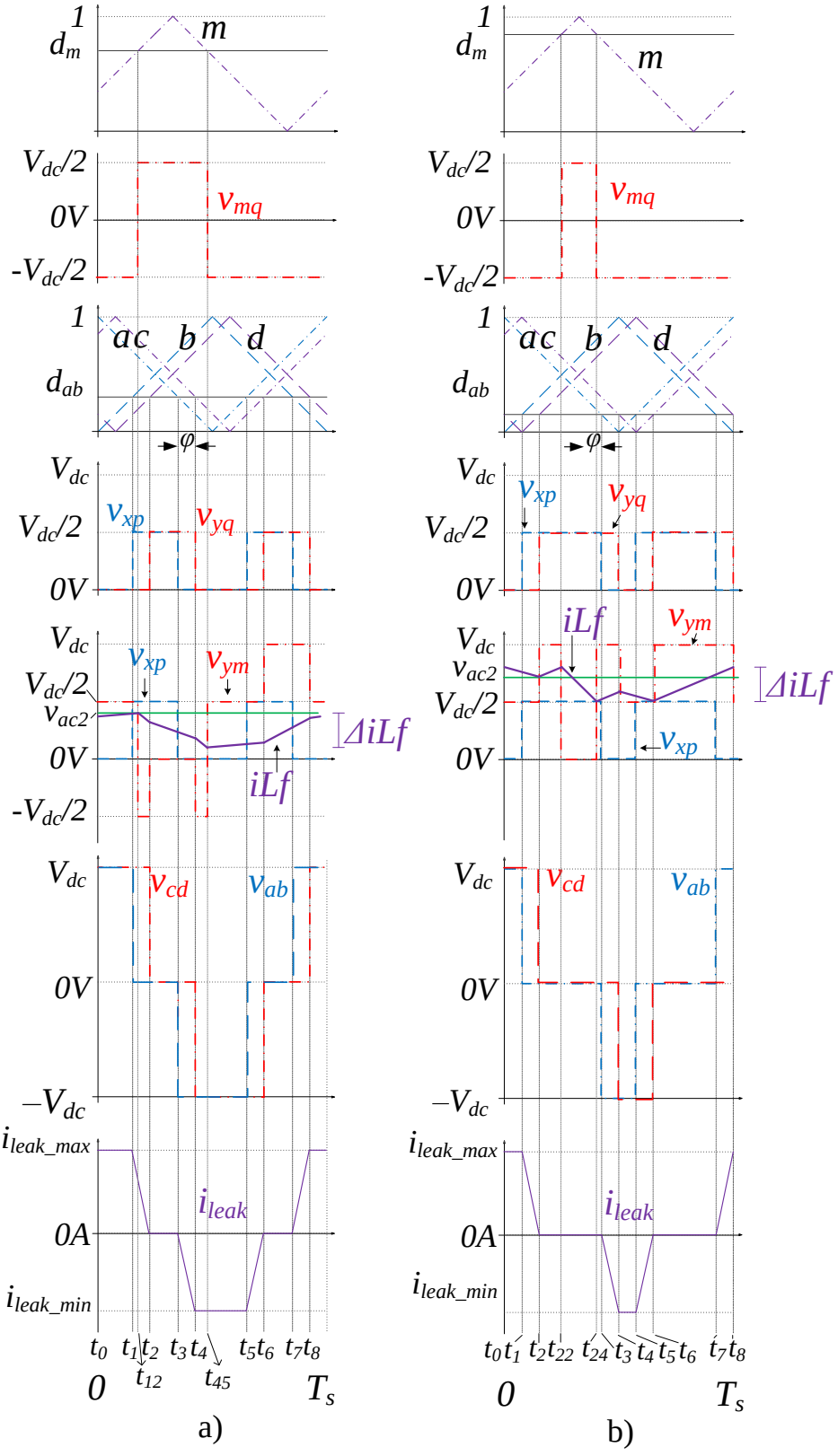


Source: Author.

voltage depicted in Figure 59d. The highest harmonic content is present in 30 kHz, but there are also harmonics in 90 kHz, 120 kHz, and 150 kHz. The calculated WTHD is 0.0980.

Figure 60 presents the modulating waveforms, with the respective carriers and the resulting converter voltages and currents for one switching period. The Figure 60a presents the voltage waveforms valid for $0.25 < d_{ab}$, $d_m < 0.75$. Notice that the Half-bridge arrangement voltages are the same as previously observed. The converter output voltage v_{ym} is formed by the difference between v_{yq} and v_{mq} and presents three different levels inside one period ($-V_{dc2}/2$, 0 and V_{dc2}). In addition, it is clear that this voltage waveform repeats every switching period, which is a drawback when compared with the Full-bridge arrangement with low-frequency modulation. The output current (iLf) waveform is also depicted. Figure 60b shows the voltage waveforms valid for $0 < d_{ab}$, $d_m < 0.25$ and $0.75 < d_{ab}$, $d_m < 1.0$. The characteristics of the output voltage v_{ym} are the same, with three levels in one switching period (0, $V_{dc2}/2$ and V_{dc2}).

Figure 60 – Modulation of the HB-FB arrangement with key voltages for: a) $d_{ab} > 0.25$ and $d_{ef} < 0.75$; b) $d_{ab} < 0.25$ and $d_{ef} > 0.75$.



Source: Author.

The duty cycle applied to the leg ‘m’ (d_m) has 180º phase-shift to the duty cycle applied to the legs ‘c’ and ‘d’. As it is considered that the same duty cycle function is applied to the primary and secondary sides of the transformer, $d_m = 1 - d_{ab}$. The transformer-related voltages and current are the same observed for the SHB since the modulating reference is equal to (8).

7.1.2 Converter operation

Figure 61 and Figure 62 present the operation stage of this converter, considering positive current circulating in the grid and in the load. The converter operation is based on the waveforms depicted in Figure 60a. There are ten distinct time intervals in one switching period, and they are used to describe in details the converter operation.

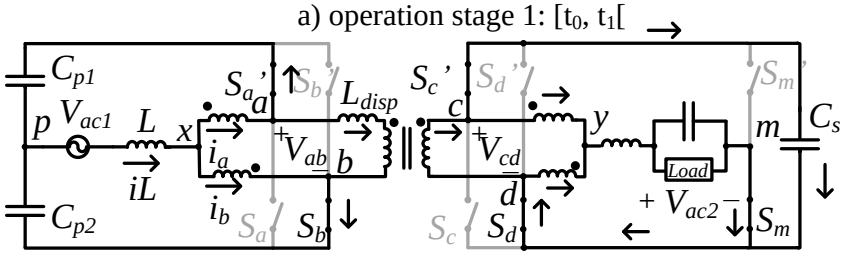
- Operation stage 1 [t_0, t_1[(Figure 61a): the switches S_b and S_d and S_m are turned on, which applies zero voltage to the input (v_{xp}) and $-V_{dc2}/2$ to the output (v_{ym}) of the converter. The primary and secondary windings of the transformer are submitted to V_{dc1} and V_{dc2}, respectively. The transformer current remains equal to the initial value.
- Operation stage 2 [t_1, t_{12}] (Figure 61b): during this stage the switch S_b is turned off, which short circuit the interleaved transformer of the primary side, imposing the voltage $V_{dc1}/2$ to the input. The transformer primary winding voltage becomes zero and its current start to decrease. The converter output voltage remains the same.
- Operation stage 3 [t_{12}, t_2[(Figure 61c): the switch S_m is turned off and the converter output voltage becomes half of the Dc-link voltage. The converter input voltage remains the same as well as the transformer current, which continues to decrease.
- Operation stage 4 [t_2, t_3[(Figure 61d): in this stage, the switch S_d turns off, which sets zero voltage to the transformer secondary winding (v_{cd}) and the transformer current reaches zero. The converter input voltage is equal to half of its DC-link voltage. The current stops circulating through the DC-link of the secondary side and the converter output voltage becomes zero.
- Operation stage 5 [t_3, t_4[(Figure 61e): in this stage, the switch S_a turns on, which makes the converter input voltage zero again. The output voltage remains zero

and the voltage v_{ab} becomes negative ($-V_{dc1}$) while the voltage v_{cd} remains null. This increase the transformer current in the opposite direction.

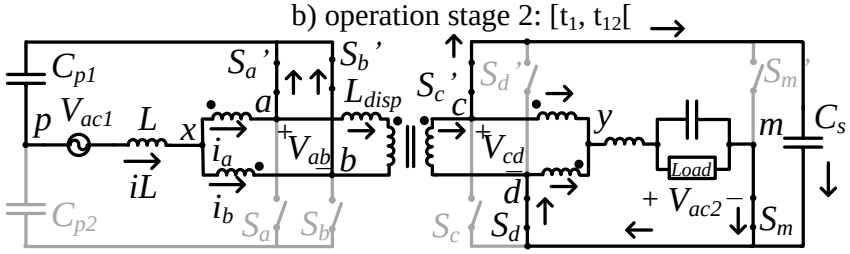
- Operation stage 6 [t_4, t_{45}[(Figure 62a): in this stage, the switch S_c turns on, which sets equal voltages to both transformer's windings and stops its current decrease. The converter output voltage becomes $-V_{dc2}/2$, while the input voltage is zero.

Figure 61 – Half-bridge - Full-bridge converter operation: a) operation stage 1; b) operation stage 2; c) operation stage 3; d) operation stage 4; e) operation stage 5.

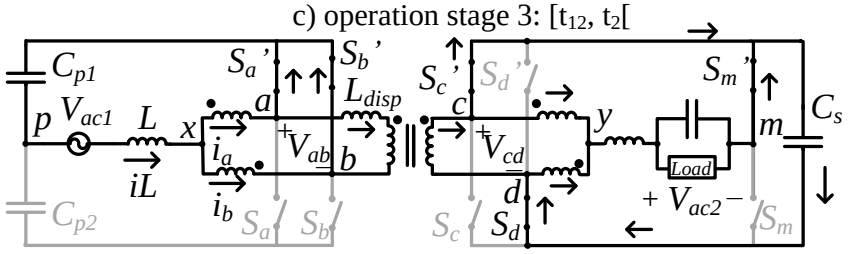
a) operation stage 1: [t_0, t_1[



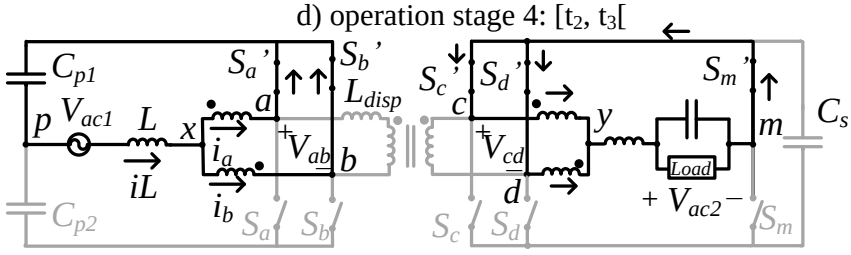
b) operation stage 2: [t_1, t_{12}[



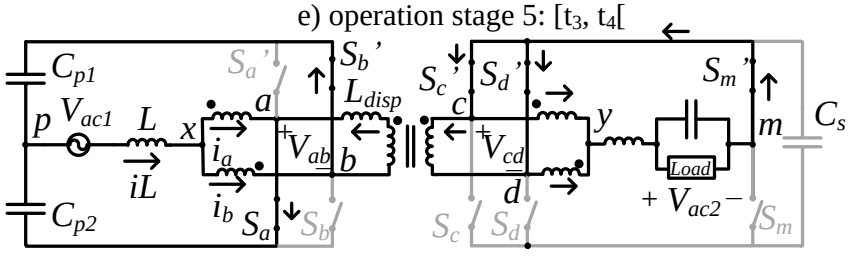
c) operation stage 3: [t_{12}, t_2[



d) operation stage 4: [t_2, t_3[



e) operation stage 5: [t_3, t_4[



Source: Author.

- Operation stage 7 [t_{45}, t_5[(Figure 62b): the switch S_m is turned on, which sets the converter output voltage to $V_{dc2}/2$. The converter input voltage is zero and both transformer windings have the same voltage, which maintains the transformer current constant.
- Operation stage 8 [t_5, t_6[(Figure 62c): the switch S_a is turned off, which sets the converter input voltage to half of the DC-link. The voltage applied to the primary transformer winding is zero, which drives its current to zero. The converter output voltage remains unchanged,
- Operation stage 9 [t_6, t_7[(Figure 62d): in this stage, the switch S_c is turned off. Both transformer windings voltages are zero and the transformer current becomes zero. The converter input voltage remains unchanged while the output voltage becomes V_{dc2}. The current in the DC-link inverts its direction and the DC-link start to discharge.
- Operation stage 10 [t_7, t_8[(Figure 62e): the switch S_b is turned on and the input voltage becomes zero. The output voltage remains V_{dc2}, The transformer primary voltage becomes V_{dc1} which start to increase its current,

7.1.3 Current ripple

The ripple of the Full-bridge arrangement with high-frequency modulation can be determined following the steps presented in Section 3.2.3. Naming the output filter inductor current *iLf* and considering sinusoidal the load voltage $v_{ac2}(t) = V_{ac2}.\sin(\omega.t)$, the current rate is determined as:

$$\frac{diLf(t)}{dt} = \frac{v_{ym}(t) - v_{ac2}(t)}{Lf} \tag{47}$$

Observing the filter current *iLf* in Figure 60a, one notices that the current during time interval [t12, t5] variates from the maximum to the minimum value, which enables the determination of the current ripple, which is the summation of the current decrease during the segments [t12, t2], [t2, t4] and [t4, t45].

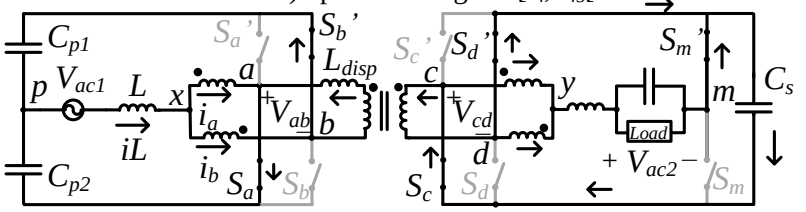
The time interval segments [t12, t2] and [t4, t45] have the same current rate and are computed together. The total time interval for these segments is $\Delta t_1 = D.Ts - (Ts/2 - D.Ts)$, while the converter output voltage is $-V_{dc2}/2$. The time interval segment [t2, t4] and it is given by $\Delta t_2 = Ts/2 - D.Ts$, while the converter output voltage is zero. The current ripple equation is:

$$\frac{\Delta iLf_1}{\Delta t_1} = \frac{V_{ac1} - V_{dc1}/2}{Lf}$$
$$\frac{\Delta iLf_2}{\Delta t_2} = \frac{V_{ac1}}{Lf} \quad (48)$$

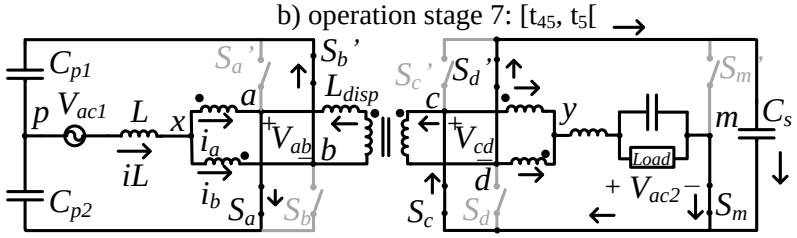
Considering $v_{ac2} = V_{ac2}\sin(\omega_g t)$ and the duty cycle function of the Half-bridge arrangement (8), the resulting current ripple is given by:

Figure 62 – Half-bridge - Full-bridge converter operation: a) operation stage 6; b) operation stage 7; c) operation stage 8; d) operation stage 9; e) operation stage 10.

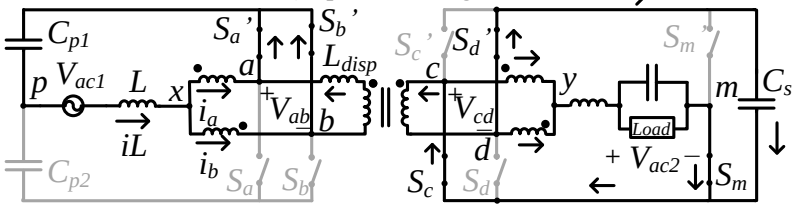
a) operation stage 6: [t_4, t_{45}[



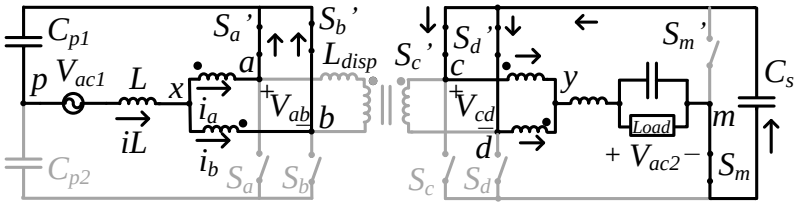
b) operation stage 7: [t_{45}, t_5[



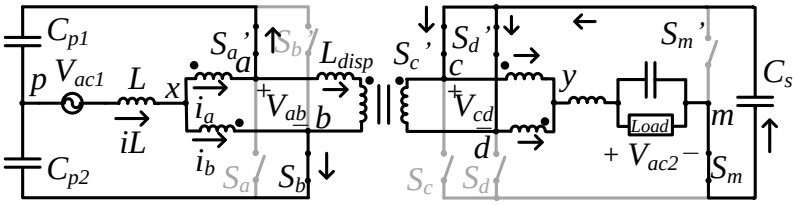
c) operation stage 8: [t_5, t_6[



d) operation stage 9: [t_6, t_7[



e) operation stage 10: [t_7, t_8[



Source: Author.

$$\Delta iLf_1 = \frac{V_{dc2}}{4 \cdot fs \cdot Lf} \cdot \left[\left(2 \cdot M_f \cdot \sin(\omega_g \cdot t) \right)^2 - 1 \right]$$
$$\Delta iLf_2 = \frac{2 \cdot V_{dc2}}{4 \cdot fs \cdot Lf} \cdot \left(M_f \cdot \sin(\omega_g \cdot t) \right)^2 \quad (49)$$

$$\Delta iLf = \Delta iLf_1 + \Delta iLf_2 = \frac{V_{dc2}}{4 \cdot fs \cdot Lf} \cdot \left[2 \cdot \left(M_f \cdot \sin(\omega_g \cdot t) \right)^2 - 1 \right] \quad (50)$$

The above equation is valid for $0.25 < d_m < 0.75$. For the range $0 < d_m < 0.25$ and $0.75 < d_m < 1.0$, the current ripple is computed from time interval [t2, t24] in Figure 60b, where v_{ym} is zero and it is given by:

$$\frac{\Delta iLf}{\Delta t_1} = \frac{V_{ac2}}{Lf} \quad (51)$$

Applying $\Delta t_1 = (D - 0.5).Ts$ one obtains:

$$\Delta iL = \frac{2 \cdot V_{dc1}}{4 \cdot fs \cdot L} \cdot \sin(\omega_g \cdot t) \cdot \left(1 - M_f \cdot \sin(\omega_g \cdot t) \right) \quad (52)$$

Considering the positive cycle and $S_n = 1$, the current ripple is:

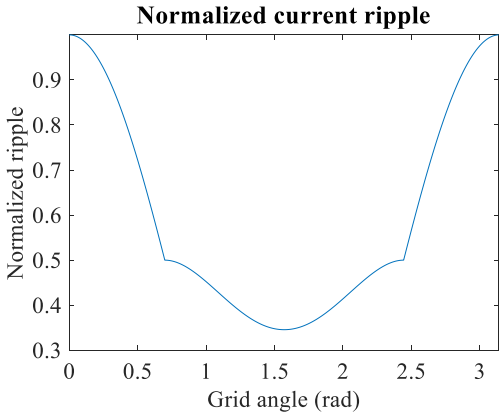
$$\Delta iL = \begin{cases} \frac{V_{dc2}}{4 \cdot fs \cdot Lf} \cdot \left[2 \cdot \left(M_f \cdot \sin(\omega_g \cdot t) \right)^2 - 1 \right] & if \quad 0 \le \omega_g \cdot t < \theta 1 \\ \frac{2 \cdot V_{dc2}}{4 \cdot fs \cdot L} \cdot \sin(\omega_g \cdot t) \cdot \left(1 - M_f \cdot \sin(\omega_g \cdot t) \right) & if \quad \theta 1 \le \omega_g \cdot t < \pi - \theta 1 \\ \frac{V_{dc2}}{4 \cdot fs \cdot Lf} \cdot \left[2 \cdot \left(M_f \cdot \sin(\omega_g \cdot t) \right)^2 - 1 \right] & if \quad \pi - \theta 1 \le \omega_g \cdot t < \pi \end{cases} \quad (53)$$

Where $\theta 1 = \sin^{-1}\left(1 / (2 \cdot M_f) \right)$. The maximal current ripple is:

$$\Delta iL \underset{\omega_g \cdot t = \theta_{\max}}{\le} \frac{V_{dc2}}{4 \cdot fs \cdot L} \quad (54)$$

Where $\theta_{\max} = n \cdot \pi \quad n = 0, 1, 2, \ldots$. Figure 63 shows the variation of (53) per unit.

Figure 63 – Per unit current ripple variation with the grid.



Source: Author.

7.1.4 Input inductor design

In order to reduce the losses produced by the modulation scheme in the filter inductor, a new filter inductor with ferrite core was designed. The design was made to achieve the same inductance of the previous design (Section 3.5). Table 27 presents the summary of the inductor design.

Table 27 – Design parameters of the filter inductor.

Parameter	**Value**
Core	ETD 59/31/22
Material	Ferrite N87
Peak flux density (B_{peak})	0.32 T
Flux density ripple (ΔB)	0.12 T
Inductance (L)	645 µH
Ripple frequency	30 kHz
Inductance fator (A_L)	350 nH/turns^2
Current density	450 A/cm^2
Wire diameter	1.4 mm
Air gap	1.5 mm
Number of turns	51 turns

Source: Author.

7.1.5 Losses estimation

7.1.5.1 Conduction and switching losses determination

In this converter, only high-frequency modulation was applied. This means the leg 'm' of the Full-bridge arrangement is switched at 30 kHz. The switch used in this leg is SCT3030AL, while the other legs used the SCT3120AL. Table 28 presents the conduction and switching losses obtained with the simulation software PLECS® and datasheet information.

Table 28 – Losses of the SFB converter with SCT3120AL switches.

Losses	**Value**
Conduction losses	5.49 W
Switching losses	8.80W
Total losses	**14.29 W**

Source: Author.

7.1.5.2 Magnetic devices losses

The estimated transformer losses are the same observed in the Symmetric Half-bridge converter. The input inductor losses estimation is obtained from the Half-bridge arrangement, while the output inductor loss is calculated with Steinmetz equation. The interleaved transformer losses are the same obtained in Section 6.1.3.2. The summary of the magnetic losses is presented in Table 29.

Table 29 – Magnetic devices losses.

Device	**Losses value**
Input/output inductor	3.5 W / 2.6 W
Input/output interleaved transformer	4.23 W / 2.10 W
Transformer	3.14 W
Total	**15.57 W**

Source: Author.

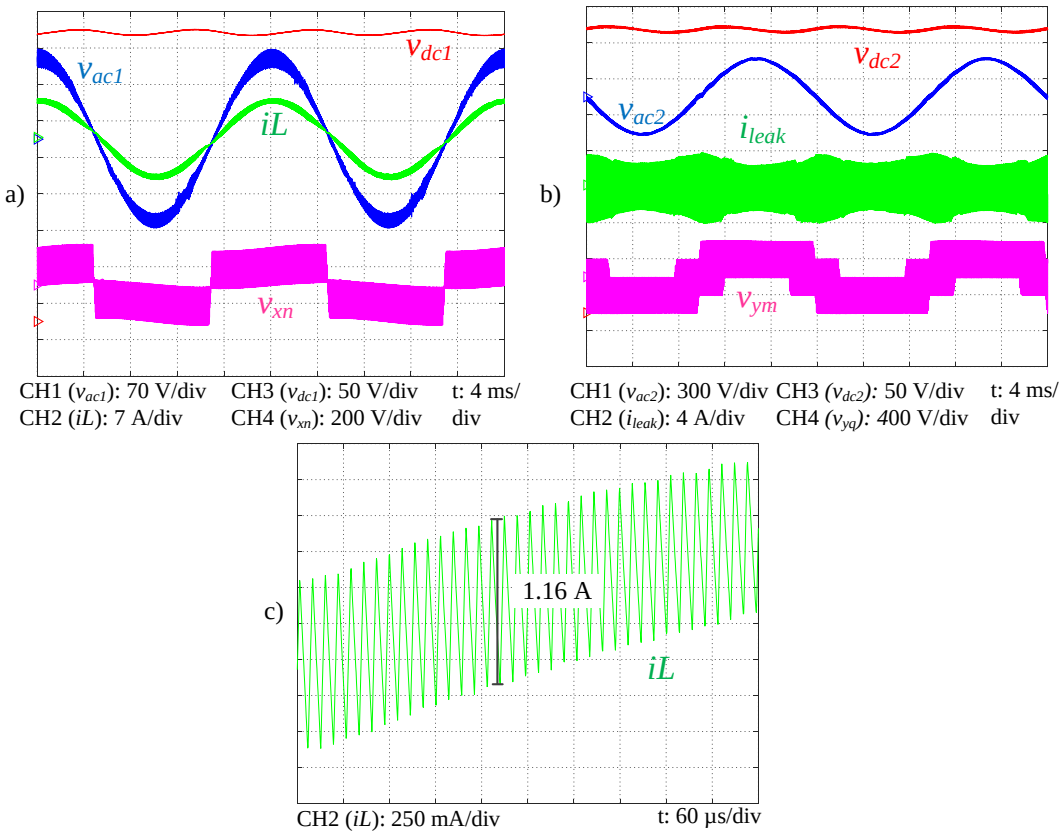
7.1.5.3 Electrolytic capacitor losses

The layout of both DC-link capacitors is the same used in the HB-IFB converter. The resulting currents in both DC-link are the same and they generate the same losses (~6W) for both DC-links.

7.1.6 Experimental results

Figure 64 presents the HB-FB converter operating at 0.5 kW. The grid voltage and the input current are presented in Figure 64a. They are in phase and have a power factor of 0.996 with a current THD of 6.85%. Figure 64c shows the obtained input current ripple of 1.16A. The primary side DC-link voltage is controlled in 400V as well as the secondary side DC-link voltage presented in Figure 64b. Figure 64b also shows the converter output voltage v_{ym}. The load voltage v_{ac2} is sinusoidal and controlled in 220V. With an increased filter capacitance (680µF), the THD of v_{ac2} is 4.94%. The transformer current, presented in Figure 64b, is very similar to the one obtained with the HB-IFB converter (Figure 52b). It should be noticed that, although the same duty cycle waveform was applied to the primary and secondary

Figure 64 – Experimental results (HB-FB) at nominal power (0.5 kW): a) converter primary side variables; b) secondary side variables; c) input current ripple.

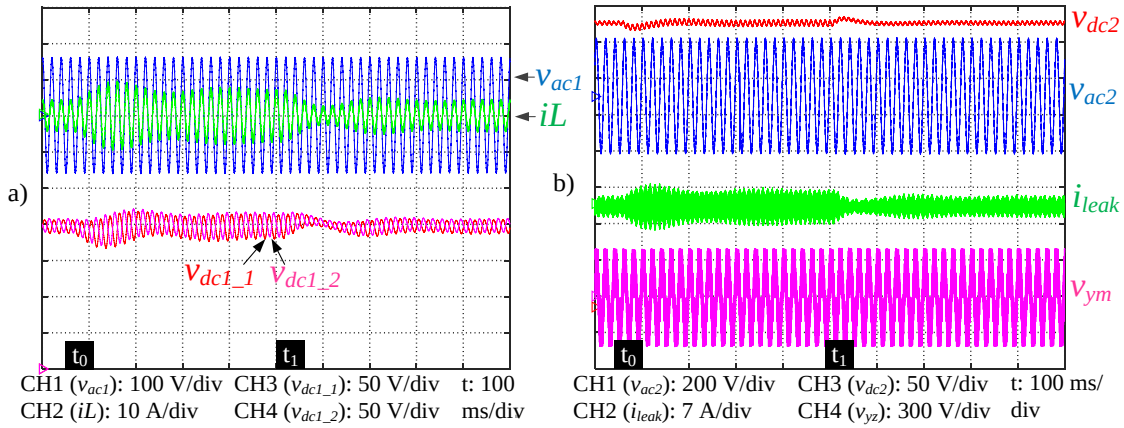


Source: Author.

sides, the experimental results were collected with both sides (primary and secondary) employing full actuators.

Figure 65 presents the dynamic response of the converter to a load step from 0.5 p.u. to 1.0 p.u. at t_0 and back to 0.5 p.u.at t_1. Notice the increase in the input current caused by the increased load (Figure 65a). It is clear that the voltage is equally distributed between the DC-link upper capacitor (v_{dc1_1}) and lower capacitor (v_{dc1_2}). This occurs during the transitory and also in steady-state. Figure 34b shows the dynamic of the secondary side variables. A small DC-link voltage perturbation can be observed at both time instants t_0 and t_1. The increased transformer current shows the increased power flow. The converter output voltage is also presented as well as the load voltage (v_{ac2}) which remains unchanged.

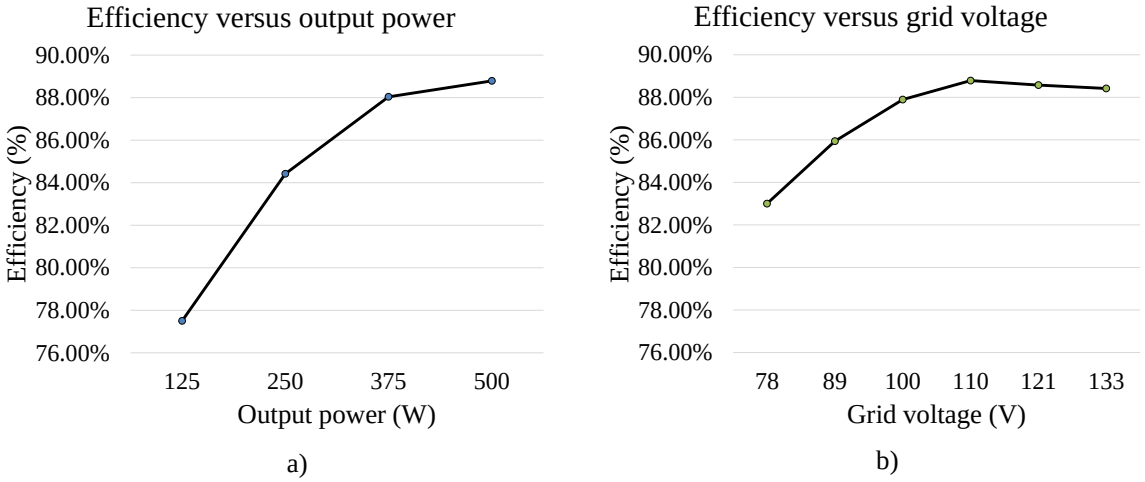
Figure 65 – Experimental results (dynamic response): a) and b) primary and secondary sides variables, respectively, during a step response (0.5 p.u. - 1.0 p.u).



Source: Author.

The converter efficiency variating the output power is presented in Figure 66a. The maximum efficiency obtained for this converter was 88.79% at 500W. Figure 66b[6] shows the efficiency for different input voltages. The maximal efficiency was obtained with nominal voltage (110V).

Figure 66 – Efficiency results: a) efficiency changing output power; b) efficiency changing grid voltage.



Source: Author.

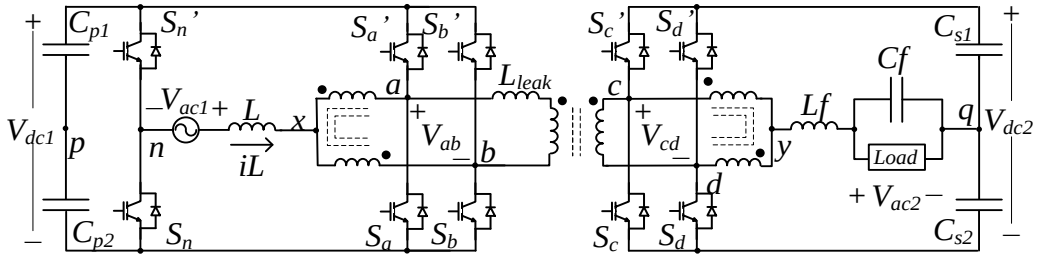
[6] Due to the voltage source current limit, the converter had to be derated to 350 W (78V) and 400W (89V).

7.2 FB-HB

In this topology, depicted in Figure 67, the Full-bridge arrangement is placed on the primary side. This converter is similar to the HB-FB converter presented in the previous section since the same arrangements are used. Therefore, the previous analysis applies to this converter as well.

This converter uses partial actuator in the primary side, which means the output of the secondary side controller is applied to the primary side, reducing the transformer current. As both converters (FB-HB and HB-FB) works similarly, only the simulation results are presented for this converter.

Figure 67 – Asymmetric topology FB-HB.

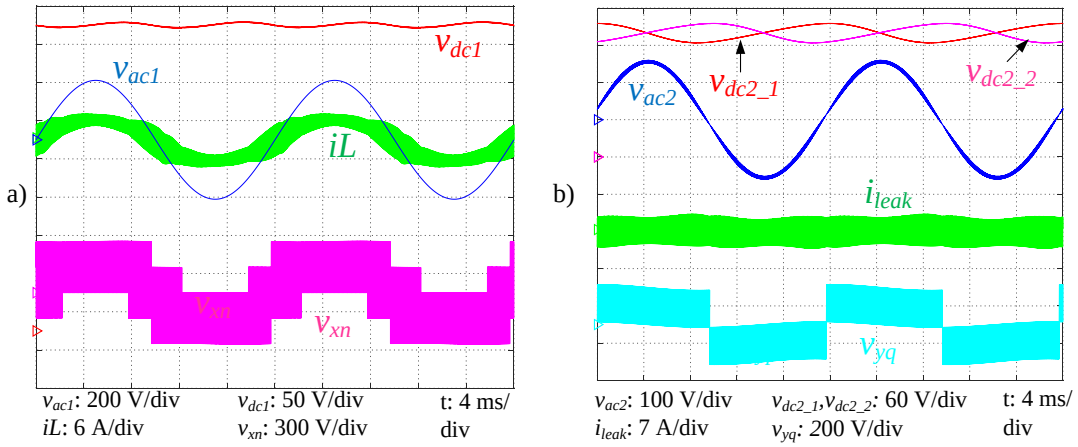


Source: Author.

7.2.1 Simulation results

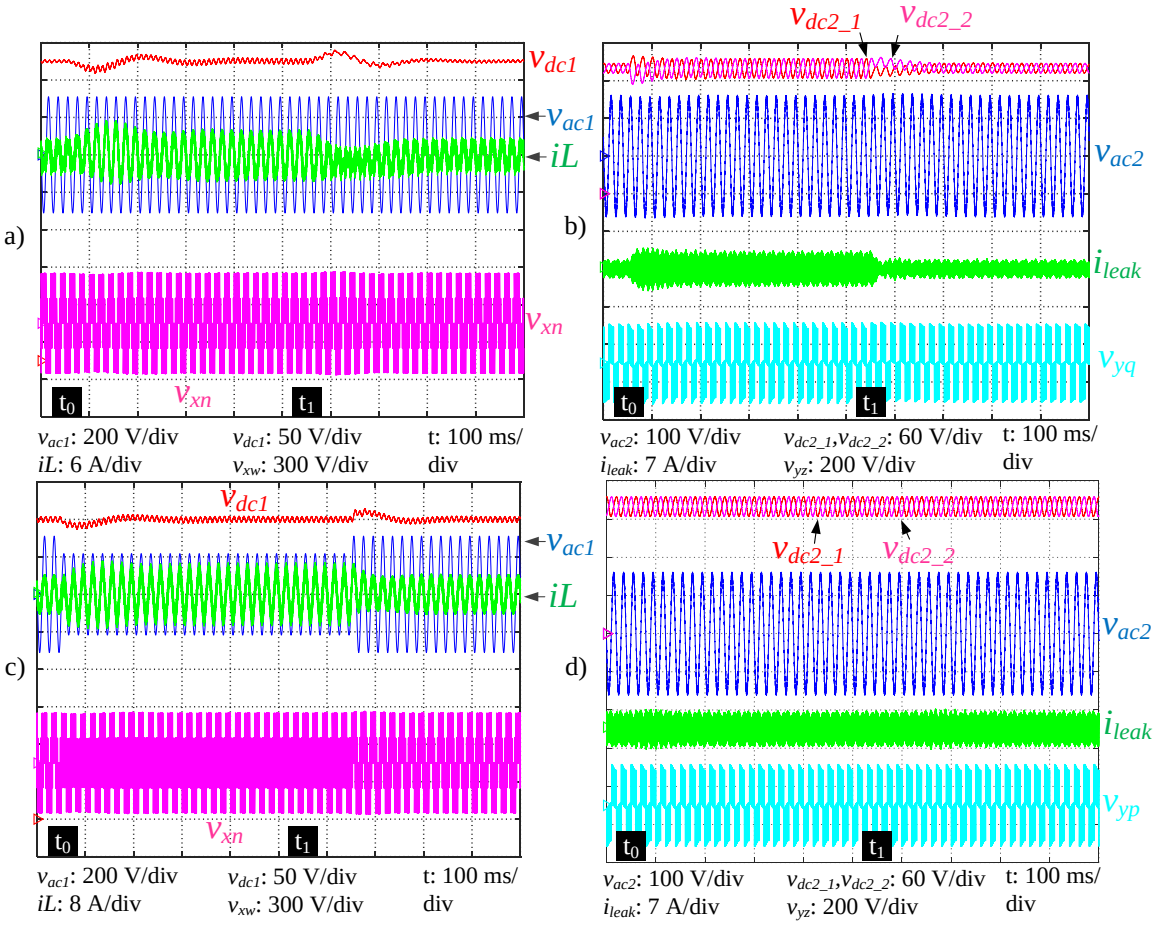
Figure 68 presents the converter at nominal power (0.5kW). Figure 68a shows the primary side variables. Notice the converter input voltage obtained with the high-frequency modulation of the FB arrangement and the obtained input current. The input current THD is 69.6%. Figure 68b shows the secondary side variable. The load voltage is controlled in 110V as well as the DC-link voltage (400V). Following the procedure adopted previously, the converter is submitted to a load step and a voltage sag in order to observe its dynamic response (Figure 69). Figure 69a and Figure 69b shows converter behavior when it is submitted to the load step from 0.5 p.u. to 1.0 p.u. at t_0 and back to 0.5 p.u. at t_1. Notice that both DC-link voltages (primary and secondary) are controlled within 200 ms. The voltage balance between the capacitors of the secondary DC-link is obtained within 100 ms (Figure 69b), although no control method was employed for this purpose. The load voltage is controlled and it is not affected by the load change.

Figure 68 – Simulation results at nominal power: a) converter primary side variables; b) secondary side variables.



Source: Author.

Figure 69 – Simulation results of the FB-HB converter (dynamic response): a) and b) primary and secondary sides variables, respectively, during a step response (0.5 p.u. - 1.0 p.u); c) and d) primary and secondary sides' variables, respectively, during a voltage sag to 0.7 p.u.



Source: Author.

Figure 69c and Figure 69d presents the converter response to a voltage sag to 0.7 p.u. applied to at t_0 and removed at t_1. The voltage sag perturbs the primary DC-link voltage and increases the input current. No voltage perturbation is observed in the secondary side DC-link as well as in the load voltage (v_{ac2}). Notice the transformer current is not affected by the voltage sag because the duty cycle of the secondary side is applied to the primary side.

8 ASYMMETRIC CONVERTERS WITH FULL-BRIDGE AND INTERLEAVED FULL-BRIDGE ARRANGEMENTS

This Chapter presents the asymmetric converters that combine Full-bridge and Interleaved Full-bridge arrangements. Part of the analysis of the FB-IFB and the IFB-FB are presented in previous chapters.

The duty cycle function of the IFB arrangement is the same as the HB arrangement (see Figure 15 and Figure 41). Therefore, I n order to reduce the transformer current, one could apply the duty cycle of the IFB arrangement to the FB arrangement. This strategy was already adopted in Chapter 7, which proposed a new modulation method for the FB arrangement. However, the modulation resulted in high current ripple and poor WTHD for the converter input/output voltage. To avoid such disadvantages, instead of applying the IFB duty cycle function to the FB arrangement, the duty cycle function of the FB arrangement is applied to the IFB arrangement. That means to apply the original low-frequency modulation of the FB arrangement to the IFB.

8.1 FB-IFB

The Full-bridge – Interleaved Full-bridge (HB-FB) topology is presented in Figure 70. Both input and output converter voltages present five-levels. Table 30 shows the converter main voltages according to the switching states for $S_n = 1$.

Table 30 – Main converter voltages (for $S_n = 1$)

Switches state				**Voltages**		
S_e	S_f	S_a/S_c	S_b/S_d	$v_{ab} \mid v_{cd}$	v_{xn}	v_{yz}
0	0	0	0	0	V_{dc1}	0
0	0	0	1	$V_{dc1} \mid V_{dc2}$	$V_{dc1}/2$	$V_{dc2}/2$
0	0	1	0	$-V_{dc1} \mid -V_{dc2}$	$V_{dc1}/2$	$V_{dc2}/2$
0	0	1	1	0	*0*	V_{dc2}
0	1	0	0	0	V_{dc1}	$-V_{dc2}/2$
0	1	0	1	$V_{dc1} \mid V_{dc2}$	$V_{dc1}/2$	*0*
0	1	1	0	$-V_{dc1} \mid -V_{dc2}$	$V_{dc1}/2$	*0*
0	1	1	1	0	*0*	$V_{dc2}/2$
1	0	0	0	0	V_{dc1}	$-V_{dc2}/2$

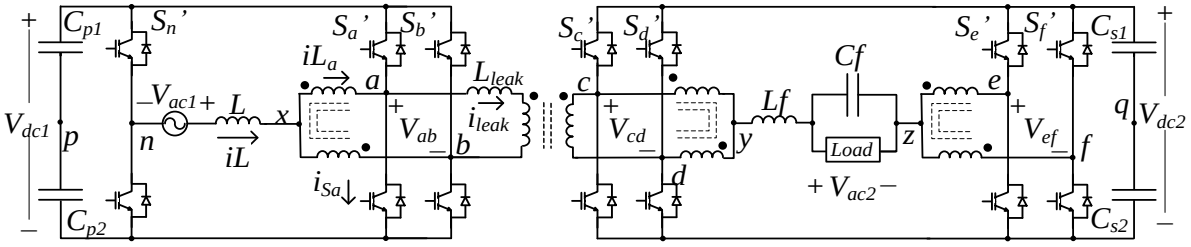
1	0	0	1	V_{dc1} | V_{dc2}	$V_{dc1}/2$	*0*
1	0	1	0	$-V_{dc1}$ | $-V_{dc2}$	$V_{dc1}/2$	*0*
1	0	1	1	0	*0*	$V_{dc2}/2$
1	1	0	0	0	V_{dc1}	$-V_{dc2}$
1	1	0	1	V_{dc1} | V_{dc2}	$V_{dc1}/2$	$-V_{dc2}/2$
1	1	1	0	$-V_{dc1}$ | $-V_{dc2}$	$V_{dc1}/2$	$-V_{dc2}/2$
1	1	1	1	0	*0*	*0*

Source: Author.

8.1.1 Converter modulation

The most important aspects when defining the modulation to be implemented by the converter are the transformer current and the imposed converter input/output voltage. In the previous Chapter, the transformer current was minimized in exchange for a poorer converter input/output voltage. In this chapter, a trade-off solution is adopted resulting in a mid-term performance of these two aspects.

Figure 70 – Asymmetric topology FB-IFB.



Source: Author.

When the natural duty cycle function of the FB and IFB arrangements are applied, each one generates the associated transformer winding voltage. The instantaneous difference between the transformer winding voltages determines the leakage inductance voltage drop and it is directly proportional to the transformer current rate. In order to analyze the transformer windings voltage variation in one grid period, one can compute its mean value of half switching period. Figure 71a shows the mean value of each transformer winding voltage variating in one and a half grid period using the natural duty cycle of each arrangement. The transformer current is as higher as the difference between both values. It is clear that applying the natural duty cycle function would lead to very high transformer currents.

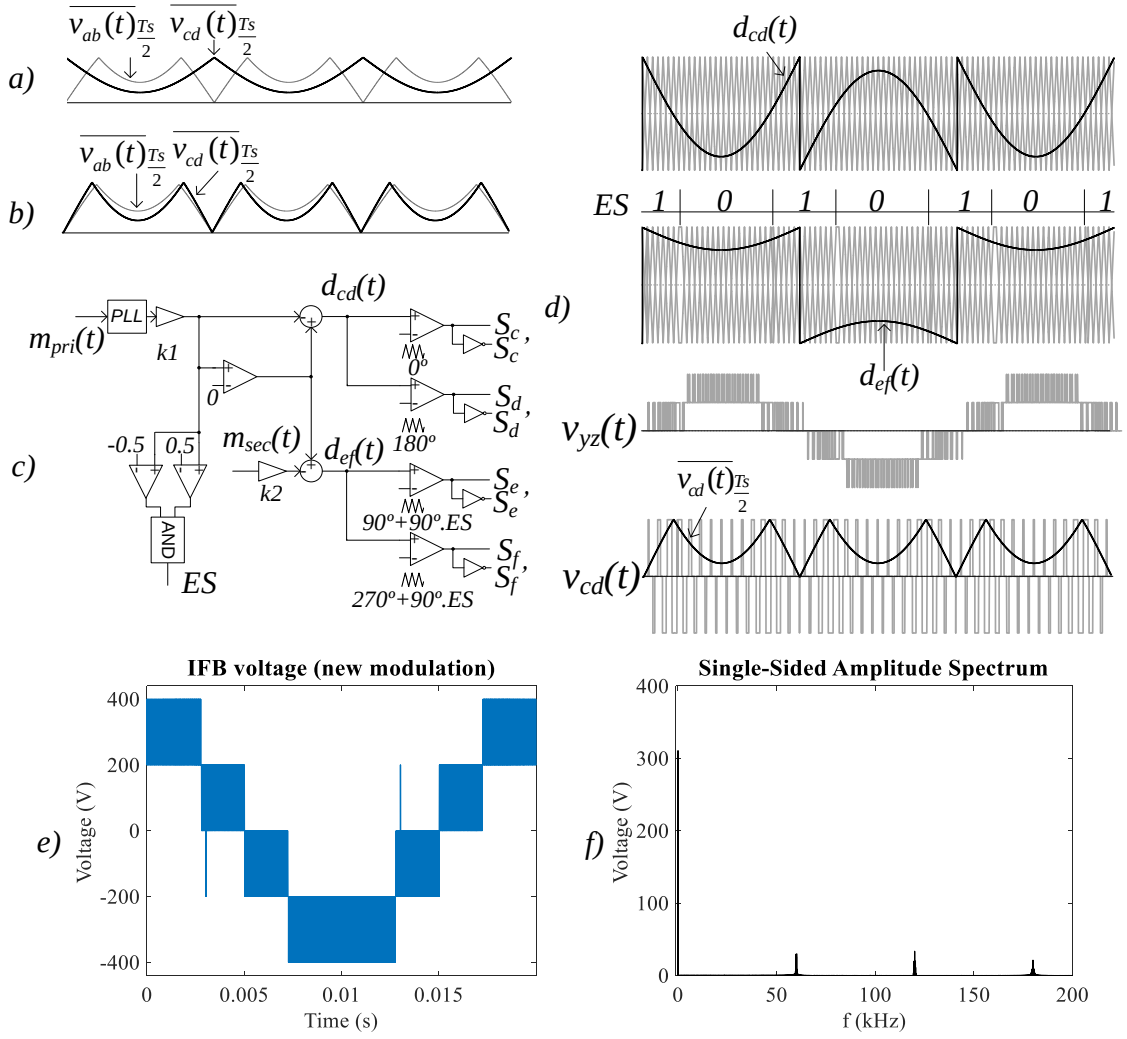
Another solution would be to apply the duty cycle function of the FB arrangement to the IFB arrangement. In this case, the transformer current would be reduced to a minimum. However, the legs ‘e’ and ‘f’ of the secondary side need to be switched in low frequency in order to have a five-level output voltage, which would result in an IFB arrangement working as a FB arrangement. This is not a good approach since the effective converter output frequency would be reduced by a factor of two despite the use of two extra switches and one extra magnetic element (interleaved transformer).

To overcome such problems, the duty cycle function adopted by legs ‘c’ and ‘d’ (M_{cd}) is slightly different from the one applied to the legs ‘a’ and ‘b’ (Figure 71b). In fact, it is defined to be in phase with the duty cycle function applied to the primary side but with a fixed and increased amplitude (satisfies $d_{cd}(t) = S_m - M_{cd}.\sin(\theta)$). This results in a higher transformer current than the minimum but lower than the obtained with the natural duty cycle functions of the arrangements. This can be observed through the difference between medium values of v_{ab} and v_{cd} in Figure 71a (natural duty cycle functions) and Figure 71b (proposed duty cycle function).

The converter output voltage is given by the difference between v_{yq} and v_{zq}. The increased amplitude applied in the construction of v_{yq} needs to be compensated by v_{zq}. In addition, v_{zq} is used to control the load voltage since the secondary side needs to have a partial actuator. Figure 71c presents the employed modulation scheme. The phase of the primary side controller output m_{pri} is obtained through a PLL and its amplitude is set through a constant *k1*. The result is subtracted from the low-frequency signal, obtained with a comparator, to create the secondary duty cycle function d_{cd} (Figure 71d) according to (28). The d_{cd} is applied to the legs ‘c’ and ‘d’ and has a constant amplitude during the operation. In order to decrease the controller effort, the output of the load voltage controller m_{sec} is adapted through a constant *k2*, so that the target modulation index of the load voltage is achieved. Both *k1* and *k2* are adjusted so that when the load voltage is maximum, $Mf2 = d_{cd} - d_{ef}$, where *Mf2* is the modulation index of the load voltage. The result is also subtracted from the low-frequency signal and generates the duty cycle function of the switches ‘e’ and ‘f’ ($d_{ef}(t) = S_m - (M_{cd} - M_{f2}).\sin(\theta)$). To obtain the five-level output voltage v_{yz}, one needs to shift the carriers by 90º when $-0.5 < m_{pri}.k1 < 0.5$. The flag Enable Shift (ES) is used for this purpose and it is presented in Figure 29d.

Figure 71e shows the output voltage obtained through simulation and Figure 71f presents its spectrum. Notice the harmonics are multiple of 60 kHz and the resulting WTHD value is 0.0251.

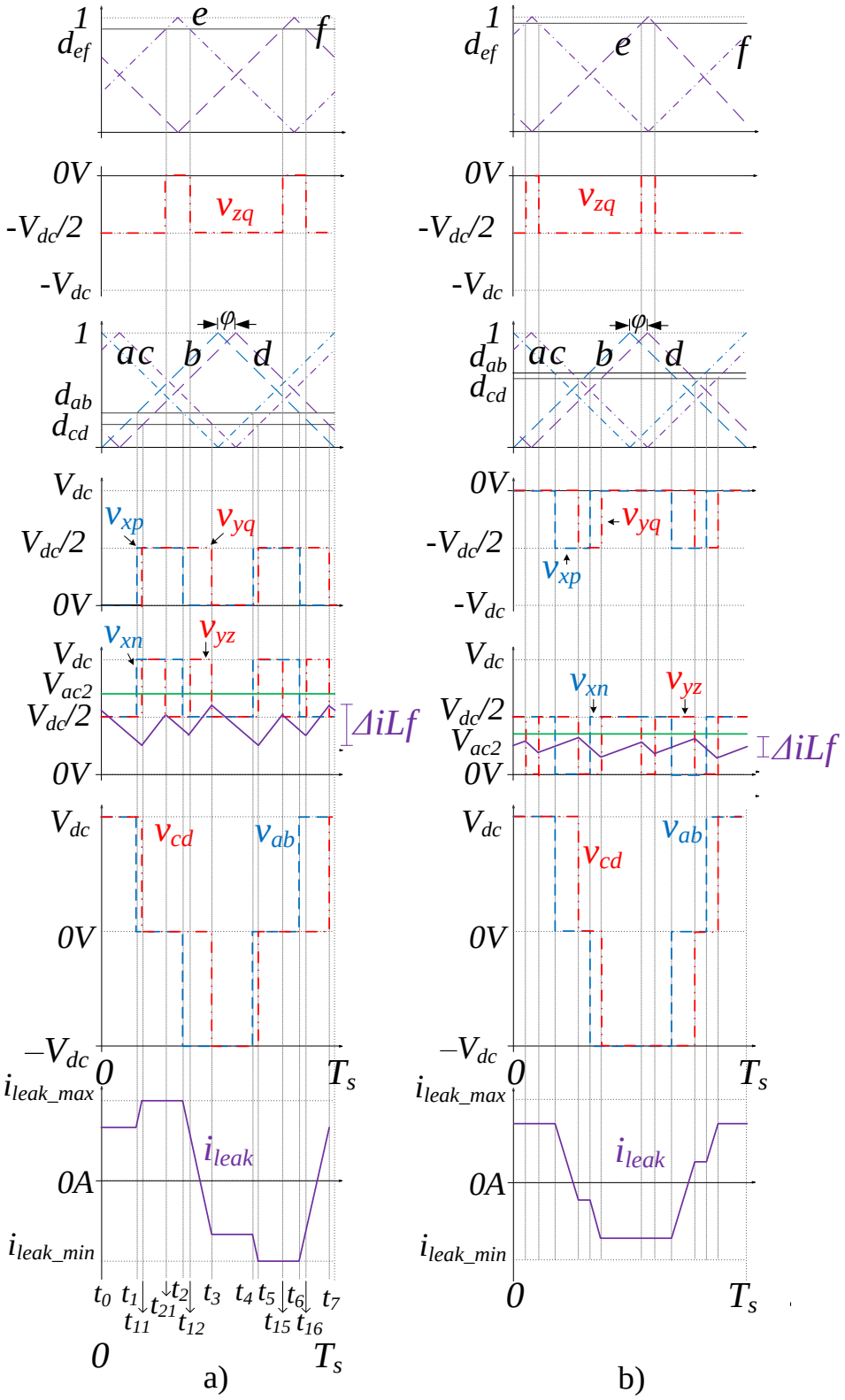
Figure 71 – Modulation of the converter secondary side of the FB-IFB: a) transformer windings mean voltages when the arrangements natural duty cycle function are applied; b) transformer windings mean voltages obtained with the new modulation; c) modulation scheme; d) carriers and duty cycle functions of legs ‘c’, ‘d’, ‘e’ and ‘f’ in addition to the converter output voltage and the v_{cd}.; e) converter output voltage; f) spectrum of the output voltage.



Source: Author.

Figure 72 presents the main converter waveforms for one switching period for a modulation index of 0.7. Figure 72a shows the waveforms for the maximum value of the load voltage. The converter input voltage formation is derived from the FB arrangement and it is the same presented in Chapter 4. The converter output voltage v_{yz} is very similar to the output voltage presented in Chapter 5. Due to the modulation, the voltage pulse distribution is not uniform. In addition, the transformer current waveform is different because of the different duty cycle applied to the primary and secondary sides. Figure 72b presents the same waveforms for an operating point where the carriers ‘e’ and ‘f’ are 90º phase-shifted. The converter output voltage is also non-uniform but presents four pulses in one switching period.

Figure 72 – Modulation of the FB-IFB arrangement with key voltages for (S_n = 1): a) d_{ab} = 0.3, d_{cd} = 0.2 and d_{ef} = 0.9; b) d_{ab} = 0.65, d_{cd} = 0.6 and d_{ef} = 0.95.



Source: Author.

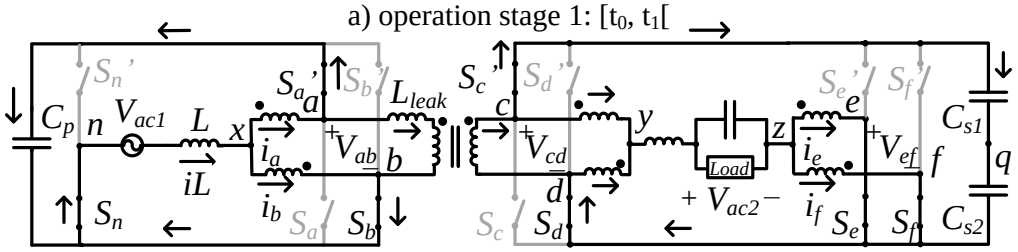
8.1.2 Converter operation

Figure 73 present the operation stages of this converter based on the waveforms depicted in Figure 72a and considering positive current circulating in the grid and in the load. There are twelve distinct time intervals in one switching period but only the first six are presented since the others are similar.

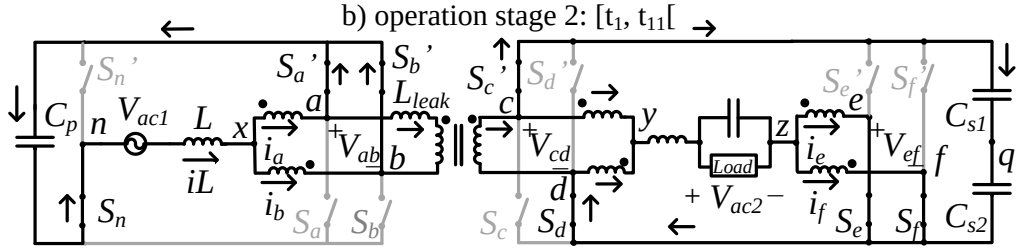
- Operation stage 1 [t_0, t_1[(Figure 73a): the switches S_a and S_c are turned off, which applies half of the DC-link voltage to the converter input and output. The primary and secondary windings of the transformer are submitted to V_{dc1} and V_{dc2}, respectively. The transformer current remains equal to its initial value.
- Operation stage 2 [t_1, t_{11}] (Figure 73b): during this stage the switch S_b is turned off, which short circuit the interleaved transformer of the primary side, imposing the voltage V_{dc1} to the input. The transformer primary winding voltage becomes zero but the voltage in the secondary winding is still V_{dc2}, which increases the current. The converter output voltage remains the same.
- Operation stage 3 [t_{11}, t_{21}[(Figure 73c): the switch S_d is turned off and the converter output voltage becomes the DC-link voltage while the converter input voltage remains the same. Both transformer windings voltages are the same during this stage and transformer current remains constant.
- Operation stage 4 [t_{21}, t_2[(Figure 73d): in this stage, the switch S_e turns off, which sets $V_{dc2}/2$ to the output voltage. The transformer variables and the converter input voltage remain the same.
- Operation stage 5 [t_2, t_{12}[(Figure 73d): in this stage the switch S_a turns on, which makes the converter input voltage $V_{dc1}/2$ again. The output voltage remains the same but the voltage v_{ab} becomes negative ($-V_{dc1}$) while the voltage v_{cd} remains zero. This decrease the transformer current, which becomes negative during this operation stage.
- Operation stage 6 [t_{12}, t_3[(Figure 73d): in this stage, the switch S_e turns on, which sets the converter output voltage to V_{dc2}. The converter input voltage remains the same as well as the transformer variables.

Figure 73 – FB-IFB converter operation: a) operation stage 1; b) operation stage 2; c) operation stage 3; d) operation stage 4; e) operation stage 5; f) operation stage 6.

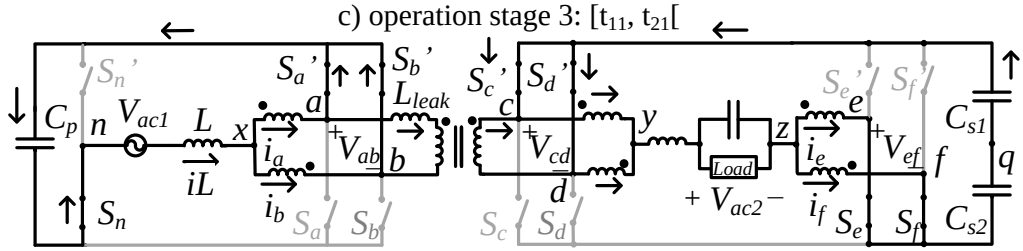
a) operation stage 1: [t_0, t_1[



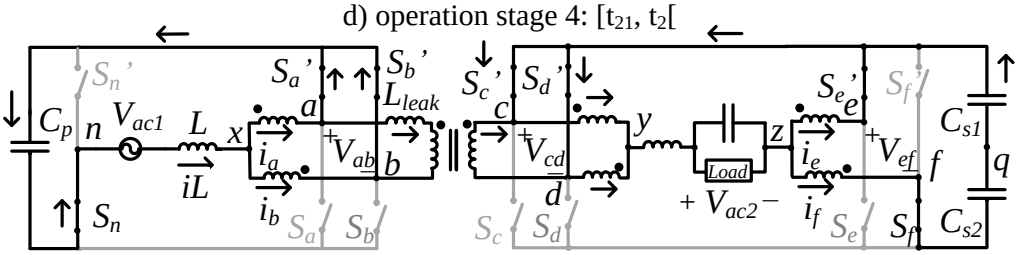
b) operation stage 2: [t_1, t_{11}[



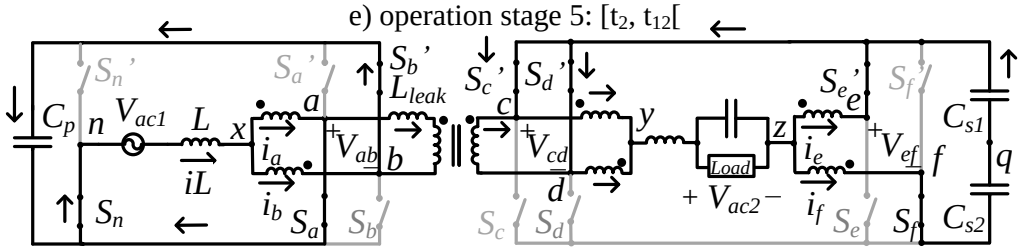
c) operation stage 3: [t_{11}, t_{21}[



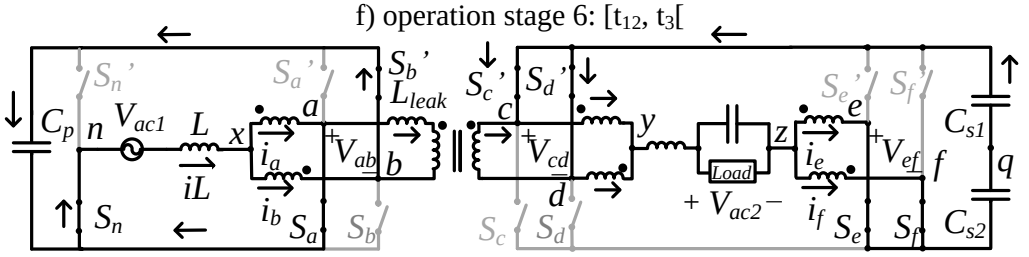
d) operation stage 4: [t_{21}, t_2[



e) operation stage 5: [t_2, t_{12}[



f) operation stage 6: [t_{12}, t_3[



Source: Author.

8.1.3 Current ripple

The current ripple for the FB arrangement is presented in Section 4.2.3. This section presents the current ripple for the IFB arrangement with the proposed modulation, which is determined following the steps presented in Section 3.2.3.

Naming the output filter inductor current *iLf* and considering sinusoidal the load voltage $v_{ac2}(t) = V_{ac2}.\sin(\omega_g.t)$, the current rate is determined as:

$$\frac{diLf(t)}{dt} = \frac{v_{ym}(t) - v_{ac2}(t)}{Lf} \tag{55}$$

Notice from Figure 72a that the current ripple can be calculated during the time interval $\Delta t1$ = [t3, t5]. In Figure 72b, the time interval $\Delta t2_a$ = [t3, t4] can be used. However, when the duty cycle decreases towards 0.5, this time interval becomes smaller than the time segment $\Delta t2_b$ = [t1, t2]. In this case, $\Delta t2_b$ is used to calculate the current ripple.

The time interval $\Delta t1$ can be written as D.Ts, while the converter output voltage is $V_{dc2}/2$. The time interval $\Delta t2_a$ is [D-(1-D)].Ts/2 and the time interval $\Delta t2_b$ is (1-D).Ts. In both cases, the converter output voltage is zero. The current ripple equation is:

$$\begin{aligned} \frac{\Delta iLf_1}{\Delta t_1} &= \frac{V_{dc1}/2 - V_{ac2}}{Lf} \\ \frac{\Delta iLf_2}{\Delta t_{2a}} &= -\frac{V_{ac2}}{Lf} \\ \frac{\Delta iLf_2}{\Delta t_{2b}} &= -\frac{V_{ac2}}{Lf} \end{aligned} \tag{56}$$

Applying d_{cd} to time intervals $\Delta t1$ and $\Delta t2a$ and d_{ef} to time interval $\Delta t2b$, one obtains the following current ripples.

$$\begin{aligned} \Delta iLf_1 &= \frac{V_{dc2}}{2 \cdot fs \cdot Lf} \cdot \left(2 \cdot M_{f2} \cdot \sin(\omega_g \cdot t) - 1\right) \cdot \left(M_{cd} \cdot \sin(\omega_g \cdot t) - 1\right) \\ \Delta iLf_2 &= \frac{V_{dc2} \cdot M_{f2} \cdot \sin(\omega_g \cdot t)}{2 \cdot fs \cdot Lf} \cdot \left(2 \cdot M_{cd} \cdot \sin(\omega_g \cdot t) - 1\right) \\ \Delta iLf_3 &= \frac{V_{dc2} \cdot M_{f2} \cdot \sin^2(\omega_g \cdot t)}{fs \cdot Lf} \cdot \left(M_{f2} - M_{cd}\right) \end{aligned} \tag{57}$$

Where M_{f2} is the modulation index of the converter output voltage. The angle where the current ripple changes from $\Delta iLf2$ to $\Delta iLf3$ is found making both ripples equal and it is given by $\theta 2 = \sin^{-1}\left(1 / \left[2 \cdot (2 \cdot M_{cd} - \mathrm{M}_{f2})\right]\right)$.

Considering the positive cycle and S_m = 1, the current ripple is:

$$\Delta iL = \begin{cases} \frac{V_{dc2}\cdot M_{f2}\cdot \sin(\omega_g\cdot t)}{2\cdot fs\cdot Lf}\cdot\left(2\cdot M_{cd}\cdot\sin(\omega_g\cdot t)-1\right) & if \quad 0\le \omega_g\cdot t<\theta 2 \\ \frac{V_{dc2}\cdot M_{f2}\cdot \sin^2(\omega_g\cdot t)}{fs\cdot Lf}\cdot\left(M_{f2}-M_{cd}\right) & if \quad \theta 2\le \omega_g\cdot t<\theta 1 \\ \frac{V_{dc2}}{2\cdot fs\cdot Lf}\cdot\left(2\cdot M_{f2}\cdot\sin(\omega_g\cdot t)-1\right)\cdot\left(M_{cd}\cdot\sin(\omega_g\cdot t)-1\right) & if \quad \theta 1\le \omega_g\cdot t<\pi-\theta 1 \\ \frac{V_{dc2}\cdot M_{f2}\cdot \sin^2(\omega_g\cdot t)}{fs\cdot Lf}\cdot\left(M_{f2}-M_{cd}\right) & if \quad \pi-\theta 1\le \omega_g\cdot t<\pi-\theta 2 \\ \frac{V_{dc2}\cdot M_{f2}\cdot \sin(\omega_g\cdot t)}{2\cdot fs\cdot Lf}\cdot\left(2\cdot M_{cd}\cdot\sin(\omega_g\cdot t)-1\right) & if \quad \pi-\theta 2\le \omega_g\cdot t<\pi \end{cases} \tag{58}$$

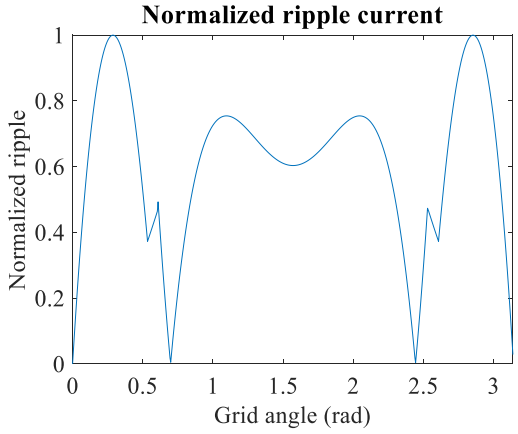
Where $\theta 1=\sin^{-1}\left(1/(2\cdot M_{f2})\right)$.

The maximal current ripple is:

$$\Delta iLf \underset{\omega_g\cdot t=\theta_{\max}}{\le} \frac{M_{f2}\cdot V_{dc2}}{16\cdot fs\cdot L\cdot M_{cd}} \tag{59}$$

Where $\theta_{\max}=\sin^{-1}\left(1/(4\cdot \mathrm{M}_{cd})\right)$. Figure 74 shows the variation of (58) per unit.

Figure 74 – Per unit current ripple variation with the grid.



Source: Author.

8.1.4 Transformer power flow

The transformer is modeled following the same procedures found in Section 3.3. The proposed modulation applies different duty cycle function to each side of the transformer, which modifies the transformer power flow. Considering $d_{ab} = S_n - Mf1.\sin(\omega_g.t)$, $d_{cd} = S_m - M_{cd}.\sin(\omega_g.t)$ and (22) one obtains the mean power varying with time.

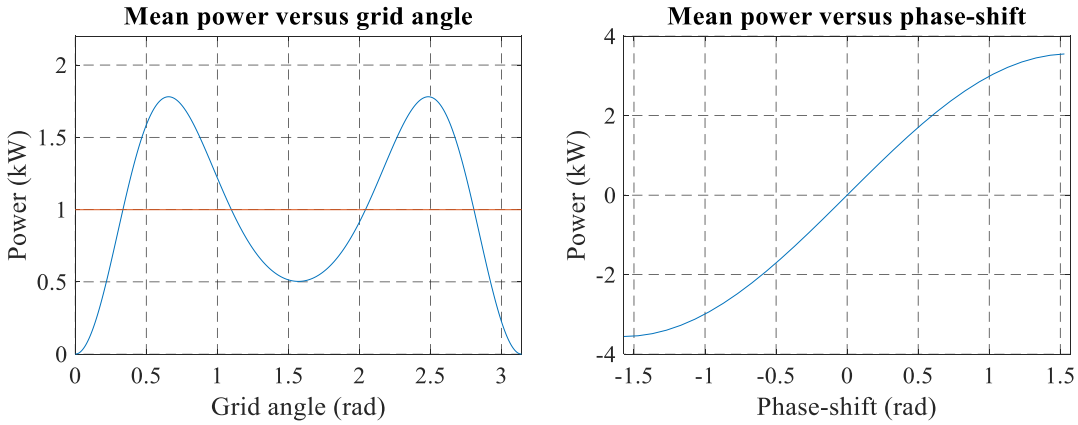
$$P_{fb-ifb}\left(\omega_g \cdot t, \varphi\right) = \frac{8 \cdot N \cdot V_{dc1} \cdot V_{dc2} \cdot \sin(\varphi)}{\pi^2 \cdot L_{leak} \cdot \omega_s} \cdot \sin(\pi \cdot \mathrm{M}_{f1} \cdot \sin(\omega_g \cdot t)) \cdot \sin(\pi \cdot \mathrm{M}_{cd} \cdot \sin(\omega_g \cdot t)) \quad (60)$$

The mean power transferred in one grid period is given by:

$$P_{mean\_\mathrm{fb-ifb}}\left(\varphi\right) = \frac{1}{\pi}\int_0^{\pi} P_{fb-ifb}\left(\omega_g \cdot t, \varphi\right) d\omega_g t \quad (61)$$

Figure 75 presents the power flow variation with the grid phase and with the phase-shift. Figure 75a is determined using (60) for φ = 0.28 (16.3º) while Figure 75b is determined using (61).

Figure 75 – Example of power flow variation for FB-IFB converter with V_{dc1} = V_{dc2} = 400V, fs = 30 kHz, M_{f1} = 0.778, M_{cd} = 1.1.M_{f1} and L_{leak} = 108 µH, for 1000W mean power: a) according to the grid voltage θ for φ = 0.28 (16.3º) showing the mean value in one grid period (straight line); b) according to the phase-shift.



a) b)

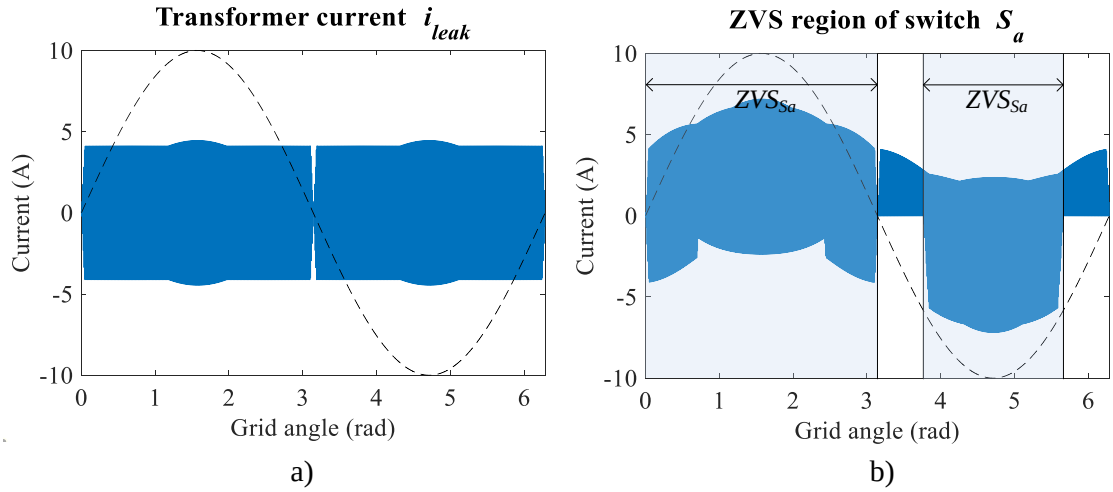
Source: Author.

8.1.5 ZVS analysis

As observed in Figure 71d, the duty cycle waveform applied to the transformer's windings is the same applied to the SFB converter. However, the modulation applied in the FB-IFB creates a small difference between d_{ab} and d_{cd}, which increases the transformer current. Therefore, the ZVS region is also modified. The transformer current obtained with the proposed modulation during one grid period is presented in Figure 76a (with the grid voltage reference).

In addition, the transformer current waveform during one switching period is presented in Figure 72a and Figure 72b. Notice in Figure 76a that the transformer current is higher in the region near the maximum and minimum of the grid voltage, which corresponds to the region with the highest difference between d_{ab} and d_{cd}. The Figure 76b shows the switch current, the grid voltage reference and the ZVS regions, which are longer (5.03 rad – 288º) than the obtained with the SFB, showing the impact of the transformer current in the ZVS regions size.

Figure 76 – Transformer and switch current of converter FB-IFB: a) transformer current and the grid voltage reference; b) grid voltage reference, current in switch and the associated ZVS regions.



Source: Author.

8.1.6 Losses estimation

For this converter, it was assumed a nominal power of 750W. For this reason, the power losses estimation were determined for this operation point.

8.1.6.1 Conduction and switching losses determination

The leg ‘n’ of the Full-bridge arrangement employed the SCT3030AL SiC switches, while the other legs used the SCT3120AL. Table 31 presents the conduction and switching losses obtained with the simulation software PLECS® and datasheet information.

Table 31 – Losses of the FB-IFB converter with SCT3120AL and SCT3030AL switches.

Losses	**Value**
Conduction losses	13.59 W
Switching losses	10.88W
Total losses	**24.48 W**

Source: Author.

8.1.6.2 Magnetic devices losses

The estimated transformer losses are the same observed in the Symmetric Half-bridge converter. The input inductor losses estimation if obtained from the Half-bridge arrangement, while the output inductor is calculated with Steinmetz equation. The interleaved transformer losses are the same obtained in Section 6.1.3. The summary of the magnetic losses is presented in Table 32.

Table 32 – Magnetic devices losses.

Device	**Losses value**
Input/output inductor	3.06 W / 5.44 W
Input/output interleaved transformer	2.99 W / 2x2.99 W
Transformer	4.94 W
Total	**22.41 W**

Source: Author.

8.1.6.3 Electrolytic capacitor losses

The layout of both DC-link capacitors is the same used by the other converters. The resulting currents in both DC-link are very similar same and they generate the same losses for both DC-links. The overall estimated losses for both DC-links considering 750W of nominal power is 1.1W.

Table 33 – Capacitor losses estimation.

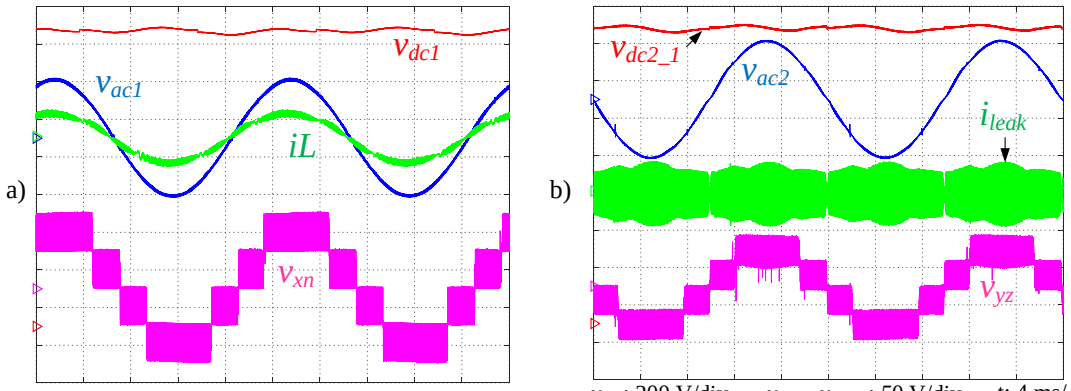
Capacitor	**RMS current value**	**Estimated ESR value**
Series associated capacitor	0.47 A @ 100 Hz	0.351 Ω
	0.30 A @ 200 Hz	0.234 Ω
	0.64 A @ 60 kHz	0.012 Ω
Parallel associated capacitor	1.32 A @ 100 Hz	0.351 Ω
	0.85 A @ 200 Hz	0.234 Ω
	1.11 A @ 60 kHz	0.012 Ω

Source: Author.

8.1.7 Experimental results

Figure 77 presents the FB-IFB converter operating at 0.75 kW with M_{cd} = 0.85. The grid voltage and the input current are in phase and have a power factor of 0.994 with a current THD of 9.89% (Figure 77a). Both DC-link voltages are controlled in 400V as presented in Figure 77a and Figure 77b. Figure 77b also shows the transformer current i_{leak}, which differs from the obtained by SFB converter presenting an increased value during the peak values o voltage grid voltage, which results in higher currents. The load voltage v_{ac2} is sinusoidal, controlled in 220V and presents THD of v_{ac2} is 2.23%.

Figure 77 – Experimental results (FB-IFB) at nominal power (0.75 kW): a) converter primary side variables; b) secondary side variables.

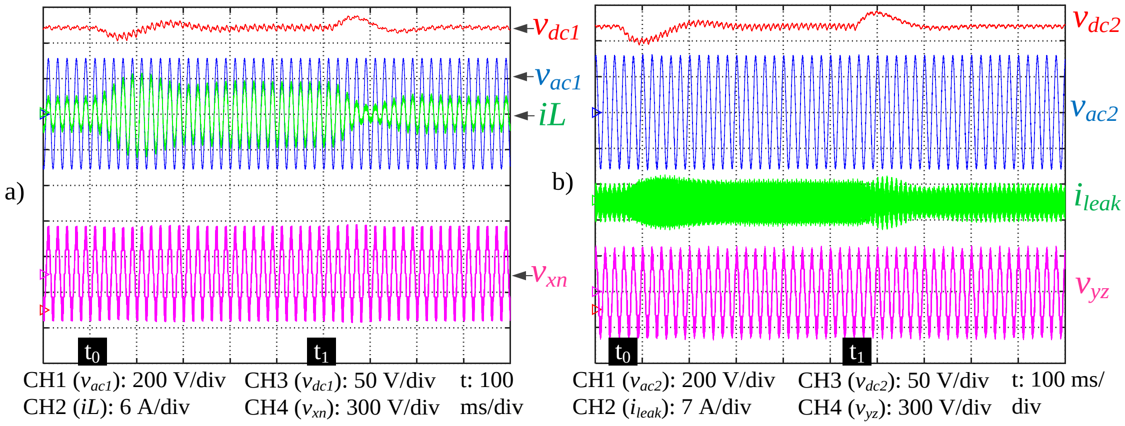


Source: Author.

Figure 78 presents the dynamic response of the converter to a load step from 0.5 p.u. to 1.0 p.u. at t_0 and back to 0.5 p.u. at t_1. Notice the increase in the input current caused by the increased load (Figure 78a). Figure 78b shows the dynamic of the secondary side variables. Notice that the converter output voltage is not affected by the load change.

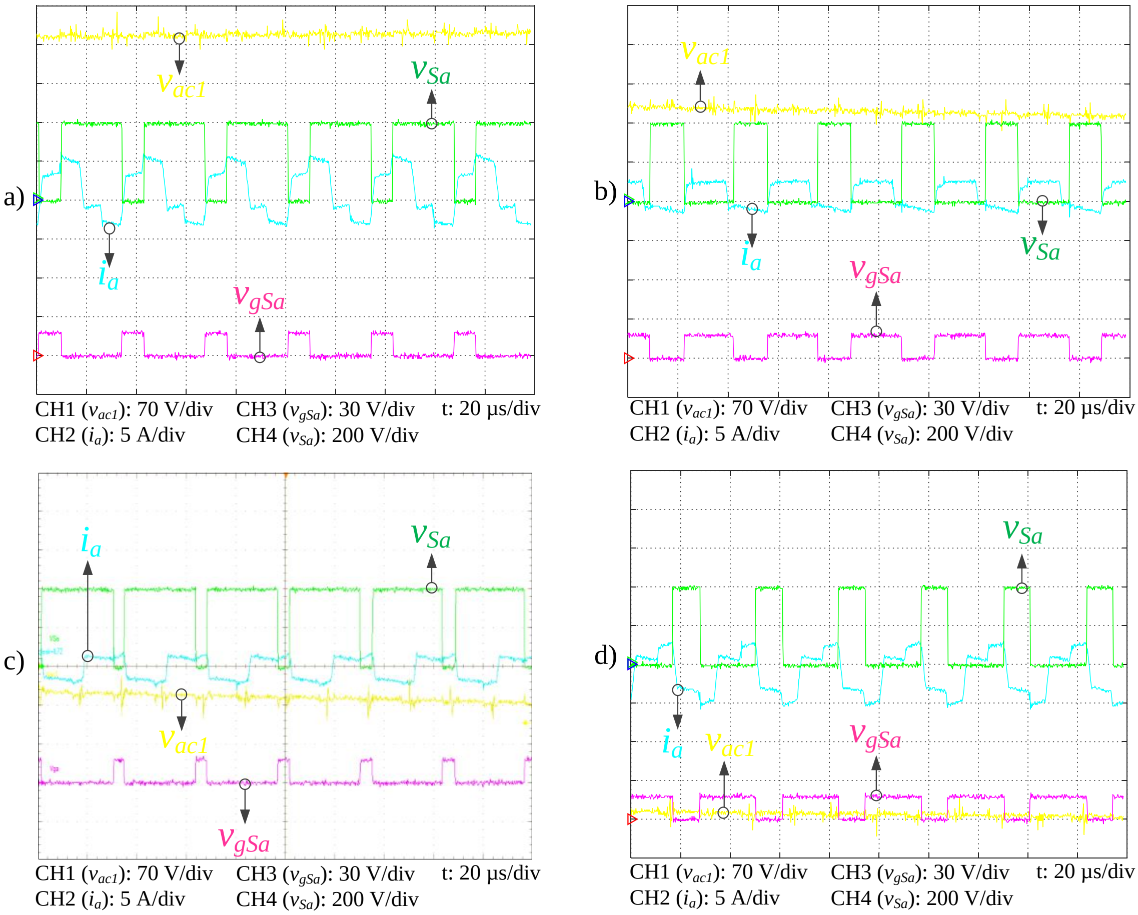
Figure 79 presents the ZVS region analysis of the switch Sa. The grid voltage, the switch voltage, and the gate signal and the node current ‘a’ are presented. Figure 79a shows the switch operating inside the ZVS region with a positive grid voltage. Figure 79b shows that the switch keeps operating inside the ZVS region with a smaller grid voltage. In Figure 79c, the grid voltage becomes negative and the switch operates outside the ZVS region. When the grid voltage decreases more, (Figure 79d) the switch operates once more inside the ZVS region.

Figure 78 – Experimental results (dynamic response) of the FB-IFB converter: a) and b) primary and secondary sides variables, respectively, during a step response (0.5 p.u. - 1.0 p.u).



Source: Author.

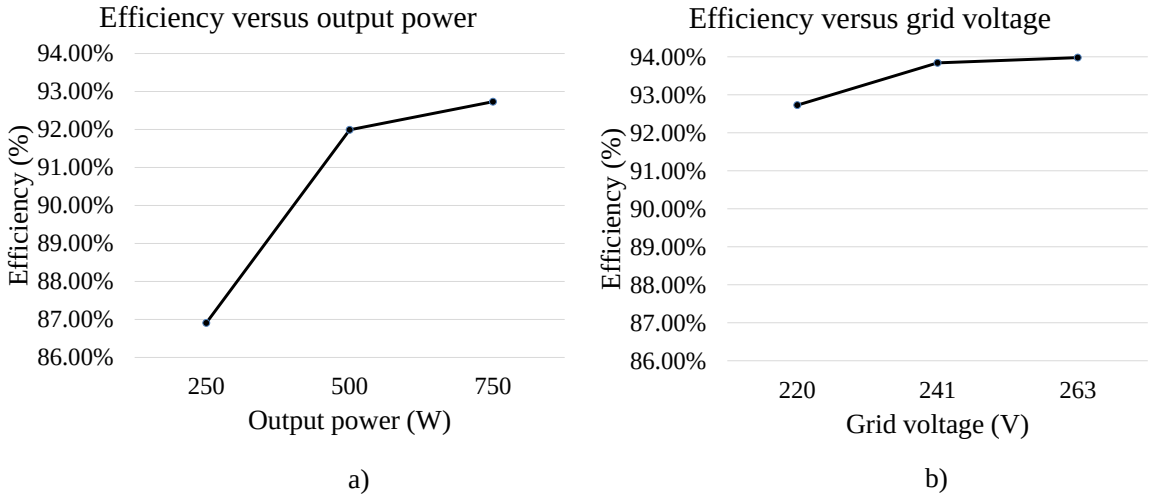
Figure 79 – Switching characteristics of S_a with the grid voltage, the switch voltage and gate signal and the node 'a' current: a), b) and d) converter operating inside the ZVS region; c) converter operating outside the ZVS region.



Source: Author.

The converter efficiency variating the output power with nominal grid voltage is presented in Figure 80a with maximum efficiency of 92.73% obtained at 750W. Figure 80b shows the efficiency for different input voltages. The maximal efficiency of 93.98% was obtained with nominal voltage (263V).

Figure 80 – Efficiency results: a) efficiency changing output power; b) efficiency changing grid voltage.

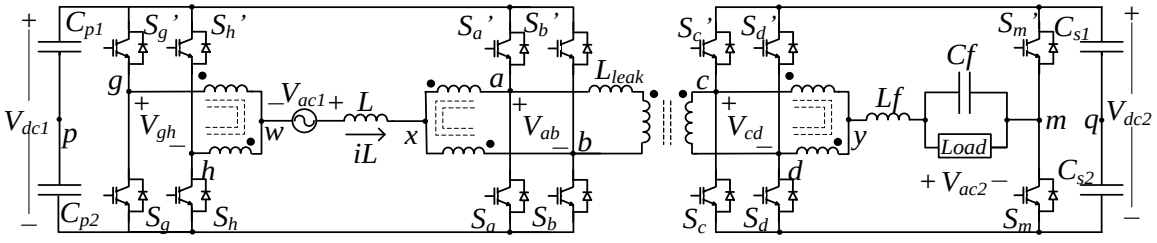


Source: Author.

8.2 IFB-FB

The FB-IFB topology is depicted in Figure 81. In this topology, the Full-bridge arrangement is placed on the secondary side while the Interleaved Full-bridge arrangement is moved to the primary side. Since the same arrangements of the FB-IFB converter are used, the analysis is similar and only the simulation results are presented for this converter.

Figure 81 – Asymmetric topology FB-IFB.



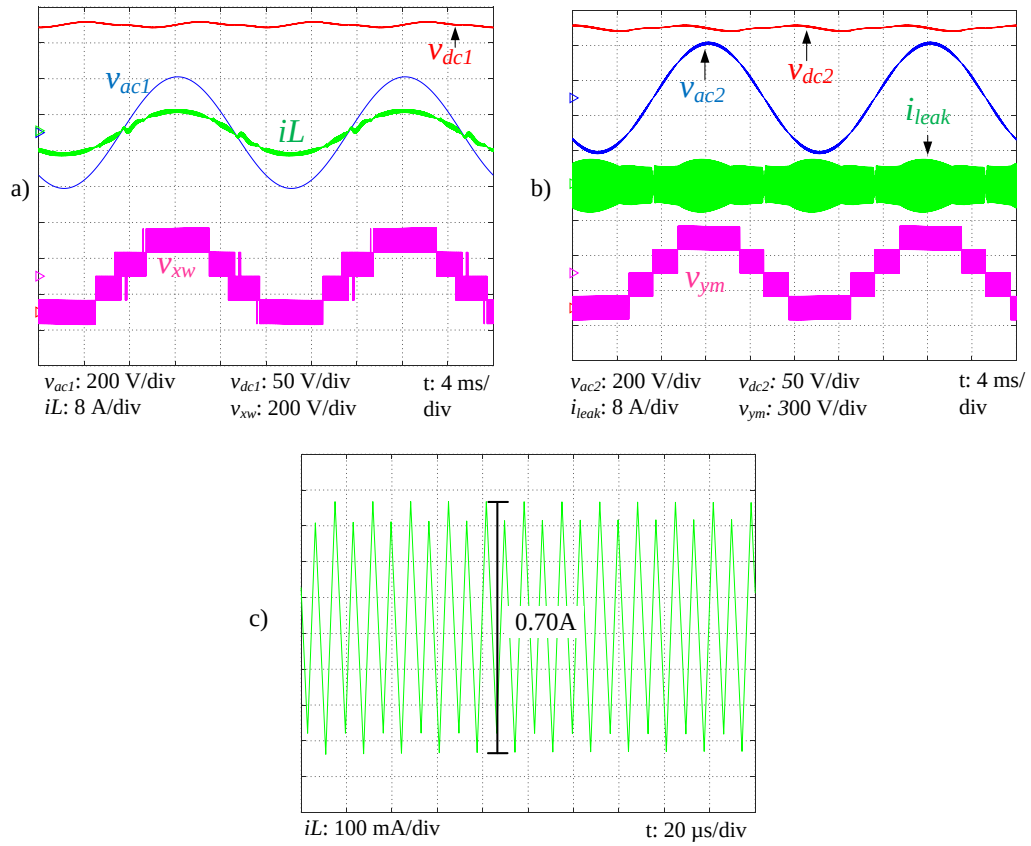
Source: Author.

8.2.1 Simulation results

Figure 82 presents the simulation results of the converter working at 750W with a fixed M_{ab} of 0.88. Figure 82a shows that the converter input voltage presents five-levels. The input current and grid voltage are in phase with a power factor of 0.999. The THD of the input current is 3.80%. Figure 82b shows sinusoidal controlled load voltage with a THD of 1.25%. The secondary side DC-link is also controlled in 400V. In addition, one observes the transformer current with the same waveform obtained in the experimental results. Figure 82c shows the input current ripple at π/2, which present the same waveform of Figure 28a. The obtained current ripple from (58) at this time instant is 0.695, which is very similar to the obtained in simulation.

Figure 83 presents the converter dynamic response to a load step and a voltage sag, which occurs with the same intensities and at the same time instants as specified for the previous

Figure 82 – Simulation results at nominal power: a) converter primary side variables; b) secondary side variables.

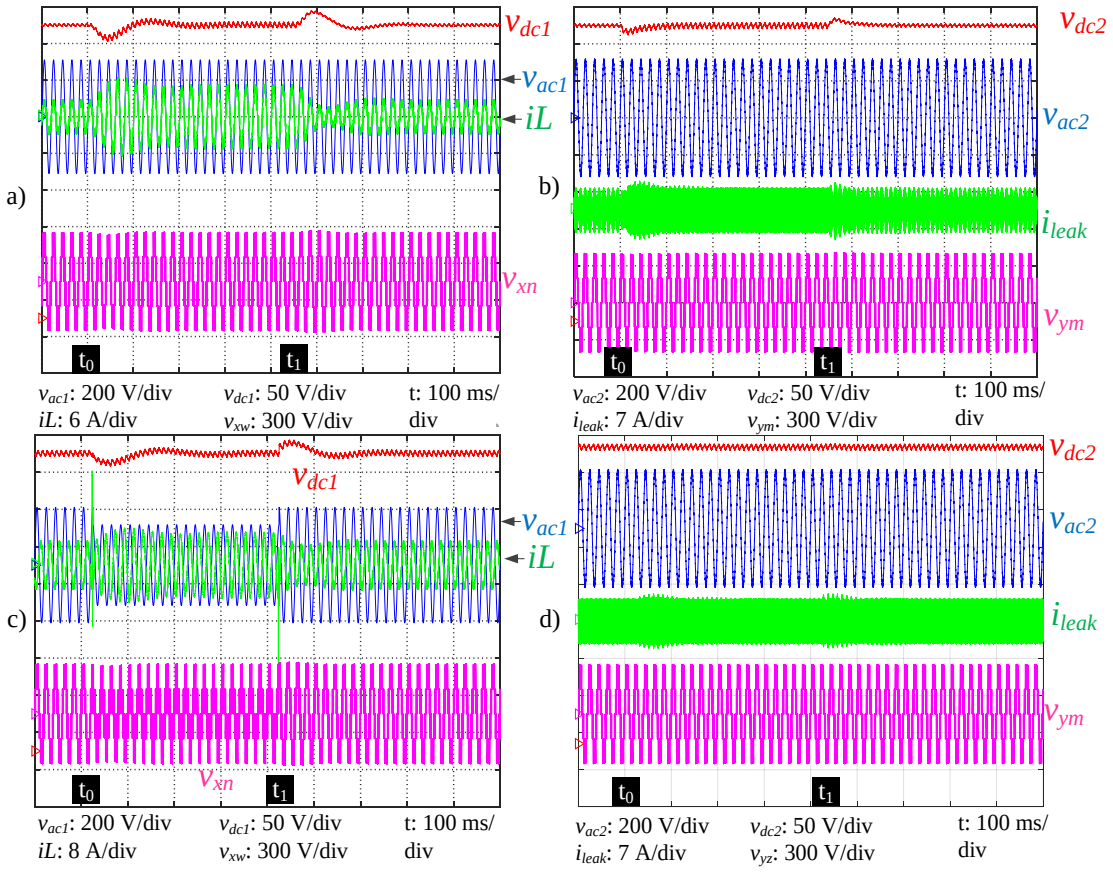


Source: Author.

converters. Figure 83a presents the primary side variables. Notice the increase in the input current in response to the load increase. The perturbation on the DC-link voltage is controlled within 200ms. Figure 83b shows the secondary side variables. The perturbation of the DC-link voltage is controlled in less than 200ms and it does not affect the load voltage. The transformer current increases due to the load increase.

Figure 83c presents the response to the voltage sag. Notice the increase of the input current due to the grid voltage reduction. The disturbance on the DC-link voltage is controlled within 200ms. Figure 83d presents the secondary side variables dynamics. The voltage sag does not disturb the DC-link voltage and the load voltage. Notice due to the similar duty cycles applied to both sides of the transformer, its current remains unchanged within the voltage sag event.

Figure 83 – Simulation results of the IFB-FB converter (dynamic response): a) and b) primary and secondary sides variables, respectively, during a step response (0.5 p.u. - 1.0 p.u); c) and d) primary and secondary sides variables, respectively, during a voltage sag to 0.7 p.u.



Source: Author.

9 MAGNETIC INTEGRATION

As presented in the former Chapter 4, the converters of the proposed family can have many magnetic elements. According to Figure 26, the SFB converter presents the following list of magnetic elements:

- 2 coupled inductors (interleaved transformers): CI-ab and CI-cd.
- 2 low-frequency filter inductors: *L* and *Lf*
- 1 transformer: T
- 1 energy transfer inductor: L_{leak}

Each element can be manufactured in its own core, which would lead to six different magnetic devices. Integrating more than one magnetic element into a single core could bring advantages in terms of volume and losses.

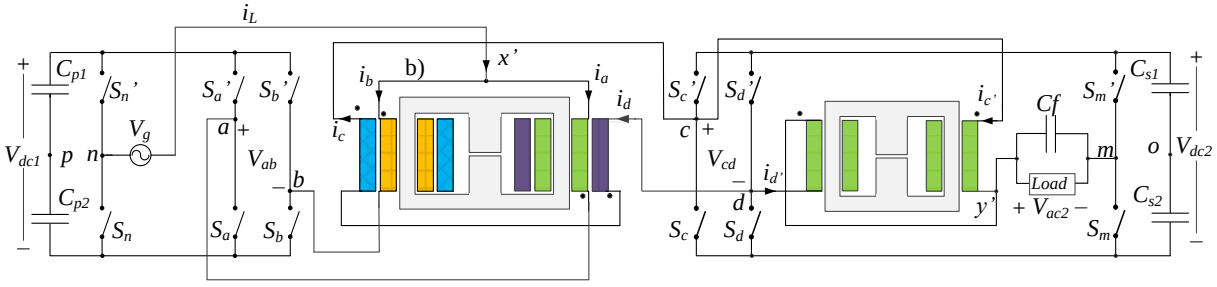
The first integration to perform is to manufacture the energy transfer inductor L_{leak} with the isolation transformer. This can be performed by adjusting the leakage inductance of the transformer to be equal to L_{leak}. To achieve such a goal one can select between different winding arrangements as will be further explained.

The second integration is to manufacture the low-frequency inductor together with the coupled inductor, into a single core. The third integration puts both previous integrations into a single core. This means that one core has one coupled inductor, a low-frequency inductor, a transformer, and an energy transfer inductor.

This chapter presents how these integration steps can be performed in order to obtain the Symmetric Full-bridge converter with only two magnetic devices as presented in Figure 84.

The following assumptions are made in this chapter: the DC voltages are constant, the same duty cycle is applied to both sides of the converter and the dead time is not considered.

Figure 84 – Connection of the integrated magnetics with the Symmetric Full-bridge converter.



Source: Author.

9.1 Transformer leakage inductance[7]

The integration of the energy transfer inductor with the transformer is performed adjusting the transformer's leakage inductance which depends mainly on the window area (which depends on the core) and on the winding arrangement. There are three basic types of winding arrangements, also listed in (KLEEB, 2016), from which one can obtain higher or lower leakage inductance for the same core. The arrangements are presented in Figure 85 and are organized from the bottom (interleaved arrangement - Figure 85f) which usually provides the smaller leakage values to the top (top-bottom arrangement) which provides the highest values. Figure 85b presents the side-side arrangement in which leakage values lie between the top-bottom and the interleaved arrangement. Figure 85e presents a combination of interleaved and side-side arrangement.

A fine-tune adjustment of the leakage can be performed by changing the displacement between the windings or introducing ferromagnetic elements between then (KATS; IVENSKY; BEN-YAAKOV, 1997) as presented in Figure 85c so that more energy can be stored in these spaces increasing the leakage inductance. The leakage inductance can also be further increased using two different cores as presented in Figure 85d, where the leakage value is determined by the gap of the second core.

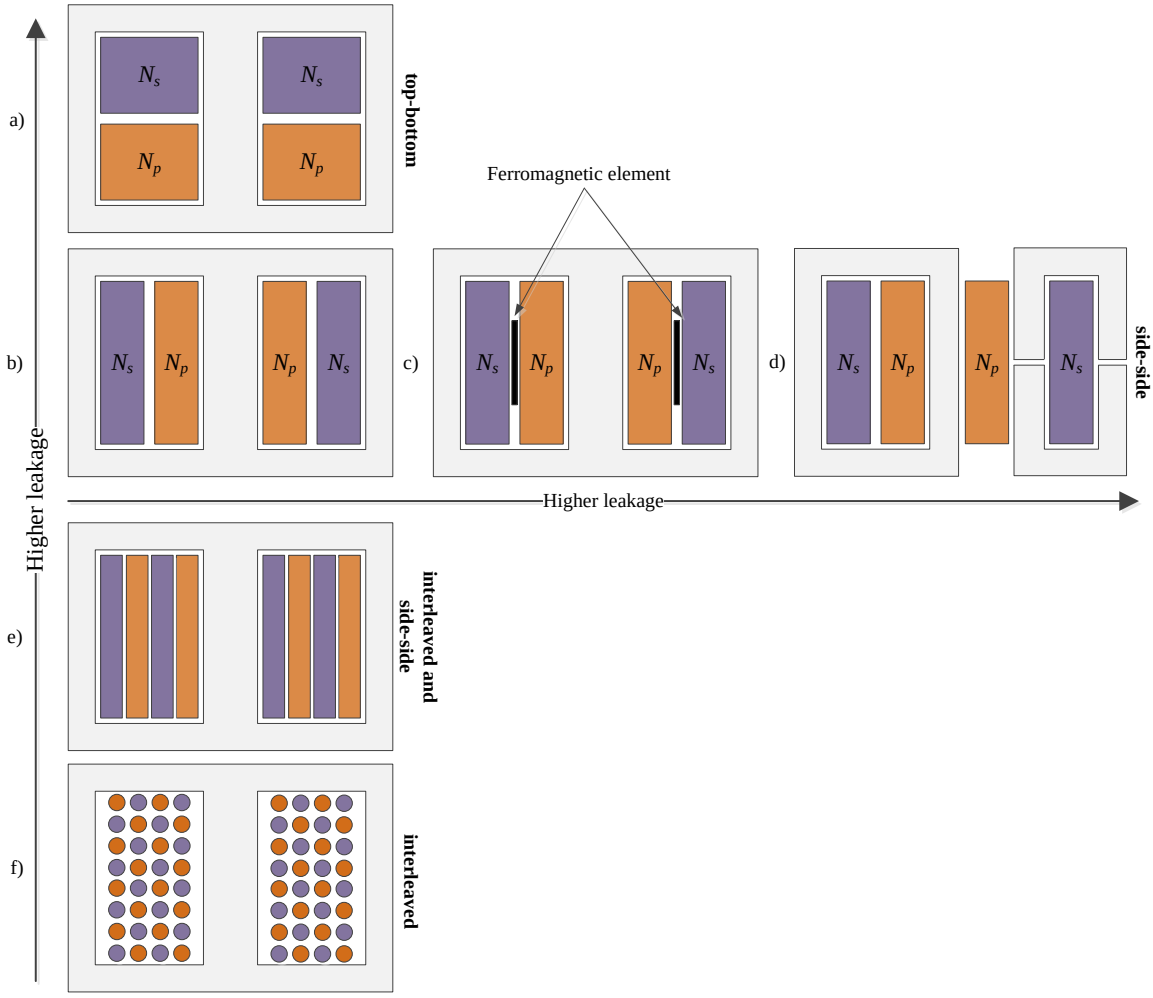
There are three approaches to design a transformer with custom leakage inductance: experimental, FEM simulation and analytical estimation. The experimental approach is based on empirical knowledge and try and error. It may take a few interactions until an approximate target value is obtained. FEM simulations usually lead to very accurate results but it may be time-consuming for complex models. Analytical estimation is not as accurate as FEM simulation but can result in approximate values and is usually easy to perform. One example is the formula presented by (DOEBBELIN; LINDEMANN, 2010) which can estimate the leakage inductance for symmetric windings arrangement.

9.2 Integrated magnetic design

The most common and traditional approach to model magnetic circuits is the reluctance-resistance analogy (e.g. Figure 86). Based on this analogy, variables defined in

[7] Based on Appendix V of (KLEEB, 2016).

Figure 85 – Winding arrangements for E-core and a general view of the achievable leakage intensities: a) top-bottom; b) side-side; c) side-side with ferromagnetic element; d) side-side with two cores; e) interleaved and side-side; f) interleaved.

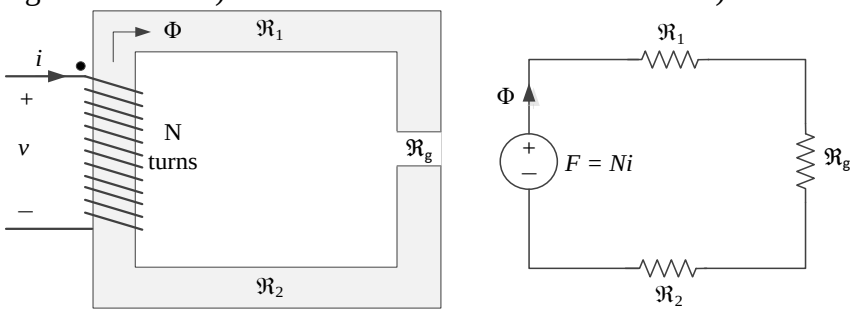


Source: Based on (KLEEB, 2016), (ZACHARIAS, 2020) and modified.

magnetic circuits (Figure 86a) has a counterpart in an equivalent electric circuit (Figure 86b). Magnetomotive force (mmf) F, is equivalent to voltage (v) and magnetic flux (Φ) is equivalent to current (i). For linear materials, the reluctance ($\Re$) is then equivalent to the resistance (R) in an electric circuit. Even the definition of resistance ($R = l/(\sigma A)$) and reluctance ($\Re = l/(\mu A)$) are closely related where A and l are respectively the cross-section area and the path length for both magnetic and electric materials, μ is the magnetic permeability and σ is the electric conductivity. The Ohm's law is also valid relating its magnetic counterparts (mmf, flux, and reluctance) in the magnetic circuit.

Due to its simplicity, it is often used to design magnetic elements such as inductors, coupled inductors, transformers, etc. (WITULSKI, 1995). Although the reluctance-resistance

Figure 86 – Magnetic circuit a) and the reluctance-resistance model b).



a) b)

Source: Author.

analogy is straightforward to understand and reflects directly the geometry of the magnetic element, it cannot be directly used to simulate the interactions between electrical and magnetic devices in power electronics circuit, because magnetic devices store energy instead of dissipating energy as the resistor model would do. One can then, convert the reluctance model in an inductor model using the duality principle as presented in (LUDWIG; EL-HAMAMSY, 1991) (CHERRY, 1949).

Because the resistances do not store energy as a magnetic element, there is no direct connection between the reluctance-resistance model and the physical world. Moreover, as noted by (HAMILL, 1993), the product of the chosen effort variable *F* (mmf given in Ampère) and the flow variable Φ (flux given in Volt.second) results in energy (A.V.s = J). This differs from other systems (electric, hydraulic, mechanical) where the product of effort and flow variables results in power.

Instead of using the reluctance model, one can use of the approach presented in (YAN; LEHMAN, 2005) which employs gyrators and capacitors to model the magnetic element allowing its integration with the electrical circuit.

The approach adopted in this work to design and simulate the integrated magnetics also makes use of gyrators but employs inductors as the storage elements. This approach will be detailed in the following sections.

9.2.1 Gyrator model[8]

9.2.1.1 Duality principle

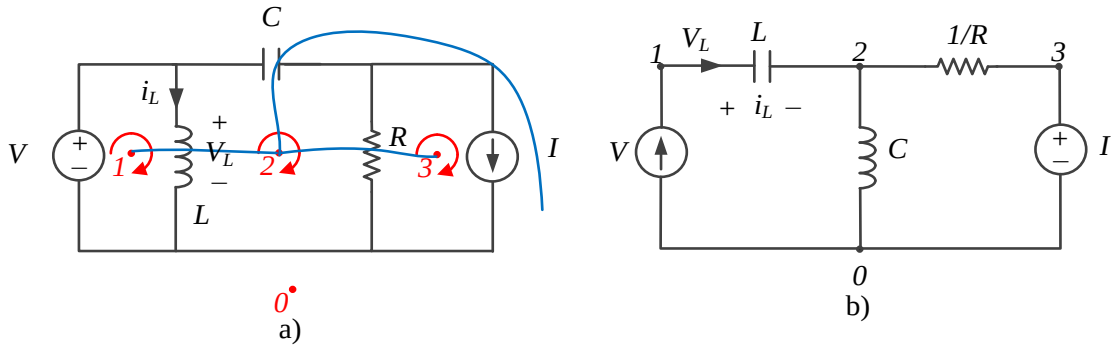
The duality principle states that a dual circuit can be constructed from the dual pairs of one circuit. Among the dual pairs for electrical circuits, one can cite resistance ↔ conductance, capacitance ↔ inductance, voltage ↔ current, node ↔ mesh/loop, series path ↔ parallel path, KVL ↔ KCL, etc. The important factor is that the characterization equations of both circuits shall be the same with interchanged variables and quantities. However, to determine the dual of one circuit one does not need to write equations but use a graphical approach which consists of the following steps given in (CHARLES K. ALEXANDER, 2012):

1. Place a numbered node at the center of each mesh and a reference node (ground) outside of the circuit.
2. Draw lines between the nodes crossing the elements.
3. Replace each element by its dual pair.
4. Determine the polarity of the voltage source and direction of the current source. Define clock-wise current for each mesh.
    a. Voltage source: if the defined mesh current is in the same direction of the voltage increase, the dual current source flows its current to the node encircled by the mesh current and vice versa.
    b. Current source: if the defined mesh current and the current source have the same direction, the dual voltage source has its positive pole connected to the node encircled by the mesh current and vice versa.
5. Draw the dual using the numbered mesh nodes as nodes and place the dual elements.

A simple example is of the application of the procedure is presented in Figure 87. Notice that the dual circuit shows the quantities of the original circuit.

[8] Based on Chapter 5 of (ZACHARIAS, 2020)

Figure 87 – Example on how to determine the dual of a circuit. b) is the dual of circuit a).



Source: Author.

9.2.1.2 Conversion between magnetic and electric circuits

Figure 88a presents a winding and the electric and magnetic variables associated with it, i.e. mmf (F) and flux (Φ). The winding can be characterized as a quadripole (Figure 88b) in which the electrical variables are in one side (v and i) and magnetic variables (F and Φ) are in the other side.

The quadripole equations are derived from the voltage drop and flux linkage as follows:

$$F = N \cdot i \tag{62}$$

$$\int v \cdot dt = \Psi = N \cdot \Phi \tag{63}$$

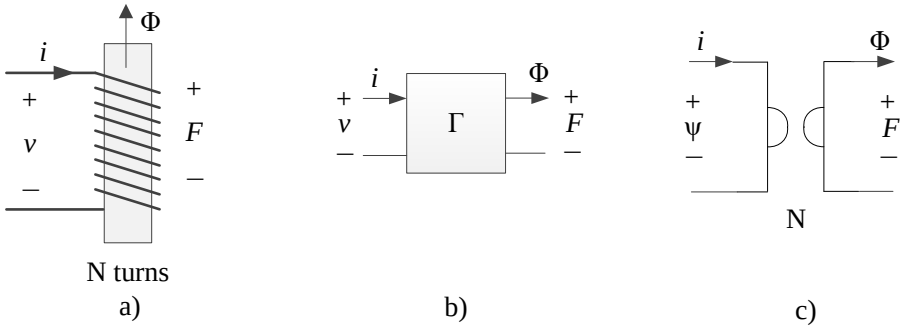
One can arrange (62) and (63) as a matrix (Γ – quadripole impedance matrix) form, (64) with its inverse (65):

$$\begin{bmatrix} \int v \cdot dt \\ F \end{bmatrix} = \begin{bmatrix} \Psi \\ F \end{bmatrix} = \begin{bmatrix} 0 & N \\ N & 0 \end{bmatrix} \cdot \begin{bmatrix} i \\ \Phi \end{bmatrix} \tag{64}$$

$$\begin{bmatrix} i \\ \Phi \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{N} \\ \frac{1}{N} & 0 \end{bmatrix} \cdot \begin{bmatrix} \int v \cdot dt \\ F \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{N} \\ \frac{1}{N} & 0 \end{bmatrix} \cdot \begin{bmatrix} \Psi \\ F \end{bmatrix} \tag{65}$$

The structure of (64) is similar to the transmission equations of a gyrator (TELLEGEN, 1948) (Figure 88c), a basic element for the representation and analysis of electrical circuits. A gyrator converts the terminal behavior of a network, which is connected on one side of this quadripole into the dual terminal behavior on the other side. The gyrator mediates the connection between electric and magnetic quantities, working as a “dualizer”

Figure 88 – Representation of a winding as a quadripole: a) winding with its related magnetic and electric variables; b) winding representation as a quadripole; c) gyrator connecting electric and magnetic quantities.



Source: (ZACHARIAS, 2020).

(HAMILL, 1993). An inversion of the impedance matrix Γ leads – as (65) shows – again on a gyrator, however with the reverse direction of action for mapping the dual pairs to each other.

If two such gyrators are connected as Figure 89a, an ideal transformer (Figure 89b – notice that the symbol for the ideal transformer is slightly different) is obtained.

The ideal transformer maps the input voltage v_1 or flux linkage Ψ_1 to the output voltage v_2 or flux linkage Ψ_2 and the input current i_1 to the output current i_2 in a bidirectional manner without loss.

For the connection between the four poles, it is advisable to choose a different representation of the transmission equations.

$$\begin{bmatrix} \Psi \\ i \end{bmatrix} = \begin{bmatrix} 0 & N \\ \frac{1}{N} & 0 \end{bmatrix} \cdot \begin{bmatrix} F \\ \Phi \end{bmatrix} \tag{66}$$

And its inverse

$$\begin{bmatrix} F \\ \Phi \end{bmatrix} = \begin{bmatrix} 0 & N \\ \frac{1}{N} & 0 \end{bmatrix} \cdot \begin{bmatrix} \Psi \\ i \end{bmatrix} \tag{67}$$

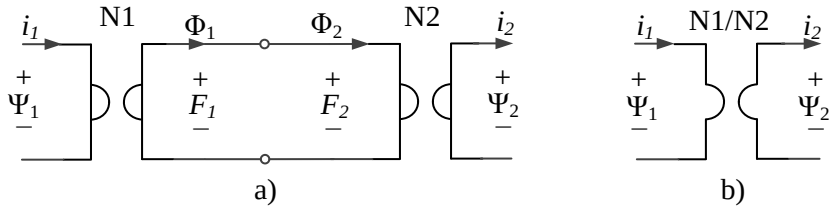
For the description of the arrangement of Figure 89a, one can then write:

$$\begin{bmatrix} \Psi_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} 0 & N1 \\ \frac{1}{N1} & 0 \end{bmatrix} \cdot \begin{bmatrix} F_1 \\ \Phi_1 \end{bmatrix} \quad and \quad \begin{bmatrix} \Psi_2 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 & N2 \\ \frac{1}{N2} & 0 \end{bmatrix} \cdot \begin{bmatrix} F_2 \\ \Phi_2 \end{bmatrix} \tag{68}$$

As $\Phi_1 = \Phi_2$ and $F_1 = F_2$, one obtains:

$$\begin{bmatrix} \Psi_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} 0 & N1 \\ \frac{1}{N1} & 0 \end{bmatrix} \cdot \begin{bmatrix} 0 & N2 \\ \frac{1}{N2} & 0 \end{bmatrix} \cdot \begin{bmatrix} \Psi_2 \\ i_2 \end{bmatrix} \rightarrow \begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} \frac{N1}{N2} & 0 \\ 0 & \frac{N2}{N1} \end{bmatrix} \cdot \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{69}$$

Figure 89 – Ideal transformer construction: a) the connection of two inverse gyrators; b) transformer.



Source: (ZACHARIAS, 2020).

To distinguish an ideal transformer from symbols commonly used in circuit diagrams, the circuit diagram of Figure 89b is derived from the gyrator symbol previously described.

The following characteristics of the transformer can also be found in the symbol of Figure 89b:

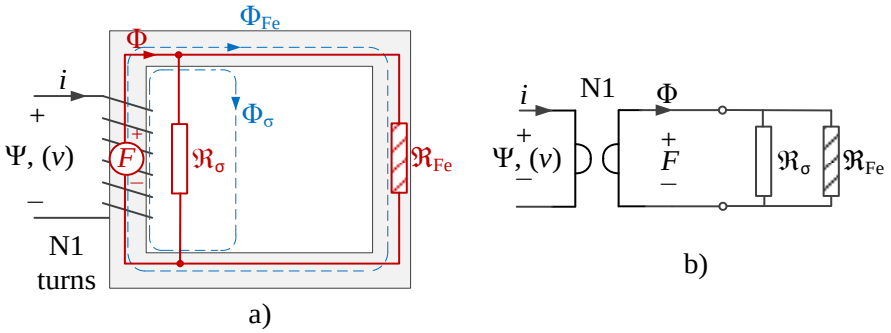
- The transformer insulates electrically.
- Although the ideal transformer transmits energy without loss bi-directionally, it has a direction of action for the voltage (and respectively current). This is illustrated by the arrows' direction in the symbol.
- The input impedance of the transformer with no-load at the output is infinitely high, while the input impedance with the secondary shorted is zero.

9.2.1.3 Modeling of a magnetic element and the connection with electrical variables

Figure 90a presents an ordinary inductor with N1 turns winding and the fluxes Φ_{Fe} (flux inside the core) and Φ_σ (leakage flux) and resultant flux Φ. The equivalent reluctance circuit is also drawn with the generated mmf (F) and the reluctance of the leakage flux ($\Re_\sigma$) and the core ($\Re_{Fe}$) flux paths.

In Figure 90b one can observe the reluctance model attached to the gyrator which acts as a mediator between magnetic and electric quantities. Notice that the reluctance of the air flux path is represented by a white rectangle and the reluctance of the core is represented by a hatched rectangle.

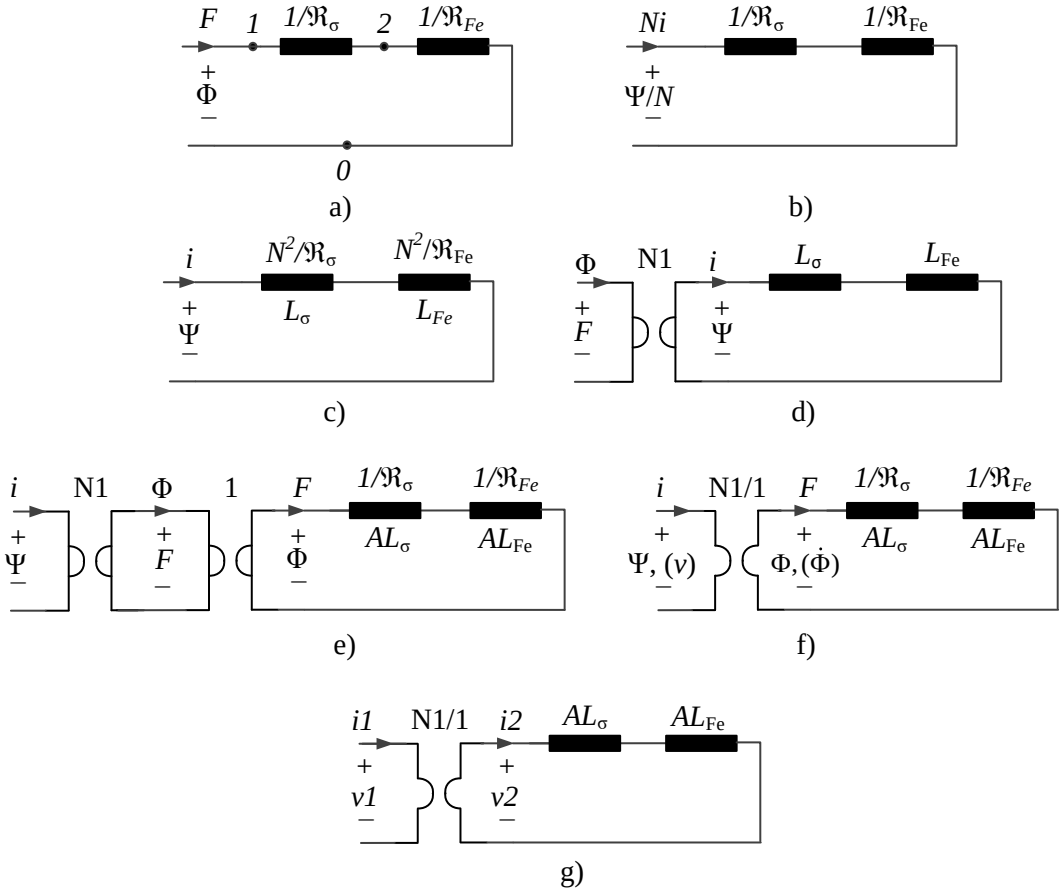
Figure 90 – Structure of an inductor: a) representation of the reluctance model equivalent circuit diagram; b) representation with the gyrator as mediator between magnetic and electrical quantities.



Source: Based on (ZACHARIAS, 2020) and modified.

One proceeds then to determine the inductance model through the application of the duality principle to the reluctance association of Figure 90b. Applying the rules of section 9.2.1.1 one obtains the circuit of Figure 91a. In this circuit, the quantities were interchanged and reluctance gives place to its dual, the permeance. As the unit of permeance is Henry, one represents it with an inductor. Making use of (62) and (63), the circuit of Figure 91b is obtained. The inductor model is then derived in Figure 91c using the definition of inductance and its relation with the permeance. The inductor model can then be used to connect the magnetic modeled device to the electrical circuit. However, this transformation doesn't work for every configuration (CHERRY, 1949). For this reason, both magnetic and electric quantities must be isolated from each other. One can then, combine two gyrators to generate a transformer, as presented before. From the inductor model presented in Figure 91c, one can combine the gyrator as specified in (67) resulting in the circuit depicted in Figure 91d. Figure 91e is obtained after combining the inverse gyrator, which results in an ideal transformer. Notice that, as the ideal transformer represents the winding with N1 turns, one gyrator has coefficient N1 and the other has unitary coefficient. In this case, the equivalent circuit is similar to the presented in Figure 91a with permeances instead of inductances. The permeances are usually treated in magnetic cores datasheets as inductance factor (AL) which is the term used from now on. The result is presented in Figure 91f. One can see that in the equivalent model, currents represent m.m.f. and voltages represent the flux. This happens when the input of the ideal transformer is linkage flux and current. When the voltage is set as the input of the ideal transformer, instead of the linkage flux, according to (63) one has flux rate in the output of the ideal transformer. This representation is aligned with other physical representation since the product of the effort variable $\dot{\Phi}$ (in Volts) and the flow variable F (in Ampère) result in power (HAMILL, 1993).

Figure 91 – Determining the dual of the circuit of Figure 90b: a) dual of the reluctance association; b) intermediate circuit; c) inductor model; d) inductor model associated to a gyrator.



Source: Based on (ZACHARIAS, 2020) and modified.

The physical meaning of the model has already been explained. Now one needs to proceed to the practical aspects of its use. It is not easy to apply circuit laws in terms of flux rate and m.m.f.. One can simply considerer voltages and currents instead of flux rate and m.m.f., respectively, as depicted in Figure 91g. The following relations hold:

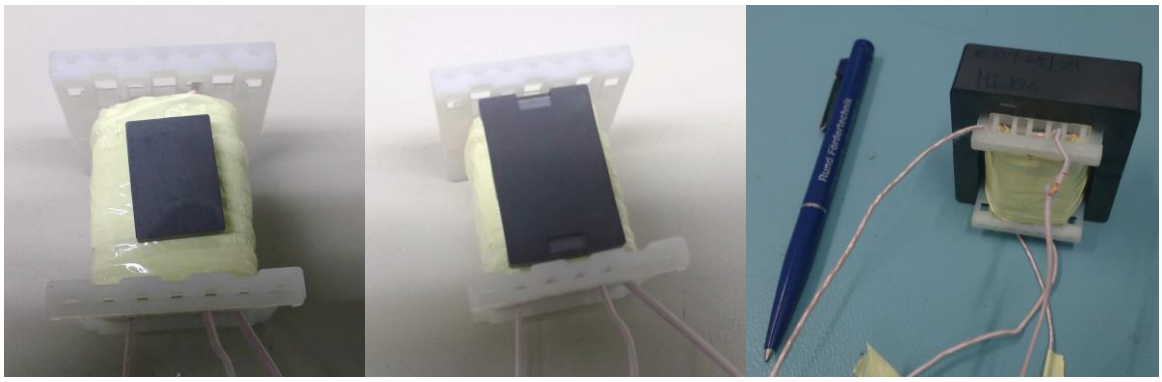
$$v1 = N1 \cdot v2$$
$$i2 = N1 \cdot i1$$
$$Z = \frac{\vec{v1}}{\vec{i1}} = \frac{N1^2 \cdot \vec{v2}}{\vec{i2}} = N1^2 \cdot \left(X_\sigma + X_{Fe}\right) = N1^2 \cdot j\omega \cdot \left(AL_\sigma + AL_{Fe}\right) \quad (70)$$

9.3 Integrated magnetic design – transformer with high leakage inductance

According to the design defined in Section 3.5.3, the leakage inductance of the transformer should be 108μH to achieve nominal power with phase-shift of 15°. The procedure

to achieve this value was try and error. One good approach to reduce the number of interactions is to determine the upper bound of the leakage inductance that can be achieved with the selected core and the designed parameters. Then, the first attempt used the top-bottom winding arrangement (Figure 85a), which resulted in a leakage inductance value of 208µH. The second try used the side-side arrangement since the expected achievable inductance value is smaller according to Figure 85. In fact, the inductance value achieved was 47µH with a small ferromagnetic segment (20.16mm x 14.02mm x 2.26mm) inserted between the windings as presented in Figure 92a. The third try used the same configuration but with a bigger ferromagnetic segment (31.95mm x 20.50mm x 2.99mm) which achieved a suitable leakage inductance of 103µH (Figure 92b).

Figure 92 – Setting the leakage inductance of the transformer with ferromagnetic segments between the windings in a side-side arrangement. The pictures *a* and *b* show one winding and the ferromagnetic segment in place: a) 47µH achieved with a 20.16mm x 14.02mm x 2.26mm segment; b) 103µH achieved with 31.95mm x 20.50mm x 2.99mm segment; c) completed transformer.



a) b) c)

Source: Author.

The constructed transformer can be observed in Figure 92c and its parameters are detailed in Table 34. To avoid saturation one small air gap of 0.1 mm was introduced.

Table 34 – Isolation transformer with high leakage inductance.

Parameter	**Description**
Core type	E 55/28/21
Material	Mf 102 – Tridelta
Number of turns	45/45
Leakage inductance	103 µH
Magnetizing inductance	11.8 mH
B_{max}	0.19 T
Frequency	30 kHz
Winding	Litz wire: 120 x 0.1 mm / 25 x 0.2 mm

Air gap	0.1 mm

Source: Author.

9.4 Integrated magnetic design – integrated interleaved transformer

The goal of this section is to present the procedure to integrate the elements *L* and CI-ab shown in Figure 26 into a single core. Usually coupled inductors like CI-ab are constructed using toroidal cores to ensure high coupling between the windings (as presented in Section 3.5.2). However, one needs to reduce the coupling factor to increase longitudinal inductance. Although toroidal cores can also be used (KLEEB, 2016), an E core was chosen.

9.4.1 Simplified model

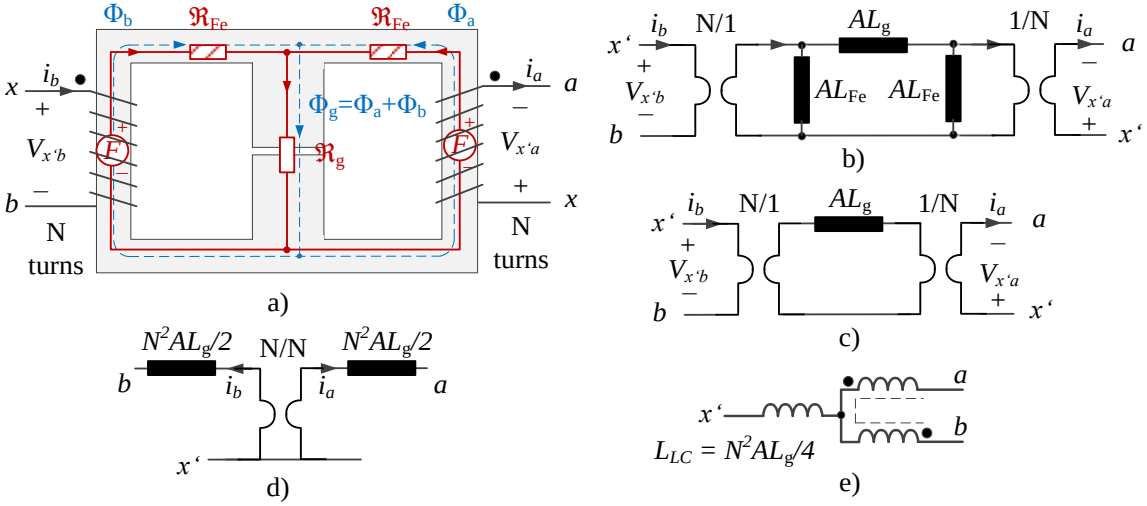
The proposed magnetic element is presented in Figure 93a. The fluxes are shown and a simplified reluctance circuit is presented superposed (in red) with the reluctance of the air gap $\Re_g$ and the reluctance of the core $\Re_{Fe}$. Applying the knowledge of Section 9.2, one obtains the equivalent circuit depicted in Figure 93b. One can further simplify this circuit considering that the core inductance factors AL_{Fe} (permeances) are much higher than the permeance of the air gap so that no current goes through these elements. The simplified circuit is presented in Figure 93c. One can then split the inductance equally generating the circuit of Figure 93d. Rearranging the circuit and using the traditional symbol of an ideal transformer, one obtains Figure 93e, where the value of the longitudinal inductance is:

$$L_{LC} = \frac{N^2 \cdot AL_g}{4} \tag{71}$$

9.4.2 Detailed model

In order to calculate the inductance accurately, one needs to consider the leakage reluctances of the E core. The most important reluctances to take into account are the reluctance of the window ($\Re_w$), the reluctance between the top and bottom surfaces of the core ($\Re_{tp}$), the reluctance of the side legs ($\Re_\sigma$) and the fringing effect created by the gap that can be modeled as reluctance ($\Re_f$). The calculations of all reluctances can be found in (KLEEB, 2016). From

Figure 93 – Proposed integrated magnetic and its simplified model: a) proposed magnetic element and its simplified reluctance circuit; b) equivalent inductor-gyrator model; c) simplified model considering $AL_{Fe} \sim \infty$; d) rearranged elements; e) longitudinal inductance.



Source: Author.

Figure 94a can be observed that all leakage reluctances are in parallel with the central leg. The leakage permeance of the parallel paths is determined as follows:

$$A_{leak} = \frac{1}{\Re_{tp1}} + \frac{1}{\Re_{tp2}} + \frac{1}{\Re_{w1}} + \frac{1}{\Re_{w2}} \tag{72}$$

The permeance of the central leg is given by:

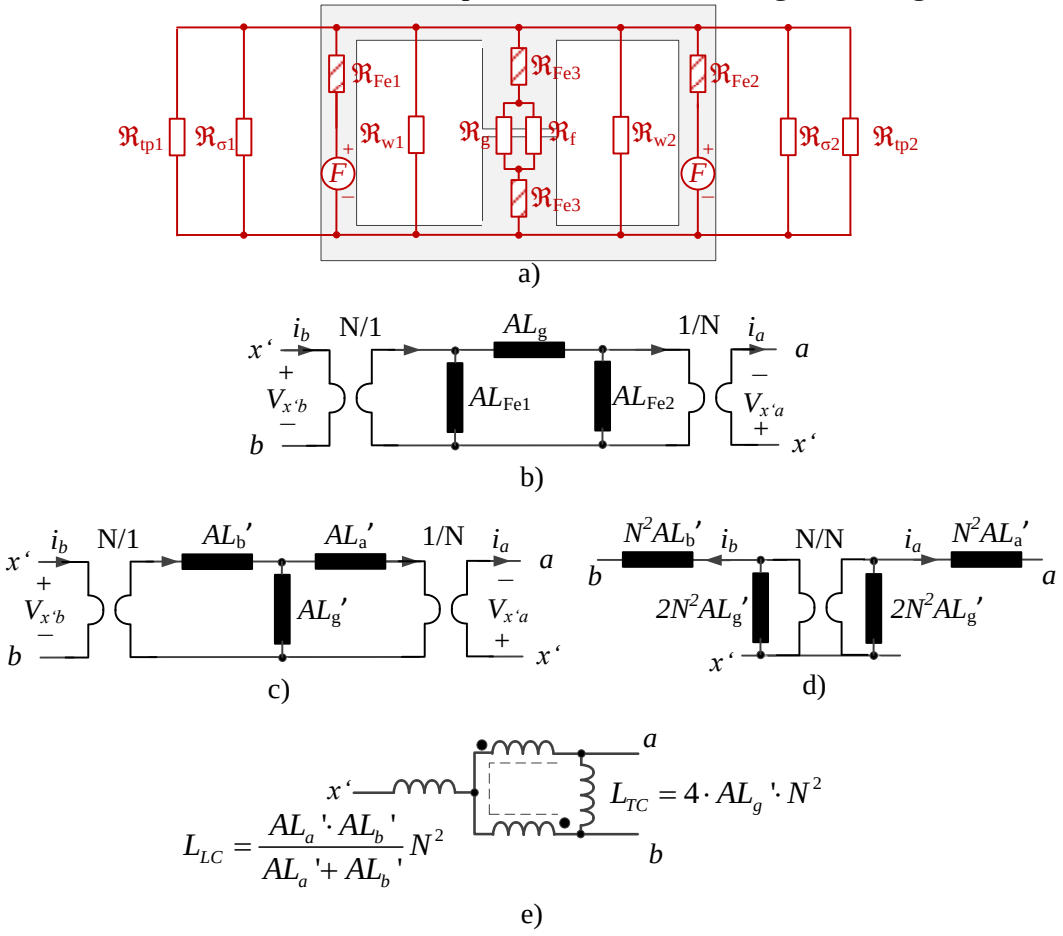
$$AL_{g1} = \frac{1}{\frac{1}{2 \cdot \Re_{Fe3}} + \frac{1}{\frac{\Re_g \cdot \Re_f}{\Re_g + \Re_f}}} \tag{73}$$

The equivalent circuit is presented in Figure 94b, where the resultant permeance $AL_g = AL_{g1} + AL_{leak}$. Making use of the Y-Δ transformation, one obtains the circuit of Figure 94c, where ($AL_{Fe} = AL_{Fe1} = AL_{Fe2}$):

$$AL_a' = AL_b' = \frac{AL_{Fe} \cdot AL_g}{2 \cdot AL_{Fe} + AL_g}$$
$$AL_g' = \frac{AL_{Fe}^{\,2}}{2 \cdot AL_{Fe} + AL_g} \tag{74}$$

Applying similar steps as used in the previous section, one reaches Figure 94d. Rearranging the circuit and following the procedures found in (BOILLAT; KOLAR, 2012), one determines the longitudinal and transverse inductance (Figure 94e) as:

Figure 94 – Reluctance model of the coupled inductor considering the leakage reluctances.



Source: Author.

$$L_{LC} = \frac{AL_a' \cdot AL_b'}{AL_a' + AL_b'} N^2 \tag{75}$$

The self-inductance of the windings can be obtained from Figure 94b (AL_{Fe} = AL_{Fe1}= AL_{Fe2}):

$$L = L_a = L_b = \frac{N^2 \cdot \left(AL_g + AL_{Fe}\right) \cdot AL_{Fe}}{2 \cdot AL_{Fe} + AL_g} \tag{76}$$

The coupling factor can also be determined from Figure 94b with the knowledge that the voltages over the inductance factor elements represent the fluxes (as represented in Figure 91f). The part of the flux linking both windings caused by a current in ‘a’ is given by:

$$k_{ba} = \frac{\Phi_b}{\Phi_a} = \frac{v_b}{v_a} = \frac{AL_{Fe2}}{AL_{Fe2} + AL_g} \tag{77}$$

Similarly:

$$k_{ab} = \frac{\Phi_a}{\Phi_b} = \frac{v_a}{v_b} = \frac{AL_{Fe1}}{AL_{Fe1} + AL_g} \tag{78}$$

As it is considered that $AL_{Fe} = AL_{Fe1} = AL_{Fe2}$, then $k_{ab} = k_{ba}$.

9.4.2.1 Determining the current ripple

Based on Figure 93, and in order to determine the current ripple one takes the winding voltages:

$$\begin{aligned} v_{x'a} &= L_a \frac{di_a}{dt} - M \frac{di_b}{dt} \\ v_{x'b} &= L_b \frac{di_b}{dt} - M \frac{di_a}{dt} \end{aligned} \tag{79}$$

Where L_a and L_b are the windings self-inductances. If we consider $L_a = L_b = L$, $M = k \cdot L$, $k = \sqrt{k_{ab} \cdot k_{ba}}$ and from (79), the current ripple for both windings is determined as:

$$\begin{aligned} \frac{di_a}{dt} &= \frac{v_{x'a} + k \cdot v_{x'b}}{L \cdot \left(1 - k^2\right)} \\ \frac{di_b}{dt} &= \frac{k \cdot v_{x'a} + v_{x'b}}{L \cdot \left(1 - k^2\right)} \end{aligned} \tag{80}$$

Considering constant the DC bus, the voltages $v_{x'a}$ and $v_{x'b}$ are determined using the state of the switches, S_a, S_b, and S_n. They are defined as:

$$\begin{aligned} v_{x'a} &= v_g - \left(v_{ap} - v_{np}\right) = v_g - \left[\left(1 - 2 \cdot S_a\right) \cdot \frac{V_{dc}}{2} - \left(1 - 2 \cdot S_n\right) \cdot \frac{V_{dc}}{2}\right] \\ v_{x'b} &= v_g - \left(v_{bp} - v_{np}\right) = v_g - \left[\left(1 - 2 \cdot S_b\right) \cdot \frac{V_{dc}}{2} - \left(1 - 2 \cdot S_n\right) \cdot \frac{V_{dc}}{2}\right] \end{aligned} \tag{81}$$

The current ripple varies throughout the grid voltage period. Considering $v_g = V_g \cdot \sin(\omega_g \cdot t)$, (28), unitary power factor and $S_n = 1$, one obtains the equations for the current ripple for the winding currents i_a and i_b (Table 35) from (80) and (81).

Table 35 – Current ripple of the windings of the integrated inductor for $S_n = 1$.

Duty cycle	Current	Interval	Equation
$0 < D \leq 0.5$	Δi_a	Δt_1	$\frac{\left(S_n - M_f \cdot \sin\left(\omega_g \cdot t\right)\right) \cdot \left[\left(V_{dc} \cdot M_f \cdot \sin\left(\omega_g \cdot t\right)\right) \cdot \left(1 + k\right) - V_{dc} \cdot k\right]}{L \cdot fs \cdot \left(1 - k^2\right)}$
	Δi_b	Δt_3	

	Δi_a	Δt_3	$\frac{\left(S_n - M_f \cdot \sin\left(\omega_g \cdot t\right)\right) \cdot \left[\left(V_{dc} \cdot M_f \cdot \sin\left(\omega_g \cdot t\right)\right) \cdot (1+k) - V_{dc}\right]}{L \cdot fs \cdot \left(1-k^2\right)}$
	Δi_b	Δt_1	
	Δi_a, Δi_b	Δt_2, Δt_4	$\frac{V_{dc} \cdot \left(2 \cdot M_f \cdot \sin(\omega_g \cdot t) - 2 \cdot S_n + 1\right) \cdot (1+k) \cdot \left(M_f \cdot \sin(\omega_g \cdot t) - 1\right)}{2 \cdot L \cdot fs \cdot \left(1-k^2\right)}$
$0.5 < D \leq 1$	Δi_a	Δt_2	$\frac{V_{dc} \cdot \left[M_f \cdot \sin\left(\omega_g \cdot t\right) \cdot (1+k) - k\right] \cdot \left(M_f \cdot \sin\left(\omega_g \cdot t\right) - S_n + 1\right)}{L \cdot fs \cdot \left(1-k^2\right)}$
	Δi_b	Δt_4	
	Δi_a	Δt_4	$\frac{V_{dc} \cdot \left[M_f \cdot \sin\left(\omega_g \cdot t\right) \cdot (1+k) - 1\right] \cdot \left(M_f \cdot \sin\left(\omega_g \cdot t\right) - S_n + 1\right)}{L \cdot fs \cdot \left(1-k^2\right)}$
	Δi_b	Δt_2	
	Δi_a, Δi_b	Δt_1, Δt_3	$\frac{\left(V_{dc} \cdot M_f \cdot \sin\left(\omega_g \cdot t\right)\right) \cdot (1+k) \cdot \left(2 \cdot M_f \cdot \sin\left(\omega_g \cdot t\right) + 1 - 2 \cdot S_n\right)}{2 \cdot L \cdot fs \cdot \left(1-k^2\right)}$

Source: Author.

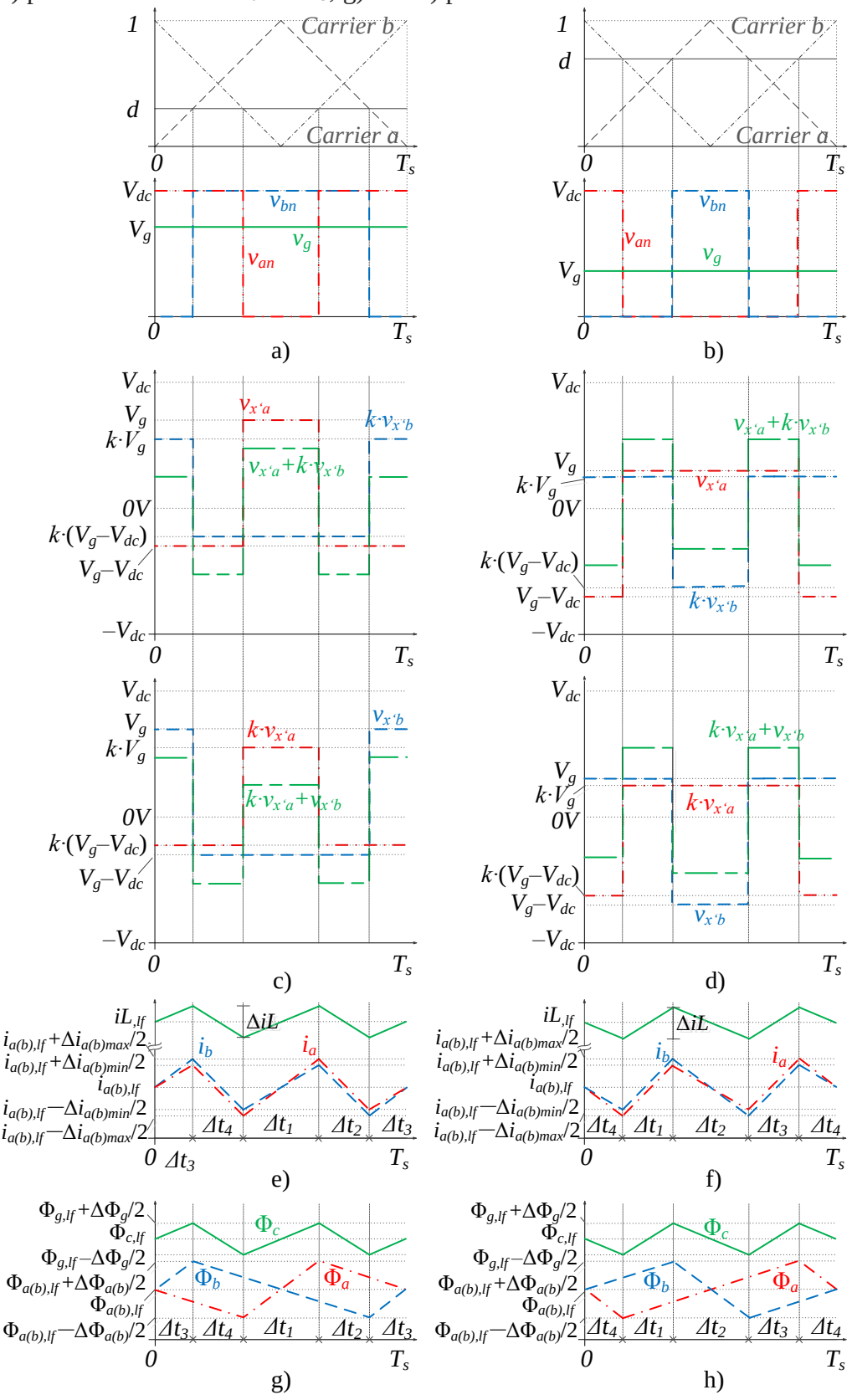
The time intervals specified in Table 35 are found in Figure 95, which details the time intervals of the voltages applied to the windings and the resulting currents. The left side of Figure 95 presents variables for $0 < d \leq 0.5$ while the right side for $0.5 < d \leq 1$. Figure 95a presents the voltages v_{an} and v_{bn}. Figure 95c presents voltage applied to each winding according to (81) and the voltage that determines the current ripple as presented in (80). Notice that each time interval present a different voltage due to the combination of the coupling factor k and the voltages waveforms. The result is a different current ripple (Figure 95e) for each time interval.

Based in Table 35 and in Figure 94, one can specify the maximum and minimum current ripple for winding currents as:

$$\begin{aligned}
\Delta i_{a,\max} &= \begin{cases} \Delta i_{a,t1} & if \quad 0 < d \leq 0.5 \\ \Delta i_{a,t4} & if \quad 0.5 < d \leq 1 \end{cases} \\
\Delta i_{b,\max} &= \begin{cases} \Delta i_{b,t3} & if \quad 0 < d \leq 0.5 \\ \Delta i_{b,t2} & if \quad 0.5 < d \leq 1 \end{cases} \\
\Delta i_{a,\min} &= \begin{cases} \Delta i_{a,t3} & if \quad 0 < d \leq 0.5 \\ \Delta i_{a,t2} & if \quad 0.5 < d \leq 1 \end{cases} \\
\Delta i_{b,\min} &= \begin{cases} \Delta i_{b,t1} & if \quad 0 < d \leq 0.5 \\ \Delta i_{b,t4} & if \quad 0.5 < d \leq 1 \end{cases}
\end{aligned} \tag{82}$$

Based on (82), the windings current ripple variation according to the voltage phase angle ($\omega_g \cdot t$) are presented in Figure 96a.

Figure 95 –.Voltages applied to the integrated inductor windings, currents and fluxes: a) and b) show voltages v_{an} and v_{bn}; the voltages applied to the windings are presented in c) and d); e) and f) present the currents i_a and i_b; g) and h) present the fluxes.



Source: Author.

The current ripple of the converter input current is easily determined adding the current rate of both windings i_a and i_b. in any time interval presented in Figure 95e. The same is valid for Figure 95f. Making use of the time interval Δt_4, the input current ripple is:

$$\Delta iL = \begin{cases} \dfrac{V_{dc}\cdot\left(2\cdot M_f\cdot\sin(\omega_g\cdot t)-2\cdot S_n+1\right)\cdot(1+k)\cdot\left(M_f\cdot\sin(\omega_g\cdot t)-1\right)}{L\cdot fs\cdot\left(1-k^2\right)} & if \quad 0\le d\le 0.5 \\ \dfrac{\left(V_{dc}\cdot M_f\cdot\sin\left(\omega_g\cdot t\right)\right)\cdot(1+k)\cdot\left(2\cdot M_f\cdot\sin\left(\omega_g\cdot t\right)+1-2\cdot S_n\right)}{L\cdot fs\cdot\left(1-k^2\right)} & if \quad 0.5< d\le 1 \end{cases} \tag{83}$$

The maximum current ripple is given by:

$$\Delta iL \le \frac{V_{dc}}{8\cdot L\cdot fs\cdot(1-k)} \tag{84}$$

9.4.2.2 Determining the flux swing and peak flux

The flux swing presented in Figure 93a can be calculated from (81) and the Faraday's law:

$$\begin{aligned} v_{x'a} &= N\frac{d\Phi_a}{dt} \\ v_{x'b} &= N\frac{d\Phi_b}{dt} \\ v_{x'a}+v_{x'b} &= N\frac{d\Phi_g}{dt} \end{aligned} \tag{85}$$

Notice in Figure 94g that the flux swing Φ_a and Φ_b have half of the frequency of Φ_g. The flux swing of Φ_a can be calculated for $\Delta t1$ and it is given by:

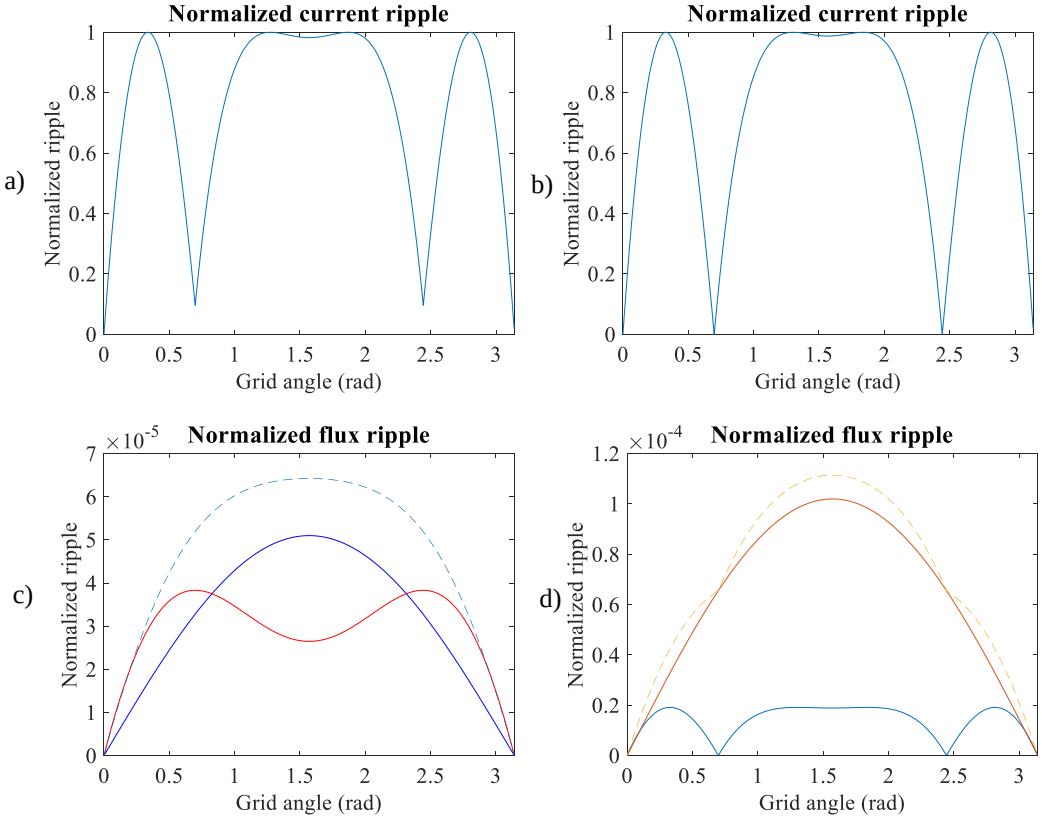
$$\Delta\Phi_{a(b)} = \frac{V_{dc}\cdot M_f\cdot\sin\left(\omega_g\cdot t\right)\cdot\left(S_n-M_f\cdot\sin\left(\omega_g\cdot t\right)\right)}{N\cdot fs} \tag{86}$$

Similar result is found for Φ_b. Both results are valid for $0 \le d \le 1$. The same is not valid for the flux Φ_g, which has different equations according to:

$$\Delta\Phi_g = \begin{cases} \dfrac{V_{dc}\cdot\left(1-2\cdot M_f\cdot\sin(\omega_g\cdot t)\right)\cdot\left(S_n-M_f\cdot\sin(\omega_g\cdot t)\right)}{N\cdot fs} & if \quad 0\le d\le 0.5 \\ \dfrac{2\cdot V_{dc}\cdot M_f\cdot\sin(\omega_g\cdot t)\cdot\left(M_f\cdot\sin(\omega_g\cdot t)-S_n+0.5\right)}{N\cdot fs} & if \quad 0.5< d\le 1 \end{cases} \tag{87}$$

In order to determine the low-frequency flux, one can use the currents and the windings' inductances. The flux Φ_a can be calculated observing Figure 93a as:

Figure 96 –.Currents and fluxes variating according the voltage phase angle: a) and b) current ripple variation of currents i_a and iL; c) flux ripple, low frequency component and their summation (valid for legs ‘a’ and ‘b’); d) flux ripple, low frequency component and their summation (valid for leg ‘g’).



Source: Author.

$$\Phi_{a(b),lf} = \frac{L \cdot i_a - M \cdot i_b}{N} \tag{88}$$

As the windings have the same number of turns, it is considered that $i_{a,lf} = i_{b,lf}$. Based on this, the low-frequency flux components become:

$$\begin{aligned} \Phi_{a(b),lf} &= \frac{L \cdot (1-k) \cdot i_{a(b),lf}}{N} \\ \Phi_{g,lf} &= 2 \cdot \Phi_{a(b),lf} \end{aligned} \tag{89}$$

To avoid core saturation, the maximal flux density admitted by the core material cannot be exceeded. The maximal peak flux needs to be determined.

The resultant flux is composed by the low frequency and high-frequency components. Figure 96c, and Figure 96d show the flux variating according to the voltage phase angle. In both cases, the maximum flux is achieved when the voltage phase angle is π/2. The maximum flux is then:

$$\Phi_{a(b),\max} \underset{\omega_g \cdot t=\pi/2}{=} \Phi_{a(b),lf} + \frac{\Delta\Phi_{a(b)}}{2}$$
$$\Phi_{a(b),\max} \underset{\omega_g \cdot t=\pi/2}{=} \frac{L\cdot(1-k)\cdot I_{a(b)pk}}{N} + \frac{(1-M_f)\cdot M_f \cdot V_{dc}}{2\cdot fs\cdot N} \quad (90)$$

Similarly the maximum flux $\Phi_{g,max}$ is given by:

$$\Phi_{g,\max} \underset{\omega_g \cdot t=\pi/2}{=} \Phi_{g,lf} + \frac{\Delta\Phi_{g}}{2}$$
$$\Phi_{g,\max} \underset{\omega_g \cdot t=\pi/2}{=} 2\frac{L\cdot(1-k)\cdot I_{a(b)pk}}{N} + \frac{(M_f-1)\cdot(1-2\cdot M_f)\cdot V_{dc}}{fs\cdot N} \quad (91)$$

9.4.3 Design

In order to design this integrated inductor one needs to determine the required longitudinal inductance. Based on (34) and for a 20% ripple, the required value is 683 µH.

An E 55/28/21 core with an air gap of 2 mm in the central leg was already available. From (75), one determines the number of turns needed to achieve the desired longitudinal inductance. Then, one needs to verify with (90) and (91) that the fluxes densities are within the limits imposed by the material.

The winding conductors are determined using a current density of 4 A/mm^2. The design results are summarized in Table 36.

Table 36 – Integrated interleaved transformer.

Parameter	**Description**
ΔiL (20%)	1.22A
Required Longitudinal inductance (L_{LC})	683 µH
Core	E 55/28/21
Cross section area	354 mm^2
Air gap (central leg)	2.0 mm
Inductance factor core (AL_{Fe})	6.4 µH
Inductance factor air gap (AL_g)	0.374 µH
Material	Mf 102 – Tridelta
Saturation flux density (B_{sat})	0.5 T
Low frequency density peak flux for legs ‘a’, ‘b’ and ‘g’	0.29 T
Peak flux density for legs ‘a’ and ‘b’ ($B_{a(b)max}$)	0.36 T
Peak flux density for leg ‘g’ (B_{gmax})	0.34 T
Coupling factor (k)	0.95071
Self-inductance (L_a and L_b)	28 mH

Current ripple frequency	60 kHz
Current density	4 A/mm^2
Winding	Magnetic wire with diameter 0.85 mm

Source: Author.

9.4.4 Experimental Results

Simulations of the designed integrated magnetics were performed with the software PLECS®. The circuit simulated presented in Figure 97 is placed in the secondary and it is the same depicted in Figure 94b.

The simulation results of the model show that the analytical expressions presented in Table 35 and in equations (86) to (91) are correct.

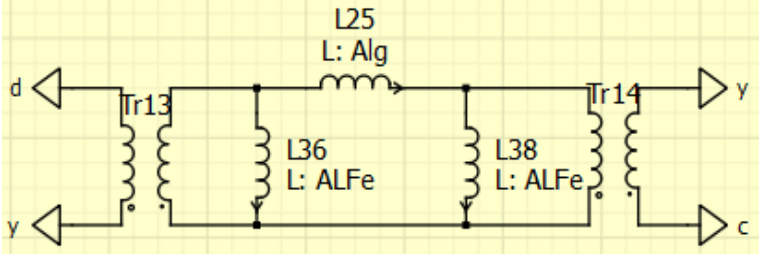
The manufactured integrated magnetic is presented in Figure 98a. The measured self-inductance was 11.5 mH while the measured longitudinal inductance was 767.5 µH (both are small signal measurements performed with HAMEG – HM8118). Figure 98b shows the experimental currents in both windings (i_a and i_b) and their summation (iL). Notice that the windings currents have the same low-frequency level. One can also observe the different current ripple in each time interval as presented in Figure 95e and Figure 95f.

The measured current ripple was 1.15A and it gives the inductance of 724 µH.

9.5 Integrated magnetic design – integrated transformer

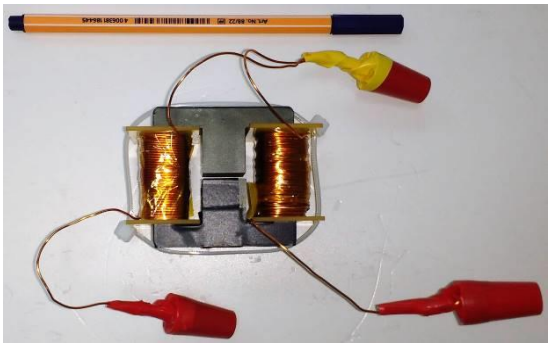
In the previous section, the filter inductor element was eliminated through its integration with the interleaved transformer. Now one needs to integrate this result with one transformer with high leakage inductance (Section 9.3). This is achieved by adding two new windings (secondary side of the transformer) connected in series. Each new winding is placed

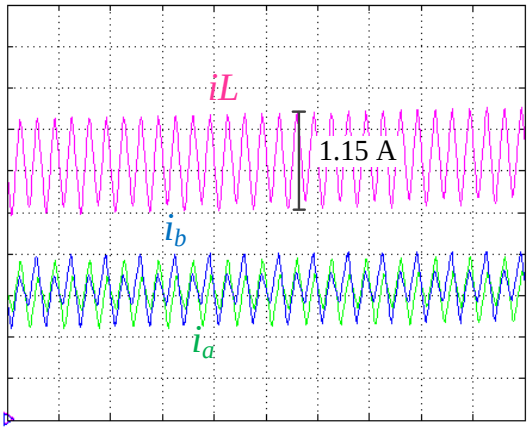
Figure 97 –.Simulated model.



Source: Author.

Figure 98 – Experimental results: a) integrated magnetic manufactured with double E 55/28/21; b) experimental results showing the windings currents and their summation.





a) b)

Source: Author.

over one winding of the integrated interleaved transformer so that one can obtain high coupling between primary and secondary. The leakage inductance is adjusted introducing a ferromagnetic segment between the primary and secondary windings.

9.5.1 Model

The proposed magnetic element is depicted in Figure 99a. One can see the four windings and their position within the core. The reluctance model of the element is also shown in the same picture. The meshes of the reluctance model are numbered. Based on this, one determines the dual circuit to obtain the equivalent gyrator model, which is shown in Figure 99b, where the meshes become nodes.

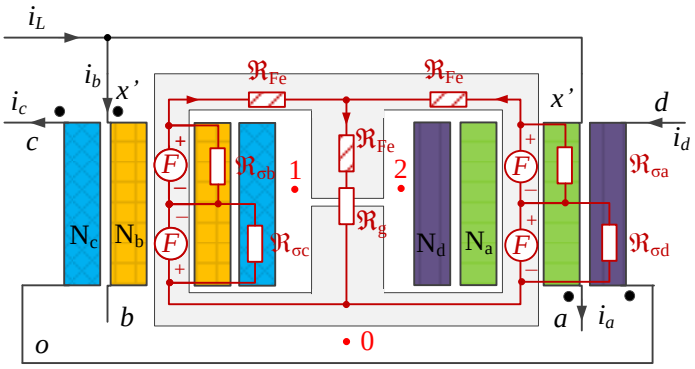
From Figure 99a, one obtains the inductance matrix given below:

$$\begin{pmatrix} v_{x'a} \\ v_{x'b} \\ v_{oc} \\ v_{do} \end{pmatrix} = \begin{bmatrix} L_a & -M_{ab} & M_{ac} & M_{ad} \\ -M_{ba} & L_b & -M_{bc} & -M_{bd} \\ M_{ca} & -M_{cb} & L_c & M_{cd} \\ M_{da} & -M_{db} & M_{dc} & L_d \end{bmatrix} \cdot \begin{pmatrix} di_a/dt \\ di_b/dt \\ di_c/dt \\ di_d/dt \end{pmatrix} \tag{92}$$

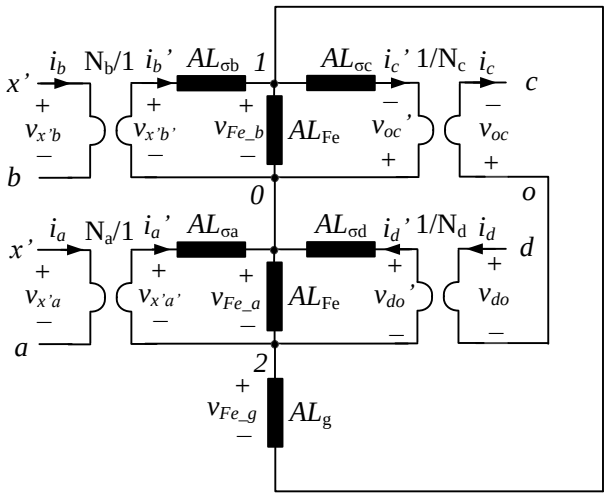
Where the point ‘o’ is the connection between the windings ‘c’, and ‘d’ to form the secondary side of the transformer. The permeance AL_g is formed by the series association of the $\Re_{Fe}$ and $\Re_g$. The self-inductance of the windings are given by:

$$
\begin{aligned}
L_a &= N_a^{\,2} \cdot \left[AL_{\sigma a} + \frac{AL_{Fe} \cdot \left(AL_{Fe} + AL_g \right)}{2 \cdot AL_{Fe} + AL_g} \right] \\
L_b &= N_b^{\,2} \cdot \left[AL_{\sigma b} + \frac{AL_{Fe} \cdot \left(AL_{Fe} + AL_g \right)}{2 \cdot AL_{Fe} + AL_g} \right] \\
L_c &= N_c^{\,2} \cdot \left[AL_{\sigma c} + \frac{AL_{Fe} \cdot \left(AL_{Fe} + AL_g \right)}{2 \cdot AL_{Fe} + AL_g} \right] \\
L_d &= N_d^{\,2} \cdot \left[AL_{\sigma d} + \frac{AL_{Fe} \cdot \left(AL_{Fe} + AL_g \right)}{2 \cdot AL_{Fe} + AL_g} \right]
\end{aligned}
\tag{93}
$$

Figure 99 –.Model of the integration of the transformer and the interleaved transformer: a) proposed magnetic element with four windings and its reluctance model: b) obtained equivalent gyrator model.



a)



b)

Source: Author.

As a simplification, all the windings are considered to have the same number of turns ($N_a = N_b = N_c = N_d = N$). In addition, the leakage permeances have the same values due to the symmetry, so that $AL_{\sigma a} = AL_{\sigma b} = AL_{\sigma c} = AL_{\sigma d} = AL_{\sigma}$. Given this, the coupling factor is:

$$\begin{aligned} k_{ab} = k_{ba} = k_{ac} = k_{ca} = k_{bd} = k_{db} &= \frac{AL_{Fe}{}^2}{\left(AL_{\sigma} + AL_{Fe}\right)\cdot\left(AL_{Fe} + AL_g\right)} \\ k_{bc} = k_{bc} = k_{ad} = k_{da} &= \frac{AL_{Fe}\cdot\left(AL_{Fe} + AL_g\right)}{AL_{Fe}{}^2 + AL_{Fe}\cdot AL_g + 2\cdot AL_{Fe}\cdot AL_{\sigma} + AL_g\cdot AL_{\sigma}} \end{aligned} \tag{94}$$

The mutual inductances are:

$$\begin{aligned} M_{ab} = M_{ba} = M_{ac} = M_{ca} = M_{bd} = M_{db} &= k_{ab}\cdot L \\ M_{bc} = M_{bc} = M_{ad} = M_{da} &= k_{bc}\cdot L \end{aligned} \tag{95}$$

Where $L = L_a = L_b = L_c = L_d$.

9.5.1.1 Determining the current ripple

From (92), one determines the current rate for all windings. The current rate of the input current iL is given by:

$$\frac{diL}{dt} = \frac{di_a}{dt} + \frac{di_b}{dt} = \frac{v_{x'a} + v_{x'b} - v_{oc} + v_{do}}{2\cdot L\cdot\left(1 - 2\cdot k_{ab} + k_{bc}\right)} + \frac{v_{x'a} + v_{x'b} + v_{oc} - v_{do}}{2\cdot L\cdot\left(1 - k_{bc}\right)} \tag{96}$$

The values of $v_{x'a}$ and $v_{x'b}$ are already available in (81). In contrast, no voltage source sets directly the voltages v_{oc} and v_{do}. Using circuit analysis and considering AL_{Fe} ~ inf, one determines such voltages from Figure 99b.

$$\begin{aligned} v_{oc} &= -\frac{\left(AL_g + 2\cdot AL_{\sigma}\right)\cdot v_{cd} + AL_g\cdot\left(v_{x'a} + v_{x'b}\right)}{2\cdot\left(AL_g + 2\cdot AL_{\sigma}\right)} \\ v_{do} &= -\frac{\left(AL_g + 2\cdot AL_{\sigma}\right)\cdot v_{cd} - AL_g\cdot\left(v_{x'a} + v_{x'b}\right)}{2\cdot\left(AL_g + 2\cdot AL_{\sigma}\right)} \end{aligned} \tag{97}$$

Applying (97) in (96) one obtains:

$$\frac{\Delta iL}{\Delta t} = \frac{\left(v_{x'a} + v_{x'b}\right)\cdot\left[AL_g\cdot\left(1 - k_{bc}\right) - 2\cdot AL_{\sigma}\cdot\left(1 + k_{ab}\right)\right]}{L\cdot\left(1 - k_{bc}\right)\cdot\left(AL_g + 2\cdot AL_{\sigma}\right)\cdot\left(k_{bc} - 2\cdot k_{ab} + 1\right)} \tag{98}$$

The result shows that the input current ripple depends only on the voltage applied to the primary side windings. The Figure 100e shows the current ripple ΔiL for d < 0.5 (left side) and d > 0.5 (right side).

As the current ripple varies throughout the grid voltage period and considering the same conditions given in Section 9.4.2.1, one obtains the current ripple variating with the grid phase:

$$\Delta iL = \begin{cases} \dfrac{\left(2\cdot M_f\cdot\sin(\omega_g\cdot t)-1\right)\cdot\left(S_n - M_f\cdot\sin(\omega_g\cdot t)\right)\cdot\left[AL_g\cdot\left(1-k_{bc}\right)-2\cdot AL_\sigma\cdot\left(1+k_{ab}\right)\right]}{L\cdot fs\cdot\left(1-k_{bc}\right)\cdot\left(AL_g+2\cdot AL_\sigma\right)\cdot\left(k_{bc}-2\cdot k_{ab}+1\right)} & if \quad 0\le d\le 0.5 \\ \dfrac{2\cdot M_f\cdot\sin(\omega_g\cdot t)\cdot\left(M_f\cdot\sin(\omega_g\cdot t)-S_n+0.5\right)\cdot\left[AL_g\cdot\left(1-k_{bc}\right)-2\cdot AL_\sigma\cdot\left(1+k_{ab}\right)\right]}{L\cdot fs\cdot\left(1-k_{bc}\right)\cdot\left(AL_g+2\cdot AL_\sigma\right)\cdot\left(k_{bc}-2\cdot k_{ab}+1\right)} & if \quad 0.5< d\le 1 \end{cases} \tag{99}$$

The maximum value of the current ripple occurs when $\omega_g.t = \sin^{-1}[3/(4.M_f)]$ and it is given by the following expression.

$$\Delta iL_{\max} = \frac{V_{cd}\cdot\left[AL_g\cdot\left(1-k_{bc}\right)+2\cdot AL_\sigma\cdot\left(1-k_{ab}\right)\right]}{8\cdot L\cdot fs\cdot\left(1-k_{bc}\right)\cdot\left(AL_g+2\cdot AL_\sigma\right)\cdot\left(k_{bc}-2\cdot k_{ab}+1\right)} \tag{100}$$

9.5.1.2 Determining the flux swing and peak flux

The flux ripple is determined by calculating the voltage v_{Fe_a} and v_{Fe_b} present in Figure 99b, as they represent the flux rate in the core leg 'a' and 'b', respectively. Such voltages are a composition of the voltages applied to the windings. Using the superposition principle, one determines the voltages to be:

$$\begin{aligned} v_{Fe\_a} &= \frac{\Delta\phi_a}{\Delta t} = \frac{2\cdot AL_g+AL_\sigma}{4\cdot\left(AL_g+AL_\sigma\right)}\cdot\frac{\left(v_{x'a}+v_{do}\right)}{N} - \frac{AL_\sigma}{4\cdot\left(AL_g+\dfrac{AL_\sigma}{2}\right)}\cdot\frac{\left(v_{x'b}-v_{oc}\right)}{N} \\ v_{Fe\_b} &= \frac{\Delta\phi_b}{\Delta t} = \frac{2\cdot AL_g+AL_\sigma}{4\cdot\left(AL_g+AL_\sigma\right)}\cdot\frac{\left(v_{x'b}-v_{oc}\right)}{N} - \frac{AL_\sigma}{4\cdot\left(AL_g+\dfrac{AL_\sigma}{2}\right)}\cdot\frac{\left(v_{x'a}-v_{do}\right)}{N} \end{aligned} \tag{101}$$

Observing Figure 99b applying circuit laws, one can easily find $v_{Fe\_g} = v_{Fe\_a} + v_{Fe\_b}$.

$$v_{Fe\_g} = \frac{\Delta\phi_g}{\Delta t} = \frac{2\cdot AL_g+AL_\sigma}{4\cdot\left(AL_g+AL_\sigma\right)}\cdot\frac{\left(v_{x'a}+v_{x'b}-v_{oc}+v_{do}\right)}{N} - \frac{AL_\sigma}{4\cdot\left(AL_g+\dfrac{AL_\sigma}{2}\right)}\cdot\frac{\left(v_{x'a}+v_{x'b}-v_{oc}-v_{do}\right)}{N} \tag{102}$$

If one considers $AL_g >> AL_\sigma$, (101) and (102) can be simplified to:

$$
\begin{aligned}
v_{Fe\_a} &= \frac{\Delta\phi_a}{\Delta t} = \frac{1}{2}\cdot\frac{\left(v_{x'\mathrm{a}} + v_{do}\right)}{N} \\
v_{Fe\_\mathrm{b}} &= \frac{\Delta\phi_b}{\Delta t} = \frac{1}{2}\cdot\frac{\left(v_{x'b} - v_{oc}\right)}{N} \\
v_{Fe\_\mathrm{g}} &= \frac{\Delta\phi_g}{\Delta t} = \frac{1}{2}\cdot\frac{\left(v_{x'\mathrm{a}} + v_{x'b} - v_{oc} + v_{do}\right)}{N}
\end{aligned}
\tag{103}
$$

Figure 100 presents the voltages needed to determine the flux rate in two scenarios: $0 < d < 0.5$ (left side); $0.5 < d < 1$ (right side) with the carriers used to generate the gating signals of all involved switches. Notice that the time intervals, differently from Figure 95, now have four new time subdivisions caused by the phase shift between the primary and secondary sides of the converter.

The calculation of (103) requires the determination of v_{oc} and v_{do} (97) which require $v_{x'a}$, $v_{x'b}$ and v_{cd} presented in Figure 100a. Figure 100c presents the voltages that drive the flux change in both core legs *a* and *b*, ½ ($v_{x'a}$ +v_{do}) and ½ ($v_{x'b}$ +v_{oc}) respectively. Based on then, the fluxes Φ_a and Φ_b is presented in Figure 100g together with the resultant flux in the central leg, Φ_g. Considering $AL_g >> AL_\sigma$ and applying (97) to (103) one obtains:

$$
\begin{aligned}
\frac{\Delta\phi_a}{\Delta t} &= \frac{1}{4}\cdot\frac{\left(3\cdot v_{x'\mathrm{a}} + v_{x'b} - v_{cd}\right)}{N} \\
\frac{\Delta\phi_b}{\Delta t} &= \frac{1}{4}\cdot\frac{\left(v_{x'\mathrm{a}} + 3\cdot v_{x'b} + v_{cd}\right)}{N} \\
\frac{\Delta\phi_g}{\Delta t} &= \frac{v_{x'\mathrm{a}} + v_{x'b}}{N}
\end{aligned}
\tag{104}
$$

Notice from Figure 100g that the flux increase occurs in time intervals Δt_1 and $\Delta t_{1\varphi}$ for Φ_a and Δt_3 and $\Delta t_{3\varphi}$ for Φ_b. Based on this fact and considering $v_g = V_g\cdot\sin(\omega_g\cdot t)$, one obtains the flux ripple variating with the grid frequency:

$$
\Delta\phi_{a(b)} = \begin{cases}
\dfrac{V_{dc}\cdot\left[M_f\cdot\sin(\omega_g\cdot t)\cdot\left(\varphi/2\cdot\pi - M_f\cdot\sin(\omega_g\cdot t) + S_n\right) - \varphi/2\cdot\pi\right]}{N\cdot fs} & if \quad 0.75 < M_f < 1 \\
\dfrac{V_{dc}\cdot M_f\cdot\sin(\omega_g\cdot t)\cdot\left(M_f\cdot\sin(\omega_g\cdot t) - S_n + \varphi/8\cdot\pi\right)}{N\cdot fs} & if \quad 0.5 < M_f \le 0.75
\end{cases}
\tag{105}
$$

When the modulation index M_f is greater than 0.75, the flux rate of the time interval $\Delta t_{4\varphi}$ becomes positive and needs to be considered. This leads to a different equation but the results are very similar.

In the case of the central leg, the flux rate is mathematically identical to the flux rate obtained for the central leg of the integrated interleaved transformer (Section 9.4). Therefore, (87) is also valid in this case.

The flux variation is superimposed to a low-frequency flux changing according to the input current. The currents in windings ‘a’ and ‘b’ contain such low-frequency component. Conversely, the current in windings ‘c’ and ‘d’ doesn’t present this component. This means that the low-frequency flux component is generated only by windings ‘a’ and ‘b’ and therefore, it is calculated in a similar way to (88), considering $i_{a,lf} = i_{b,lf}$.

$$\Phi_{a(b),lf} = \frac{L \cdot (1 - k_{ab}) \cdot i_{a(b),lf}}{N} \tag{106}$$

The maximum flux is achieved when $\omega_g \cdot t = \pi/2$:

$$\Phi_{a(b),\max} \underset{\omega_g \cdot t = \pi/2}{=} \begin{cases} \dfrac{L \cdot (1 - k_{ab}) \cdot I_{a(b)pk}}{N} + \dfrac{(1 - M_f) \cdot M_f \cdot V_{dc}}{2 \cdot fs \cdot N} - \dfrac{V_{dc} \cdot \varphi}{16 \cdot \pi \cdot N \cdot fs} & 0.5 < M_f < 0.75 \\ \dfrac{L \cdot (1 - k_{ab}) \cdot I_{a(b)pk}}{N} + \dfrac{(1 - M_f) \cdot M_f \cdot V_{dc}}{2 \cdot fs \cdot N} - \dfrac{(1 - M_f) \cdot V_{dc} \cdot \varphi}{4 \cdot \pi \cdot N \cdot fs} & M_f > 0.75 \end{cases} \tag{107}$$

As expected, the maximum flux for the central leg is the same given in (91).

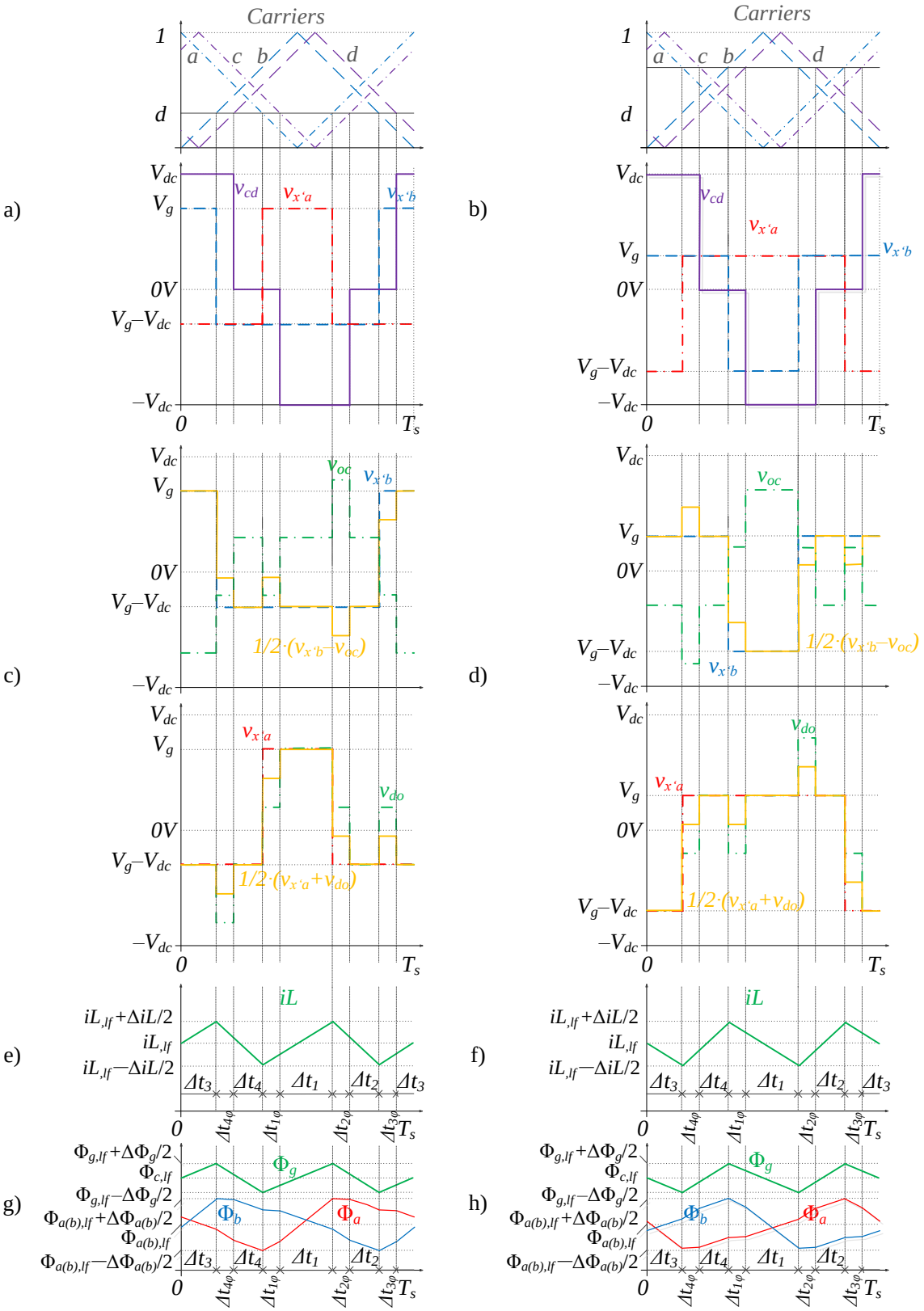
9.5.2 Design

To construct this device an E 55/28/25 core with an air gap of 2.6 mm was already available. The two essential design parameters used for this device are the longitudinal inductance and the energy transfer inductance. The longitudinal inductance is calculated based on (34) for a 35% input current ripple (2.36 A). The required value is then 352 µH. Since the same core type was used, the longitudinal inductance is determined in the same way as for the integrated interleaved transformer. This means one uses (75) to determine the number of turns needed and verify the flux density limits using (91) and (107). The Table 37 presents the design parameters for the integrated transformer.

The manufactured device is presented in Figure 101. To achieve the required leakage inductance of 108 µH for this device, the knowledge of Section 9.3 was applied.

A small ferromagnetic segment (I 20/14/2.3 - 20.1mm x 14.07mm x 2.26mm) was inserted between the primary and secondary sides’ windings as presented in Figure 101a. The obtained leakage inductance is 112 µH and the longitudinal inductance is 412 µH (both are

Figure 100 –.Voltages applied to the integrated inductor windings, currents and fluxes: a) and b) show voltages v_{an} and v_{bn}; the voltages applied to the windings are presented in c) and d); e) and f) present the currents i_a and i_b; g) and h) present the fluxes.



Source: Author.

small signal measurements performed with HAMEG – HM8118). The constructed device is presented in Figure 101b.

Table 37 – Designed parameters for the integrated transformer.

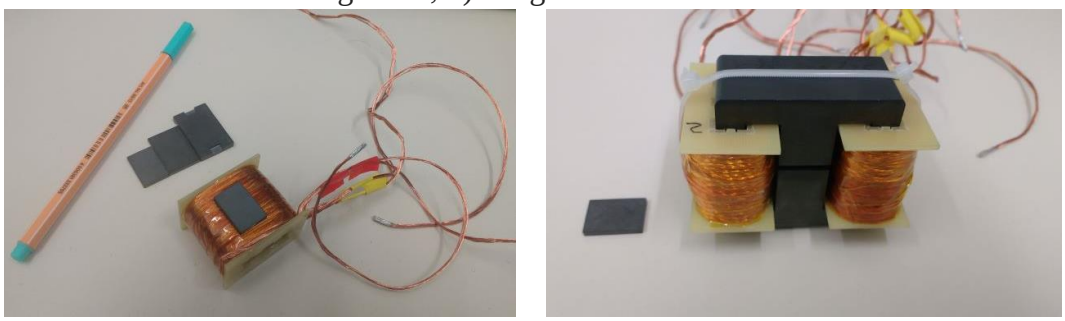
Parameter	**Description**
ΔiL (35%)	2.36A
Longitudinal inductance (L_{LC})	352 µH
Leakage inductance (L_{leak})	108 µH
Core	E 55/28/25
Cross section area	420 mm^2
Air gap (central leg)	2.6 mm
Inductance factor core (AL_{Fe})	7.3 µH
Inductance factor air gap (AL_g)	0.361 µH
Material	Mf 102 – Tridelta
Saturation flux density (B_{sat})	0.5 T
Low frequency density peak flux for legs ‘a’, ‘b’ and ‘g’	0.17 T
Peak flux density for legs ‘a’ and ‘b’ ($B_{a(b)max}$)	0.26 T
Peak flux density for leg ‘g’ (B_{gmax})	0.23 T
Coupling factor (k_{ab})	0.95197
Coupling factor (k_{bc})	0.99812
Self-inductance (L_a and L_b)	14.389 mH
Current ripple frequency	60 kHz
Current density	4 A/mm^2
Winding	90 x 0.1 mm

Source: Author.

9.5.3 Experimental results

Figure 102 shows the experimental results obtained for the converter FB-FB with the integrated magnetics. Figure 102a shows the converter primary side variables. Notice that the winding current i_a of the primary side contains the low-frequency component which is half

Figure 101 – Manufactured magnetic device: a) winding with the ferromagnetic segment in place and the other available segments; b) integrated device manufactured with E 55/28/25;



a) b)

Source: Author.

of the input current *iL* added to the integrated transformer high-frequency current i_{leak}. Power factor correction is achieved with PF = 0.99. Figure 102c shows the input current ripple of 2.12A which results in 394 µH of effective inductance. The THD obtained was 12.45%. The DC voltage was controlled on 400V.

Figure 102c presents the controlled DC voltage of the secondary side. The current i_{leak} is the current in the winding of the integrated transformer device which presents no low-frequency component. The current $i_{c'}$ is the current in the winding of the integrated interleaved transformer. Figure 102d presents the voltages and current in the transformer for a duty cycle near to 0.5. The voltage V_{ac2} imposed on the load is sinusoidal and present a THD of 2.85%. Figure 102e and Figure 102f present the response of the converter to a load step. The changes occur in time instant t_0, when the load is raised from 0.5 to 1.0 p.u., and in t_1, when the load returns to 0.5 p.u. The power change modifies all currents (t_0), which leads to perturbation of the voltages V_{dc1} and V_{dc2}. Both DC voltages are controlled in within 200 ms. Notice that, despite the load change, the output voltage V_{ac2} suffers no perturbation.

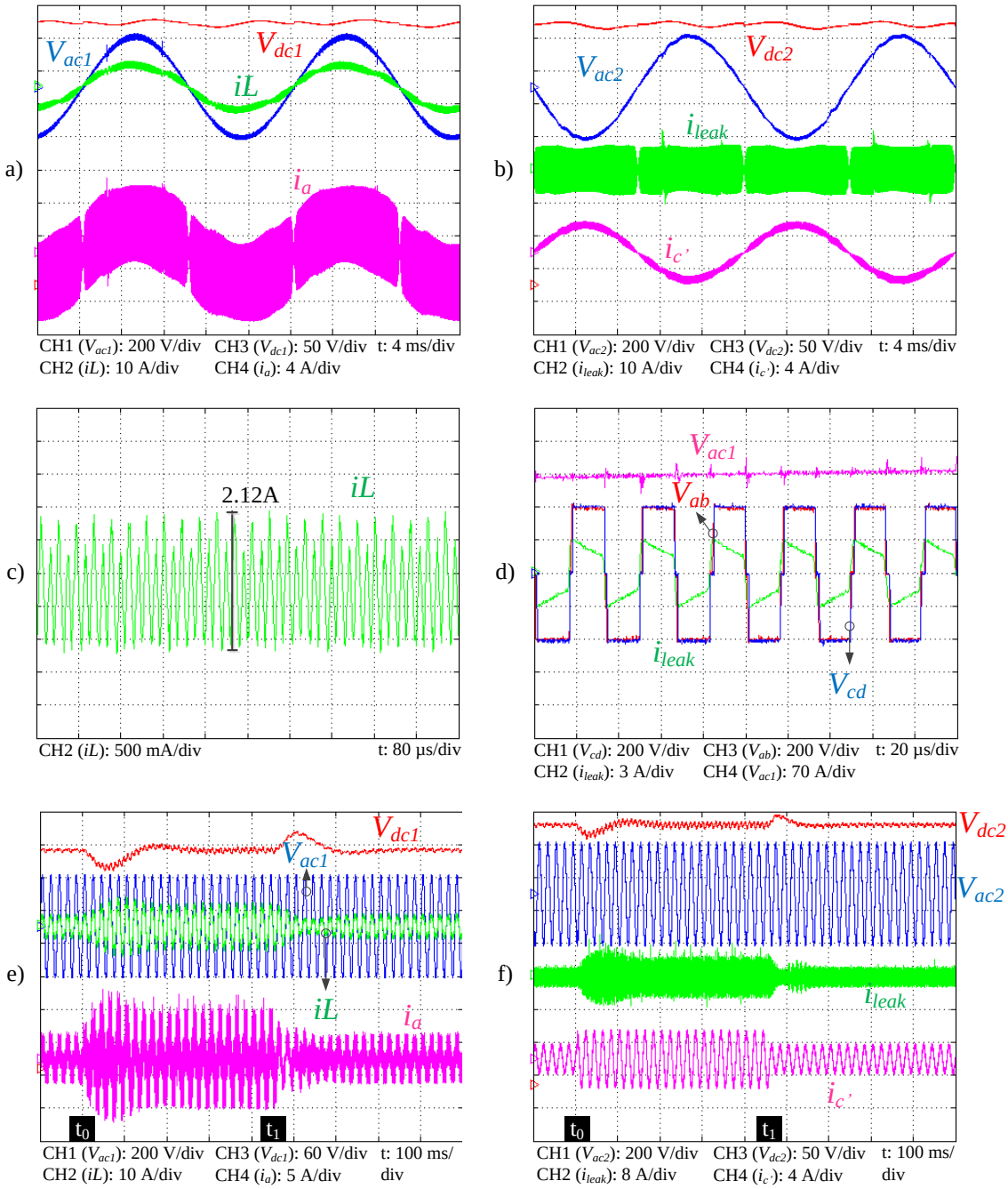
9.5.4 Comparison between integrated and individual magnetic devices solutions

The comparison focused on the volume and efficiency of both integrated and individual solutions when applied to the Symmetric Full-bridge topology. Figure 103a presents the magnetic devices involved in the comparison.

The upper row presents all the individual magnetic devices needed by the SFB converter to work while the bottom row of devices presents the integrated solution. In the upper row, from left to right they are the input inductor, interleaving transformer, high-frequency isolation transformer, another interleaving transformer and the inductor for the LC filter. Although it is named as an individual solution, the transformer was constructed with the required leakage inductance already integrated as presented in Section 9.3. The bottom row consists of the integrated transformer (left) and the integrated interleaved transformer (right). Notice that these two devices replace all devices of the upper row (five devices).

Figure 103b presents the efficiency obtained for different power levels for the SFB running with the individual and integrated magnetics. The efficiency of the integrated solution is superior to the individual solution on all tested power levels. Figure 103c shows the volume comparison (boxed volume) between the integrated and individual solution.

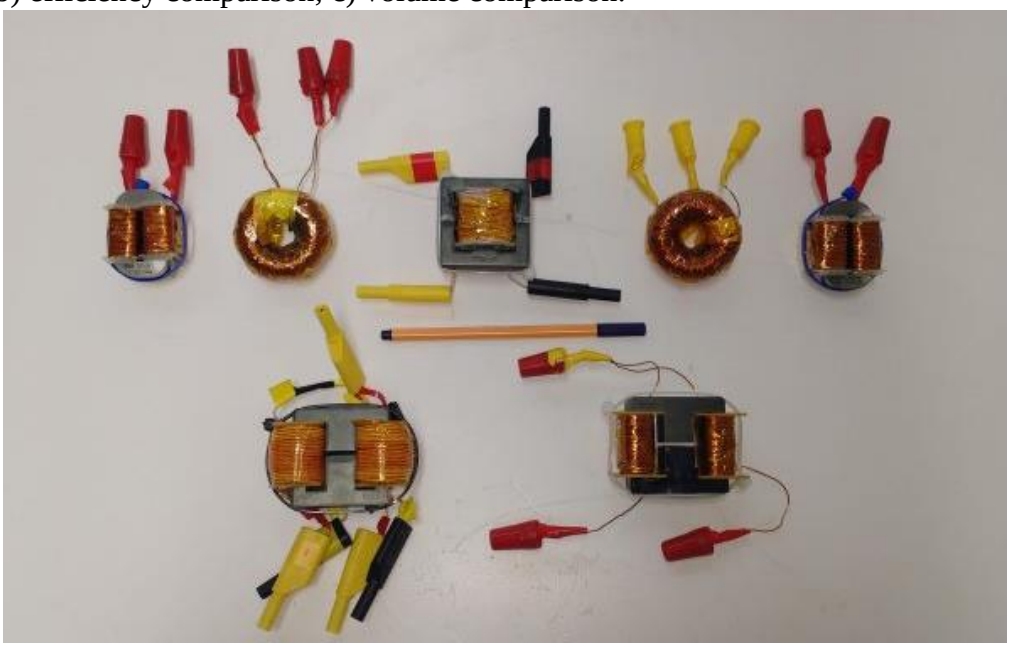
Figure 102 – Experimental results for 1 kW: a) input voltage and current, DC voltage and current i_a; b) output voltage, DC voltage, transformer current and integrated interleaved transformer winding current; c) input current ripple; d) transformer related variables; e) and f) show the dynamic response of the primary and secondary variables respectively, of load step from 0.5 to 1.0 p.u. at t_0 and back to 0.5 p.u. at t_1.



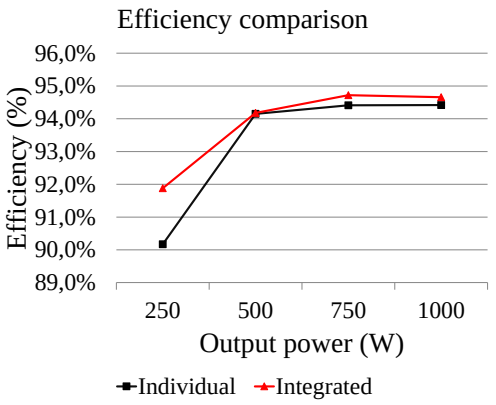
Source: Author.

Even though the transformer of the individual solution has a certain level of integration, the integrated solution presented a smaller volume.

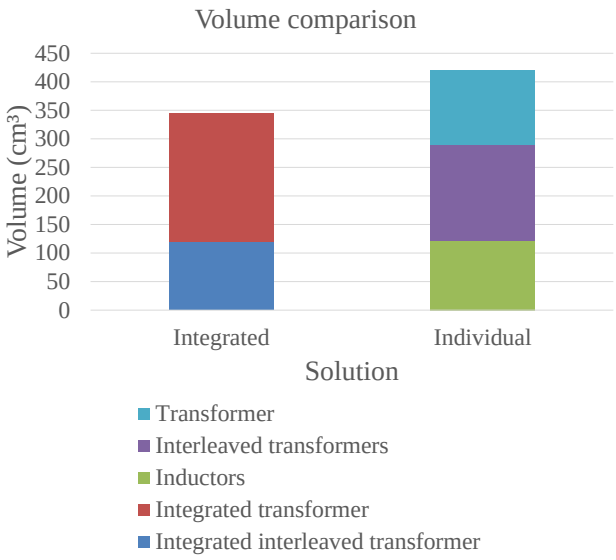
Figure 103 – Comparative view of the integrated and individual magnetics: a) discrete five magnetic devices (upper row) and the two designed integrated magnetic devices (bottom row); b) efficiency comparison; c) volume comparison.



a)



b)



c)

Source: Author.

10 CONCLUSIONS

This thesis presented a new family of single-phase isolated AC-AC converters applicable to voltage regulators, Dynamic Voltage Restorers, and Uninterruptible Power Supplies. The proposed converters are able to control the AC load voltage, the input power factor, and the DC-link voltages. The family is composed of three symmetric topologies and six asymmetric topologies. All converters topologies were simulated and six of them were tested using an experimental platform developed in the University of Kassel. In addition, two integrated magnetic devices were developed and tested comparing the volume and converter efficiency. The dynamic response of the converters was tested through the load step and voltage sag tests.

The SHB topology presents the smallest number of switches among the converter of the family. It uses half of the DC-link voltage in both converter sides to compose the input and output voltages. The experimental results showed high losses in the DC-link capacitors due to the low-frequency current flow. Therefore, this topology is indicated to low power applications.

The SFB topology uses twelve switches and takes advantage of the complete DC-link voltage in both converter sides. The four additional semiconductors divert the capacitor low frequency current of the SHB topology and are switched at the grid frequency, improving the converter efficiency. The result is that this converter topology presented the best efficiency among all converters of the proposed family.

The SIFB topology employs the highest number of switches (sixteen switches) and magnetic devices but presents an effective frequency in the input/output passive elements, which is four times the switching frequency. This topology makes possible to use the same duty cycle function in both sides of the transformer, which reduces the transformer current employing a scheme named partial actuator. Differently from the SFB, in this converter, the low-frequency current component in all switches is half of the input current, which accredits it to high current applications.

The combination of the HB and the IFB arrangements generates two converters. They can use the partial actuator scheme to obtain reduced transformer current since the duty cycle functions applied to both converter sides is the same. In terms of efficiency, the converters are located between the SHB and the SFB converters.

The FB and HB arrangements form other two converters of the family. The arrangements HB and FB present naturally different duty cycles, which generates a high voltage difference in the leakage inductance increasing the transformer current. In order to solve this problem, a new modulation scheme for the FB arrangement was proposed. In this new modulation, all semiconductors operate at high frequency. This makes possible the duty cycle of the HB arrangement to be used by the FB arrangement eliminating the high voltage difference in the leakage inductance and ensuring low current in the transformer. The drawbacks of this approach include high WTHD of the generated voltage and high current ripple. In addition, ferrite core inductors replaced the AMCC core inductors to reduce the inductors losses. However, the obtained efficiency is comparable to the obtained with the SHB converter. Therefore, the proposed modulation is indicated to low power applications. However, another modulation scheme can be proposed in order to minimize this problem.

The last two converters are formed by the FB and IFB arrangements. Both arrangements present different natural duty cycle functions. To reduce the transformer current the duty cycle of one arrangement needs to be used by the other arrangement. Applying the IFB duty cycle function (the same of the HB arrangement) to the FB arrangement resulted in poor WTHD of the generated voltage and high current ripple. The solution is to apply the FB duty cycle function to the IFB arrangement. The result is a reasonable WTHD and current ripple. Therefore, these converters are suitable for high power applications.

Many magnetic devices compose the converters of the family. Most converters need at least six different magnetic elements (two inductors, two interleaved transformers, one transformer, and one energy transfer inductor). The integration of more than one magnetic element into a single device bring losses and volume reduction. Two integrated magnetic devices were designed and tested. As the SFB converter presented the highest efficiency among the family converters, it was used to compare the two designed integrated magnetic devices with their individual counterparts. The results showed a volume reduction and a converter efficiency increase when using the integrated magnetic devices.

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APPENDIX A SCIENTIFIC PRODUCTION

During the doctorate work the following articles were published:

- CIPRIANO DA SILVA FILHO, OLYMPIO; DE SOUZA OLIVEIRA, DEMERCIL. Proposal of a new family of high frequency isolated single-phase AC-AC converters. In: 2016 12th IEEE International Conference on Industry Applications (INDUSCON), 2016, Curitiba. 2016 12th IEEE International Conference on Industry Applications (INDUSCON), 2016. p. 1.
- FILHO, OLYMPIO C. SILVA; DE ALMEIDA, BRUNO R.; OLIVEIRA, DEMERCIL S.; NETO, TOBIAS R. FERNANDES . Loss analysis of a high frequency isolated AC-AC converter applied as voltage regulator. In: 2017 Brazilian Power Electronics Conference (COBEP), 2017, JUIZ DE FORA. 2017 Brazilian Power Electronics Conference (COBEP), 2017. p. 1
- SILVA FILHO, O. C.; ALMEIDA, B. R.; OLIVEIRA, D. DE SOUZA; FERNANDES NETO, TOBIAS RAFAEL. High-Frequency Isolated AC-DC-AC Interleaved Converter for Power Quality Applications. IEEE Transactions on Industry Applications, v. 54, p. 1-1, 2018.

Anlage 6: Der Text der Erklärung gemäß § 8 Abs. 1 Satz 2 lit. d AB-PromO lautet:

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