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DAVI RABELO JOCA

AN AC-DC TOPOLOGY BASED ON AN INTERLEAVED MODULAR MULTILEVEL CONVERTER FEASIBLE TO SOLID-STATE TRANSFORMER APPLICATIONS

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Tese apresentada ao Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal do Ceará, como requisito parcial à obtenção do título de Doutor em Engenharia Elétrica. Área de concentração: Sistemas de energia elétrica.

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DAVI RABELO JOCA

AN AC-DC TOPOLOGY BASED ON AN INTERLEAVED MODULAR MULTILEVEL CONVERTER FEASIBLE TO SOLID-STATE TRANSFORMER APPLICATIONS

Thesis presented to the Doctoral Course in Electrical Engineering of the Electrical Engineering Department of Federal University of Ceará as part of the requirements for obtaining the title of Doctor of Philosophy (Ph.D.) in Electrical Engineering. Concentration Area: Electric Power Systems.

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RESUMO

Este trabalho tem como objetivo apresentar o estudo teórico, a análise numérica e a validação experimental de uma topologia de conversor eletrônico de potência a partir de um conversor multinível modular entrelaçado com transformador de média frequência. A arquitetura é adequada para o estágio CA-CC em aplicações de transformador de estado sólido para a conexão entre uma rede CA de média tensão e uma rede CC de baixa tensão. O entrelaçamento reduz as perdas de condução dos interruptores. O transformador de frequência média de 10 kHz fornece isolamento galvânico e conecta o conversor multinível modular entrelaçado a um conversor de ponte completa. A partir da estrutura do conversor, o princípio de operação, a modelagem, a técnica de modulação e o esquema de controle são discutidos. Uma característica do conversor é a geração simultânea da tensão da rede de baixa frequência e a tensão primária do transformador de média frequência. O balanceamento de tensão dos capacitores e a minimização das correntes circulantes são combinados em um único algoritmo. O sistema de controle regula a corrente CA e a tensão do barramento CC, no lado de alta tensão, e a tensão CC e o fluxo de energia, no lado de baixa tensão. A validação experimental do conversor é feita com um protótipo monofásico em escala reduzida de 720 W. Os resultados demonstram a estabilidade do sistema de controle em operações estáticas e dinâmicas (comutação de carga, inversão de fluxo de potência).

Palavras-chave: conversor CA-CC isolado, conversor multinível modular, entrelaçamento, modulação vetorial, transformador de estado sólido.

ABSTRACT

This work aims to present the theoretical study, the numerical analysis and the experimental validation of a power electronics converter topology based on an interleaved modular multilevel converter with medium-frequency transformer. The architecture is suitable for the AC-DC stage in solid-state transformer applications for the connection between a medium-voltage AC grid and a low-voltage DC grid. The interleaving reduces the switch conduction losses. The 10 kHz medium-frequency transformer provides galvanic isolation and connects the interleaved modular multilevel converter to a full-bridge converter. From the converter structure, the principle of operation, the modeling, the modulation technique, and the control scheme are discussed. One feature of the converter is the simultaneous generation of the low-frequency grid voltage and the medium-frequency transformer primary voltage. The capacitor voltage balancing and the circulating currents minimization are combined together in a single algorithm. The control system regulates the AC current and the DC bus voltage, on the high-voltage side, and the DC voltage and power flow, on the low voltage side. The experimental validation of the converter is made with a scaled-down single-phase 720 W prototype. The results demonstrate the control system stability in steady-state and dynamic (load step, power flow inversion) operations.

Keywords: interleaving, isolated AC-DC converter, modular multilevel converter, solid-state transformer, space vector modulation.

RÉSUMÉ

Ce travail concerne l'étude théorique, l'analyse numérique et la validation expérimentale d'une topologie de convertisseur d'électronique de puissance basée sur un convertisseur multiniveau modulaire entrelacé avec transformateur moyenne fréquence. L'architecture est adaptée pour l'étage de conversion AC-DC dans les applications de transformateur d'électronique de puissance pour la connexion entre un réseau alternatif moyenne tension et un réseau continu basse tension. L'entrelacement réduit les pertes par conduction dans les interrupteurs. Le transformateur moyenne fréquence 10 kHz assure une isolation galvanique et connecte le convertisseur multiniveau modulaire entrelacé à un convertisseur pont complet. Avec comme point de départ la structure, le principe de fonctionnement, la modélisation, la technique de modulation et le schéma de commande sont discutés. Une caractéristique du convertisseur est la génération simultanée de la tension du réseau basse fréquence et de la tension primaire du transformateur moyenne fréquence. L'équilibrage de la tension des condensateurs et la minimisation du courant de circulation sont combinés dans un seul algorithme. La commande régule le courant alternatif et la tension du bus continu, du côté haute tension, ainsi que la tension continue et le flux de puissance, du côté basse tension. La validation expérimentale du convertisseur est réalisée avec un prototype de 720 W monophasé à l'échelle réduite. Les résultats démontrent la stabilité du système de commande lors d'opérations en régime permanent et dynamiques (pas de charge, inversion du flux de puissance).

Mots clés: Convertisseur CA-CC isolé, convertisseur modulaire multiniveau, entrelacement, transformateur d'électronique de puissance, modulation vectorielle spatiale.

LIST OF ABBREVIATIONS AND ACRONYMS

AC	Alternating Current
ANEEL	Agência Nacional de Energia Elétrica
CCM	Circulating Currents Minimization
CHB	Cascaded H-Bridge
CVB	Capacitors Voltage Balancing
DC	Direct Current
DSP	Digital Signal Processor
FBC	Full-Bridge Converter
FC	Flying Capacitor
FPGA	Field-Programmable Gate Array
HBSM	Half-Bridge Submodule
HV	High Voltage
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
HVS	High-Voltage Side
IEEE	Institute of Electrical and Electronics Engineers
IMMC	Interleaved Modular Multilevel Converter
LV	Low Voltage
LVAC	Low Voltage Alternating Current
LVDC	Low Voltage Direct Current
LVS	Low-Voltage Side
MFT	Medium-Frequency Transformer
MIT	Massachusetts Institute of Technology
MMC	Modular Multilevel Converter
MV	Medium Voltage
MVAC	Medium Voltage Alternating Current
MVDC	Medium Voltage Direct Current
M^2LC	Modular Multi Level Converter
NPC	Neutral-Point Clamped
PI	Proportional Integrator
PRODIST	Procedimentos de Distribuição de Energia Elétrica no Sistema Elétrico Nacional
RMS	Root Mean Square
SHE-PWM	Selective Harmonic Elimination Pulse-Width Modulation

SST	Solid-State Transformer
STATCOM	Static Synchronous Compensators
THD	Total Harmonic Distortion
THDi	Current Total Harmonic Distortion
THDv	Voltage Total Harmonic Distortion
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

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1 INTRODUCTION

1.1 Context

In the last decade, the smart grids topics are attracting a considerable interest from academia and industry. Researchers recognize this technology as an improvement of the three main stages that constitute the power system scheme (generation, transmission and distribution), contributing to the increase of its reliability and efficiency. The future electric system considers the new resources and load characteristics, such as energy storage systems (batteries, supercapacitors, etc.), renewable energy sources (photovoltaic panels, wind turbines, etc.), electric vehicles and electronic loads (TVs, LED lights, computers, etc.) (JHUNJHUNWALA; LOLLA; KAUR, 2016) (NORDMAN; CHRISTENSEN, 2016).

Within the current power system architecture, the power transformers play a key role with the galvanic isolation and the voltage level adjustment. This voltage may subsequently be reduced to distribution voltage levels for industrial, commercial and residential purposes (SHE *et al.*, 2013). In Brazil, the connection of AC (alternating current) distributed generation to the utility grid is regulated by the PRODIST norm, from the National Agency of Electric Energy - ANEEL (2016, p. 30). The PRODIST - Module 3 norm states that the distribution voltage levels are divided into:

- High-voltage (HV): 69 kV or 138 kV;
- Medium-voltage (MV): 13.8 kV or 34.5 kV;
- Low-voltage (LV): 127 V to 440 V.

Also, the PRODIST - Modules 3 and 8 norms regard to the connection proceedings and the energy quality, respectively, which state that for a generator with 75 kW or higher (ANEEL, 2016, p. 38):

- The connection must be made to the three-phase low-voltage AC grid (220 V or 380 V) or to the medium-voltage AC grid (13.8 kV);
- The connection point voltage must respect the nominal voltage limits (V_n ±5%)
- A coupling transformer must be used;
- When in islanded mode operation, both voltage and frequency at the connection point must be controlled;

- The power factor at the connection point must be higher than 0.92 (inductive or capacitive);
- The voltage total harmonic distortion (THD_v) must be between the limits described in Table 1.1 (ANEEL, 2017, p. 15).

Table 1.1 – Limits for THD (% of the fundamental voltage).

Parameters	**Nominal voltage (V_n)**		
	$V_n \leq 1$ kV	**1 kV < V_n < 69 kV**	**69 kV ≤ V_n ≤ 230 kV**
THD_v	10%	8%	5%
*$THD_{v,even}$	2.5%	2%	1%
**$THD_{v,odd}$	7.5%	6%	4%
***$THD_{v,3}$	6.5%	5%	3%

*All even-order harmonics, non-multiple of 3.

**All odd-order harmonics, non-multiple of 3.

***All order harmonics multiple of 3.

Source: PRODIST – Module 8 norm – ANEEL (2017, p. 15).

Also, according to the recommended requirements for harmonic control in electrical systems, IEEE STD 519-2014 (2014, p. 7), the generators must meet the current total harmonic distortion (THD_i) limits for the grid connection, as shown in Table 1.2. In this standard, each current harmonic component should be measured and limited (suppressed in Table 1.2).

Table 1.2 – Limits for THD_i (% of the fundamental frequency component).

Parameters	**Nominal voltage (V_n)**		
	120 V < V_n < 69 kV	**69 kV < V_n ≤ 161 kV**	**161 kV < V_n**
*$THD_{i,1}$	5%	2.5%	1.5%
**$THD_{i,2}$	20%	10%	3.75%

*Scenario when short-circuit current is up to 20 times the nominal current.

**Scenario when short-circuit current is higher than 50 times the nominal current.

Source: IEEE STD 519-2004 (2014, p. 7-9).

For the connection of DC (direct current) microgrids to the utility grid, there is no norm yet, but it is expected that a similar regulation will be applied.

The development trends of traditional low-frequency power transformers aim to improve their aspects related to material engineering, insulation, and manufacturing processes, while taking into account economic and environmental factors (SHE *et al.*, 2013) (RODRIGUEZ *et al.*, 2017). Since the transformer frequency of operation is inversely proportional to its volume, the trend is to increase the frequency. According to its frequency operation, the transformers can be classified as follows (KOLAR; ORTIZ, 2014):

- Low-frequency: below 1 kHz
- Medium-frequency: 1 kHz to 100 kHz
- High-frequency: higher than 100 kHz

The advance of the power devices and power electronics brought back once again the attention for the use of DC power distribution in modern power systems, which could be highly convenient along with the AC power distribution systems. Focusing on the microgrids, one of good advantages of using DC power distribution is the elimination of unnecessary power conversion stages, which increases the overall efficiency. Besides that, the absence of reactive power and the lack of synchronization makes the system more efficient and simple to control (RODRIGUEZ-DIAZ *et al.*, 2016) (SHE *et al.*, 2012).

The connection of distributed generations between AC and DC distribution lines places a great challenge on the control and protection system (HUANG, 2016). Firstly, the galvanic isolation and the voltage level adjustment are mandatory features. Therefore, there is a strong need to provide technology which can manage the power and allow an easy connection. In order to achieve this, it is necessary to have a reliable and fast voltage control in the network (ZHAO *et al.*, 2013). One of the options is the solid-state transformer (SST) technology.

1.2 SST concepts

The solid-state transformer (BOWERS *et al*, 1980), also called “intelligent universal transformer” (LAI *et al.*, 2005) or “electronic transformer” (BIFARETTI *et al.*, 2011), is considered to be the evolution of the traditional power transformer. Recognized as one of the ten most emerging technologies by the Massachusetts Institute of Technology (MIT) Technology Review in 2010 (SHE; HUANG; BURGOS, 2013), its oldest conception was presented by McMurray (1970).

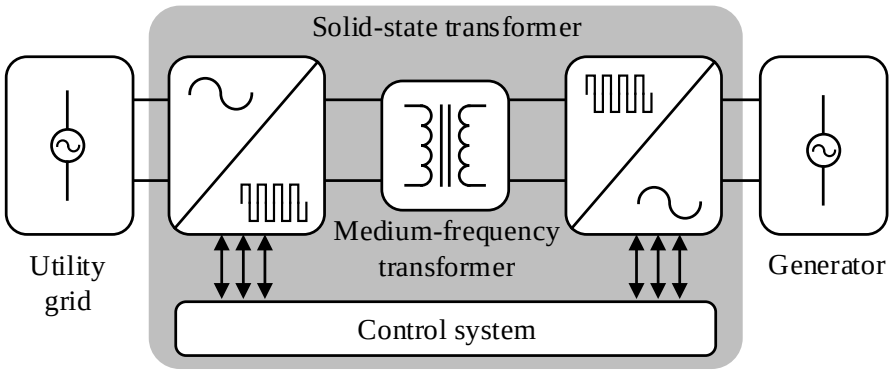
Currently, there isn´t a standard conceptual definition concerning the SST configurations, but they are mostly considered as an AC-AC conversion device. However, Falcones, Ayyanar and Mao (2013), Qin and Kimball (2014), Rodriguez *et al.* (2017), Huber *et*

al. (2017), Barreto *et al.* (2018), and other authors classify the SST as a multistage topology, *i.e.*, a structure with one or more conversion stages (AC-DC, DC-DC, DC-AC or AC-AC) followed by galvanic isolation and voltage level adjustment features. This is important to mention because some AC-DC SST topologies are applied in DC power distribution applications, as well as tractions auxiliary supplies and data-centers applications (HUBER *et al.*, 2017).

The SST includes a set of semiconductor components, a medium to high-frequency transformer and a control system, as an example shown in Figure 1.1. The SST has the same basic function than a traditional transformer: raise or reduce AC voltage levels and galvanic isolation. However, it has several advantages (TATCHO; JIANG; LI, 2011) (QIN; KIMBALL, 2013) (HUBER; KOLAR, 2014) (ZHAO *et al.*, 2017):

- Both input and output terminals can operate in direct current or alternating current;
- The voltage, current and frequency levels can be actively modified, so that it allows for bidirectional power flow control;
- Reactive energy compensation and active harmonic filtering can provide high quality voltage waveforms and improve the processed energy;
- Voltage drops and fault current limitation can be regulated by means of the control and protection system;
- The direction of the energy of any source (the concessionaires, the consumer and other transformers in the grid) to any destination can be managed by the most efficient possible route;

Figure 1.1 – Solid-state transformer configuration.



Source: author's right.

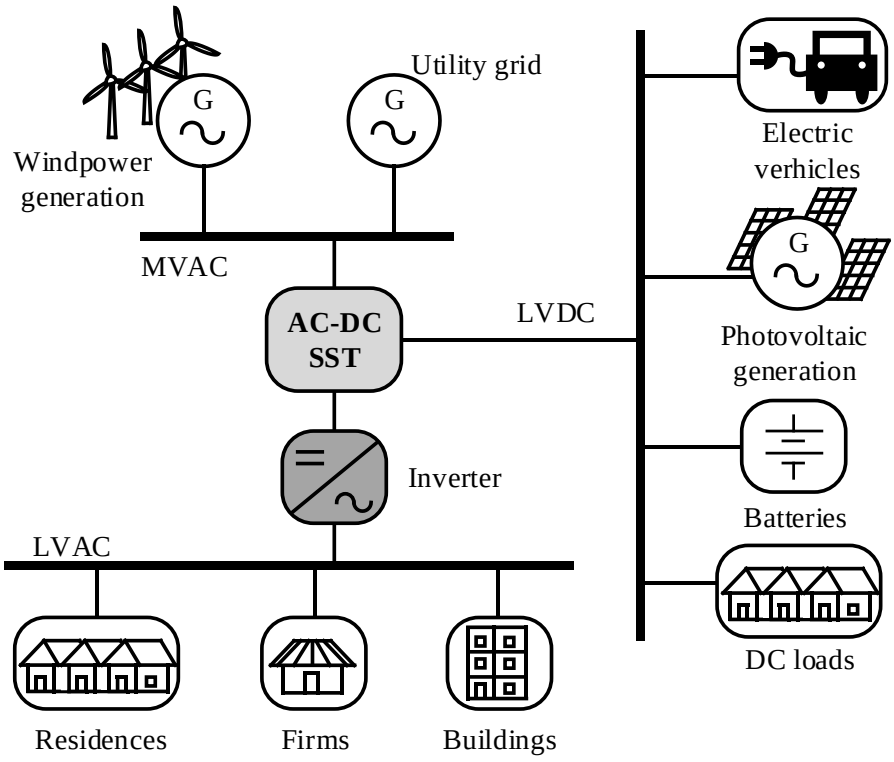
- The operating frequency is rated at the order of tens of kilohertz, thus, its intrinsic dimensions are greatly reduced if compared to their conventional counterparts;
- The control system allows dynamic and stable operations, managing the flow of energy between DC and AC energy systems, in medium-voltage and low-voltage (LV) generation centers and loads.

Therefore, these SST features are clearly adequate to the context of power distribution systems and smart grids.

With these features, some studies suggest that when SSTs will be implemented, the manner how electricity is distributed will be radically modified, and the SSTs will become key components in the future smart grids (DRAGIČEVIĆ, 2016).

One example is shown in Figure 1.2, which presents a smart grid architecture with an AC-DC SST. The energy flow is managed between the MVAC (Medium-Voltage Alternating Current) and LVDC (Low-Voltage Direct Current) grids, allowing generation centers and load characteristics to work together. Also, through an inverter, the common LVAC (Low-Voltage Alternating Current) grids can still be connected to the smart grid (WANG *et al.*, 2013).

Figure 1.2 – Example of an AC-DC SST applied in a smart grid architecture.



Source: author's right.

However, the implementation of SSTs is highly complex. Firstly, due to their complex structures, which require a high number of switches, passive elements (diodes, capacitors and inductors), drivers and auxiliary circuits. These elements together with the voltage and current measurements must be controlled by one or more control devices, such as microcontrollers, DSPs (Digital Signal Processor), or FPGAs (Field-Programmable Gate Array) to manage the power flow.

The second challenge is due to the required large number of electronic components, which reliability can be affected if redundancy is not considered (HUANG *et al.*, 2017). The control system must protect the LV side against short circuits. When a fault situation occurs, only the closest upstream protection device should trigger in order to contain the effects (HUBER, KOLAR, 2017).

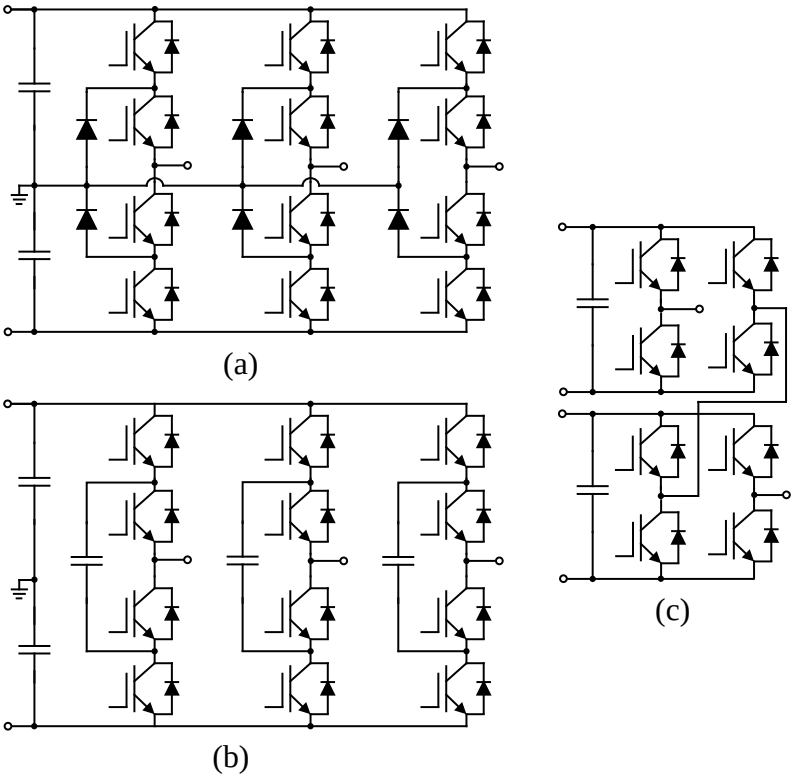
Last but not least, there aren´t SST products that would allow a price comparison against the conventional transformer, but the cost could be probably a future issue. Estimations given by Huber and Kolar (2017) results in a range of 50-250 €/kVA, compared to the conventional transformers, which are around 10-25 €/kVA for a 100-1000 kVA power rating.

1.3 SST topologies for DC power distribution systems

There are several prominent topologies for SST applications, from two-level converters to the multilevel converters, which focus around different applications, topologies, power devices requirements, among others. Examples can be found in Zhao *et al.* (2013), She *et al.* (2013), Madhusoodhanan *et al.* (2015), and Barreto *et al.* (2018). However, since each SST application brings different characteristics to the table, this topic concentrates the attention in review studies focusing on DC power distribution systems, like the ones presented by She *et al.* (2012) and Rodriguez *et al.* (2017).

The multilevel converters have already been recognized as a good option for several medium- and high-voltage industrial applications, and they can be used into the SST conversion stages. Compared to two-level converters, they allow for an increase in the number of voltage levels at the output, which allows the reduction of the harmonic content and, consequently, the filter elements. The most well-known topologies are: NPC (Neutral-Point Clamped) (Figure 1.3a), FC (Flying Capacitor) (Figure 1.3b) and CHB (Cascaded H-Bridge) (Figure 1.3c). Also, other features are provided, as they allow a voltage rise without the need for step-up transformers, high efficiency, voltage and current efforts reduction on semiconductor devices, common mode voltage elimination, among others (SADIGH; DARGAHI; CORZINE, 2015).

Figure 1.3 – Conventional multilevel converters: (a) NPC, (b) FC and (c) CHB.



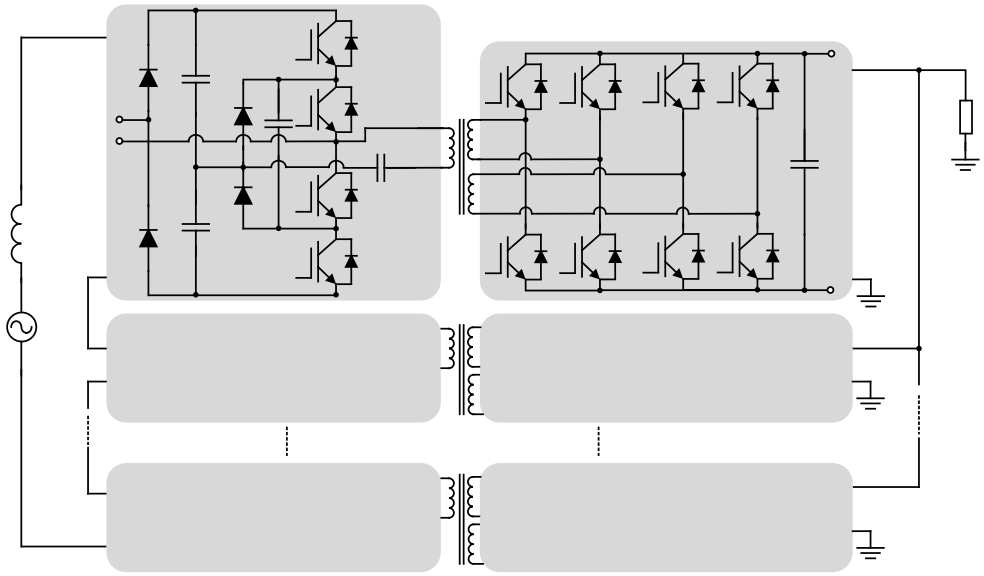
Source: author's right.

Based on the multilevel converters, Rodriguez *et al.* (2017) presented an AC-DC SST topology (Figure 1.4), using a NPC/FC converter connected to the primary of a medium-frequency transformer (MFT). At the two secondary windings, a four-leg full-bridge rectifier was connected to supply the load. Several advantages were addressed such as the single-stage AC-DC structure, ZVS and quasi-ZCS (soft-switching) for the whole operation power range, which increases its efficiency. Among its drawbacks, it doesn´t provide a bidirectional power flow control, which is an important feature for the future power systems.

Also in the family of the multilevel converters, the modular multilevel converter (MMC) was patented by Marquardt (2001) and it is also consolidated in the industry as a suitable solution for HVDC (High Voltage Direct Current) applications (Figure 1.5). Compared to the conventional multilevel converters, it provides additional features such as the modular construction, allowing them to be designed for different voltage levels, current and power (modularity), scalability, bidirectional power flow, and waveforms with low harmonic distortion (GLINKA; MARQUARDT, 2005) (FALCONES; MAO; AYYANAR, 2010) (XIAOTIAN; GREEN, 2015) (HUBER; KOLAR, 2017). The MMCs are used in a wide range of high-power applications, such as medium-voltage motor drives, offshore wind farms, static

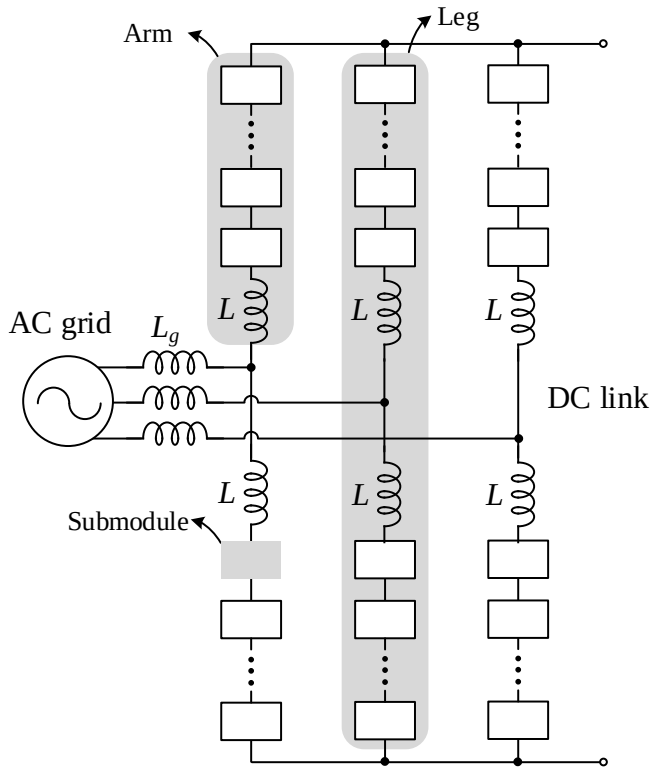
synchronous compensators (STATCOM) and solid-state transformers (DU *et al.*, 2018, p. 23) (SAHOO; MOHAN, 2017).

Figure 1.4 – AC-DC SST for electric DC power distribution systems.



Source: adapted from Rodriguez *et al.* (2017).

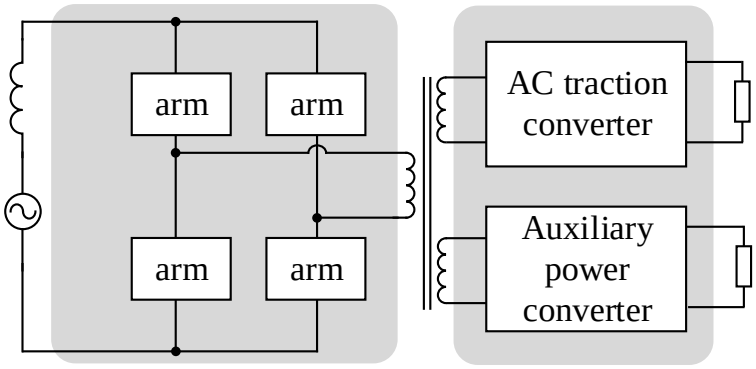
Figure 1.5 – Modular multilevel converter.



Source: adapted from Marquardt (2001).

Also, Glinka and Marquardt (2005) introduced the single-phase M^2LC (Figure 1.6), which is an AC-AC MMC-based converter with two MMC legs connected to a medium-frequency transformer. At the MFT secondary side, there is a conventional AC traction converter (full-bridge rectifier plus an inverter). The topology can be extended to one-phase/three-phase by including an extra phase module. The structure has same advantages of the MMC including the galvanic isolation in medium-frequency, which reduces the transformer size and weight when compared to topologies using conventional 50-60 Hz transformers. Among its drawbacks, there is a large number of switches, increasing the switching losses, the complex structure enhances the controllability, and the cost of its implementation.

Figure 1.6 – Single-phase AC-AC M^2LC topology.



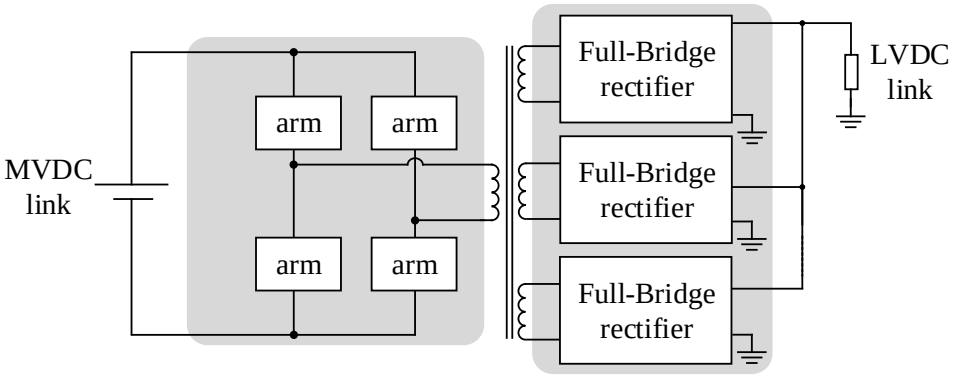
Source: adapted from Glinka and Marquardt (2005).

Similar to the M^2LC, Wang *et al.* (2018) described a single-phase DC-DC structure with two MMC legs connected to the primary of a high-frequency transformer. There are three secondary windings connected to full-bridge converters to feed the load (Figure 1.7). The main idea is to interface a MVDC (Medium-Voltage Direct Current) and a LVDC link between DC distribution networks. Basically, it has the same advantages of the M^2LC including the current sharing among the MMC legs that performs a conduction losses decrease. Among its drawbacks, it has the double number of switches per phase compared to the M^2LC, which increases the structure complexity and the switching losses.

Although all these presented topologies are highly applicable to DC power distribution systems, another group of power converter uses not only the MMC-based structure, but also provides an interleaving feature combined together with the medium-frequency transformer. This interleaving element is called here as “interphase transformer”. The interphase transformer brings some additional advantages to the converter such as the reduction of the total magnetic component size of the input inductor, the low current ripple and the proper

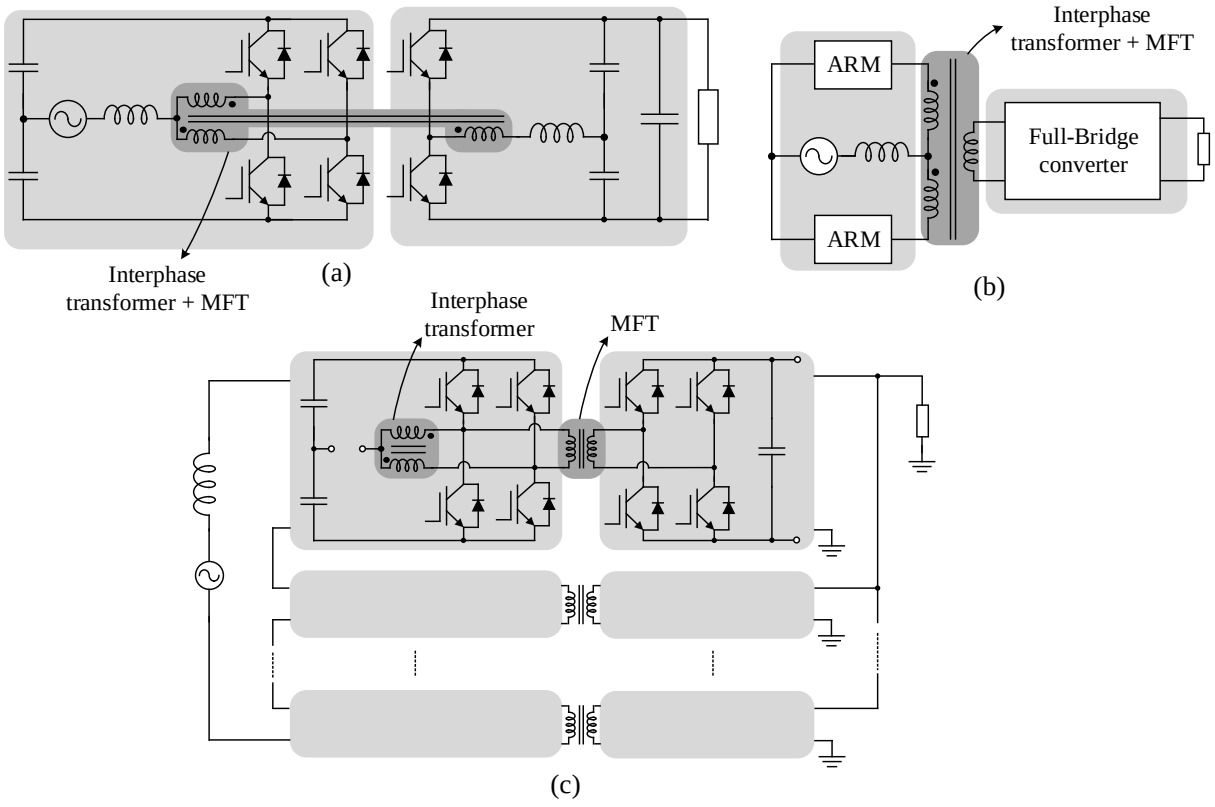
current sharing across the MMC legs (COUGO *et al.*, 2012) (BASCOPÉ; BARBI, 2000). Some examples are introduced by Oliveira Jr. *et al.* (2012), Pacheco *et al.* (2016) and Barreto *et al.* (2018) shown in Figure 1.8.

Figure 1.7 – Single-phase DC-DC MMC-based with high-frequency transformer SST topology for DC power distributions systems.



Source: adapted from Wang *et al.* (2018).

Figure 1.8 – Interleaved MMC-based topologies employed in SST applications: (a) Oliveira Jr. *et al.* (2012), (b) Pacheco *et al.* (2016) and (c) Barreto *et al.* (2018).



Source: adapted from Oliveira Jr. *et al.* (2012), Pacheco *et al.* (2016) and Barreto *et al.* (2018).

Therefore, the use of interleaved modular multilevel converters topologies together with the solid-state transformers employed in DC power distribution systems applications is justified.

1.4 Motivation and constraints

The future power systems challenges and the recent attention around the SST applications in power distribution systems is the motivation behind this PhD research. Thus, an AC-DC SST topology based on an interleaved modular multilevel converter structure is proposed.

The main constraints of the topology are to provide not only the galvanic isolation and voltage level adjustment features, but also including the features provided by the MMC-based structure, the interleaving, and the medium-frequency transformer.

1.5 Thesis objectives

In this context, this thesis presents a novel interleaved modular multilevel converter (IMMC) with a medium-frequency transformer. The proposed topology presents the combined advantages as of conventional MMC, converters with MFT and interleaving. The interleaving technique uses an interphase transformer, which reduces the conduction losses across the legs and the IGBTs ratings reduction. The MFT allows its smaller and lighter footprint. Such converter could be employed in high-power DC power distribution systems, as the AC-DC stage of a SST for example.

One of the major contributions of this thesis is the mathematical modeling of the IMMC, which allows the simultaneous generation of the low-frequency grid voltage and the medium-frequency transformer primary voltage. Also, the capacitor voltage balancing and the circulating currents minimization are combined together in a single algorithm.

In this work, features concerning the converter such as the design procedure, the converter operation and modeling, the modulation technique, the capacitor voltage balancing and circulating currents minimization algorithm, and the control scheme are detailed. In order to validate the concept, the converter has first been simulated for the connection of the medium-voltage utility grid connected to a low-voltage direct current link using a three-phase 100 kW topology. Then a scaled-down single-phase 720 W prototype has been built and tested.

1.6 Outline

The contents of this thesis are organized as follows:

- Chapter 1: a brief background of solid-state transformers for DC power distribution applications was presented: requirements and aspects. It was also presented an overview of the SST topologies for power distribution systems application, besides the thesis contextualization, motivation, and objectives.
- Chapter 2: the study of the proposed converter. The structure, the principle of operation and the modeling provide fundamental concepts to understand and develop the modulation technique, the voltage balancing and circulating currents minimization algorithm, and the control scheme.
- Chapter 3: the analyses of the converter regarding the optimum number of submodules per arm, optimum transformer turns ratio, RMS and THD of the medium-frequency transformer primary voltage and losses. Also, this chapter presents the design methodology and the simulation results.
- Chapter 4: the experimental results of the proposed converter, considering the parameters and details of the small-scale single-phase prototype. It is presented the converter behavior under steady-state operation and dynamic operation.
- Chapter 5: the conclusion of the thesis. The future works from the PhD study is presented as well, followed by the scientific production achieved during the PhD period.

2 PROPOSED TOPOLOGY

The proposed three-phase AC-DC IMMC is described in this section. The structure and the principle of operation describe the basis for the modeling, which is focused on obtaining the main equations that describe the influence of the submodules voltages across the input and transformer terminals, and the bus voltage. From that, the modulation techniques in both sides are developed in order to operate the aforementioned voltages following some restrictions. The capacitors voltage balancing and the circulating currents minimization are coordinated to be handled in a single algorithm. The control scheme is elaborated according to the converter plants, in each side, regulating the input current, the bus voltage and the output voltage while controlling the power flow between the AC and DC grids.

2.1 Structure

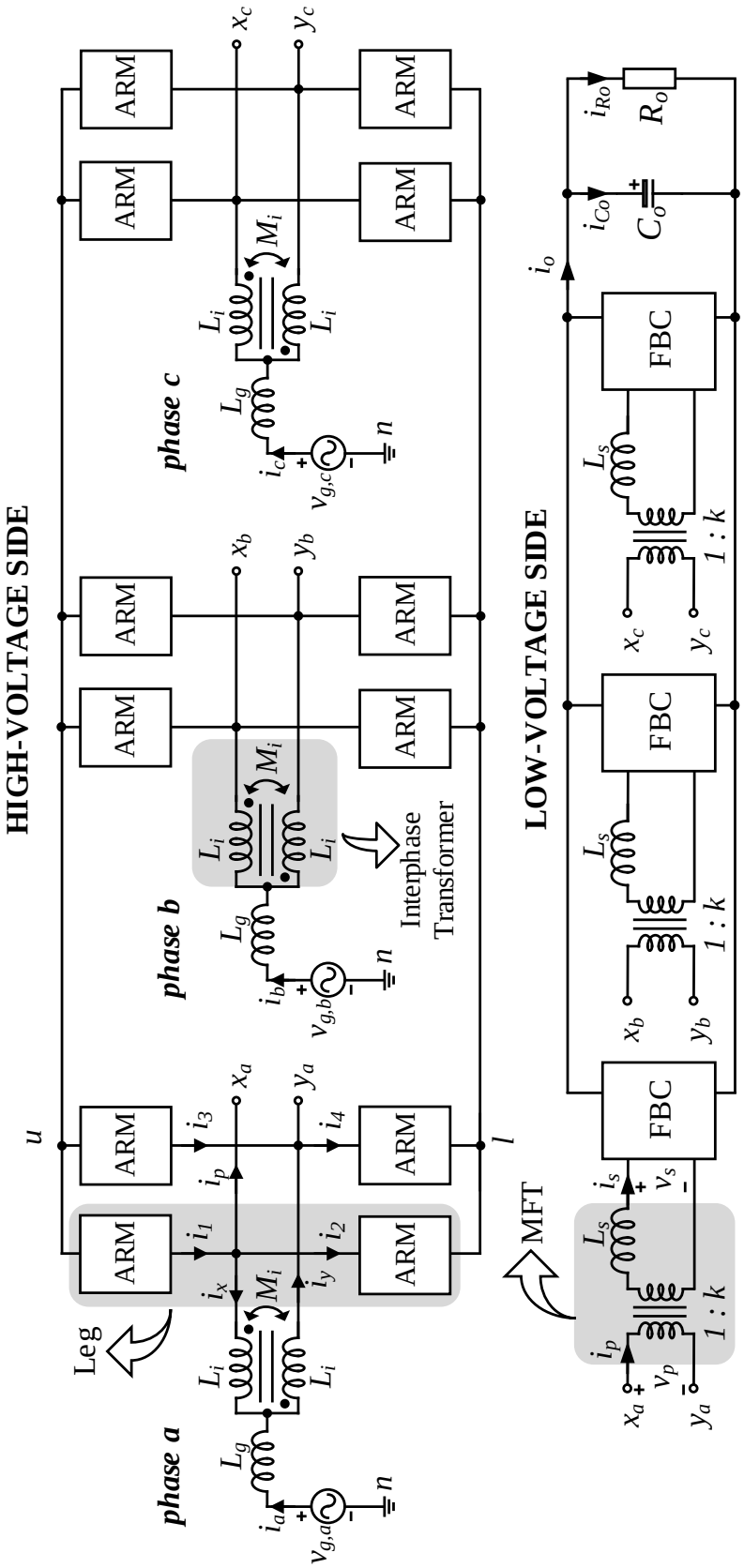
The structure of a three-phase AC-DC IMMC with medium frequency transformer is shown in Figure 2.1. The converter has three identical and independent phases (*a*, *b*, *c*), each one divided into high-voltage side (HVS) and low-voltage side (LVS).

At the HVS, one phase is made of one input inductor, one interphase transformer and two legs (X and Y). The three phases are connected to each other at the positive and negative DC bars referred as *u* and *l*, respectively. Each phase is connected to the medium-voltage AC grid through the input inductor L_g. The input current is shared between the two legs through an interphase transformer, with turn ratio 1:1, self-inductance L_i and mutual inductance M_i. The interleaving inductors help to decrease the semiconductors efforts, and thus, their conduction losses (BASCOPÉ; BARBI, 2000).

Each converter leg is made of two arms. One converter arm is composed of N half-bridge submodules (HBSM) connected in series with an arm inductor (L), as shown in Figure 2.2. The arm inductors have the task of limiting the currents through the submodules due to the instantaneous voltage difference between the arms. Each HBSM is composed of two switches (S and $\bar{S}$) with antiparallel diodes operating in a complementary way, and one capacitor (C).

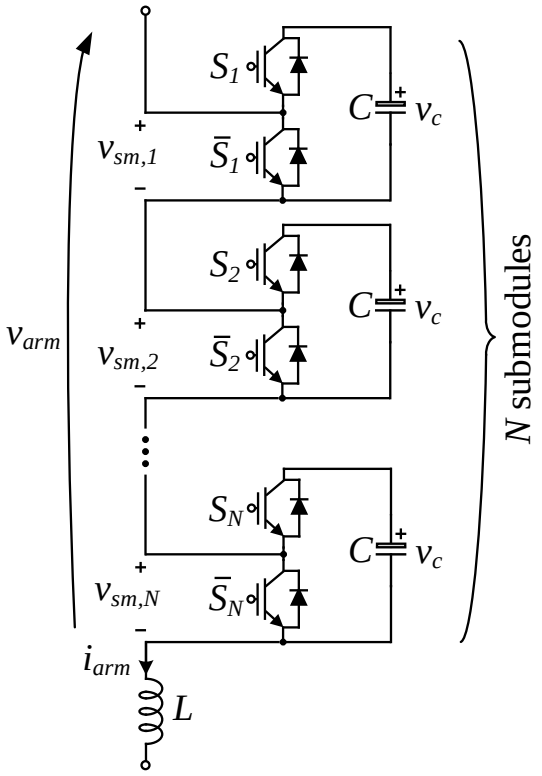
Thanks to the similarity with the MMC topology, this structure allows the same features, such as, modular construction, low total harmonic distortion (THD) of voltages and currents, large number of voltage levels and redundant submodules in each arm to achieve a fault-tolerant operation (DU *et al.*, 2018).

Figure 2.1 – Structure of a three-phase AC-DC interleaved modular multilevel converter with medium frequency transformer.



Source: author's right.

Figure 2.2 – Structure of a converter arm.

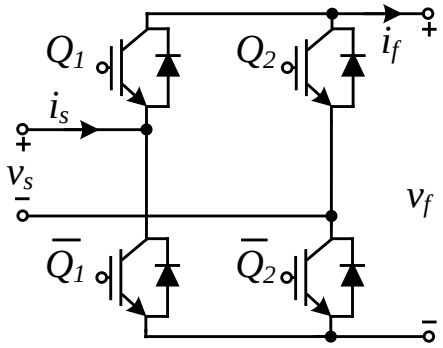


Source: author's right.

The connection of the HVS to the LVS is made by a medium-frequency transformer (MFT) in each phase, where k is the transformer turns ratio and L_s is the transformer leakage inductance reflected to secondary side.

The MFT primary side is connected to the mid-points of each converter leg (x_a, y_a, x_b, y_b, x_c, y_c), while its secondary side is connected to a full-bridge converter (FBC). The transformer offers the galvanic isolation. The medium-frequency operation allows a volume and weight reduction when compared to conventional low-frequency transformers.

Figure 2.3 – Structure of a full-bridge converter.



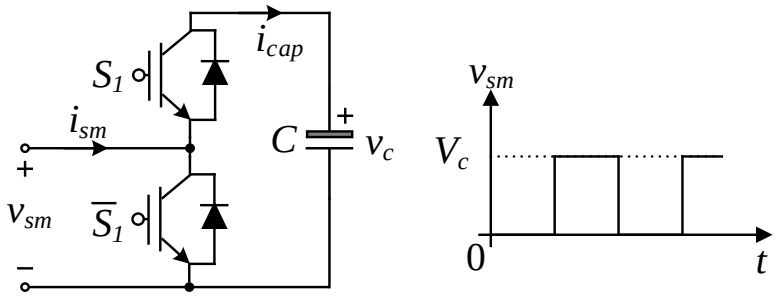
Source: author's right.

At the LVS, each FBC is composed of four switches (Q_1, $\overline{Q_1}$, Q_2 and $\overline{Q_2}$) with antiparallel diodes, operating in a complementary way (Figure 2.3). The three FBCs are connected to a single output capacitor (C_o) and the load (R_o).

2.2 Principle of operation

At the HVS, the HBSM produce the arm voltages. As illustrated in Figure 2.4, according to the top switch state *S*, the submodule output waveform v_{sm} is capable to achieve two voltage levels, "0" and "v_c". Depending on the submodule input current direction i_{sm}, the capacitor voltage v_c can either increase, decrease or not change. The possible switching states of the HBSM are described in Table 2.1.

Figure 2.4 – Half-bridge submodule and output voltage waveform.



(a) (b)

Source: author's right.

Table 2.1 – Switching states of HBSM.

State	S_1	v_{sm}	$i_{sm} > 0$	$i_{sm} \leq 0$
I	0	0	$v_c \approx$	$v_c \approx$
II	1	v_c	$v_c \uparrow$	$v_c \downarrow$

$\approx$ = no change, $\uparrow$ = increase, $\downarrow$ = decrease

Source: author's right.

Therefore, each HBSM output voltage v_{sm} can be represented in terms of the capacitor voltage and the switching state of top switch S_1 as the equation (2.1).

$$v_{sm}(t) = S_1(t) \cdot v_c(t) \tag{2.1}$$

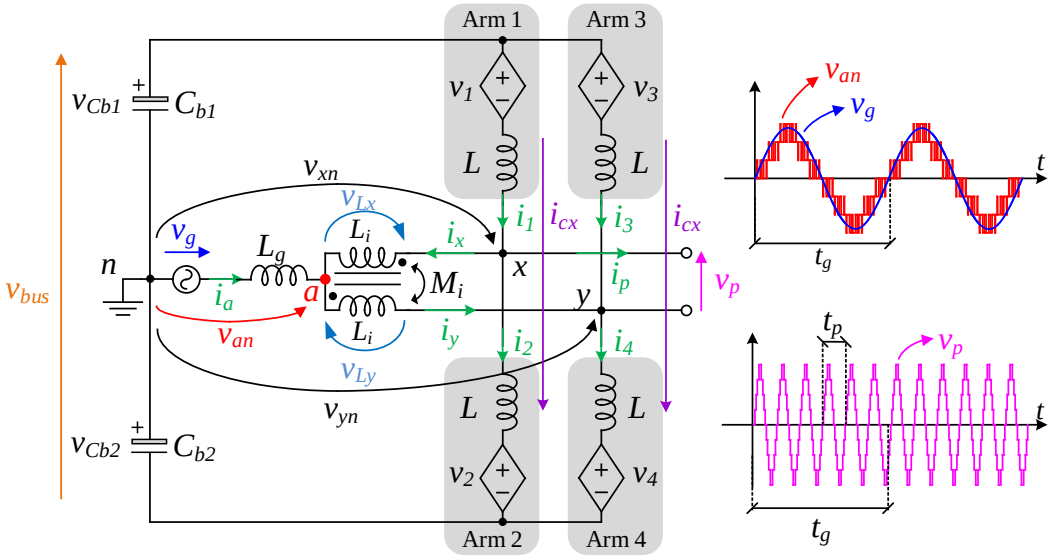
The equation (2.1) can be expanded to obtain the voltage across the arm in terms of the capacitors average voltage V_c and the number of active submodules δ, as represented in equation (2.2).

$$v_{arm}(t) = \delta(t) \cdot V_c \tag{2.2}$$

From equation (2.2), each arm can be represented by a controlled voltage source and, therefore, one phase is described as the equivalent circuit shown in Figure 2.5 (a).

One important specificity of this converter is that the HVS modulation sets the number of active submodules per arm to generate simultaneously, the low frequency input voltage v_{an} and MFT medium frequency primary voltage v_p. The idealized waveforms of v_{an}, v_g and v_p are presented in Figure 2.5 (b). t_g and t_p are the periods of the v_g and v_p, respectively.

Figure 2.5 – HVS principle of operation: (a) 1-phase equivalent circuit and (b) idealized waveforms of the grid voltage v_g, input voltage v_{an} and MFT primary voltage v_p.



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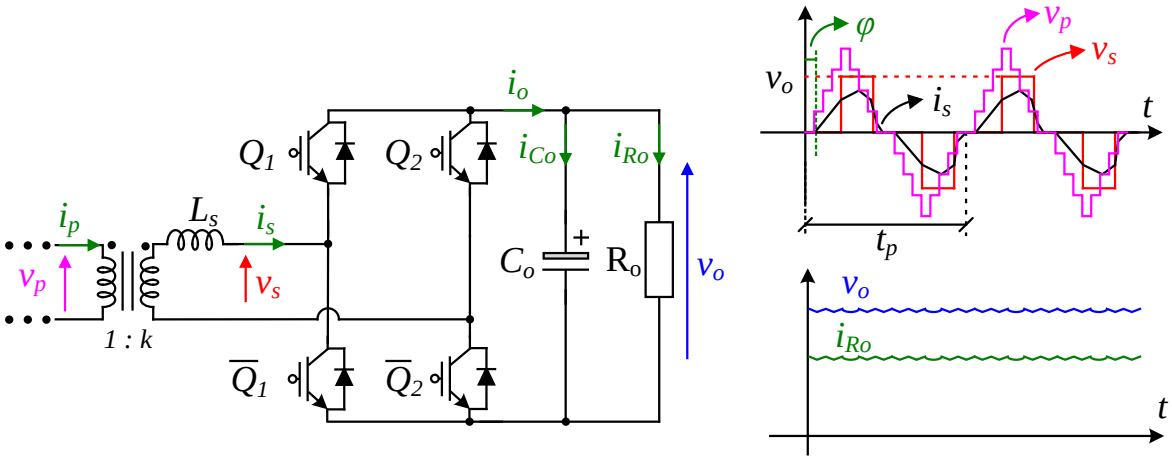
At the LVS, the operation of the FBC is shown in Figure 2.6 (a). Assuming that a large output capacitor C_o is used, the voltage of the MFT secondary v_s is related to the output average voltage V_o and to the switching states of the top switches Q_1 and Q_2 by

$$v_s(t) = V_o \cdot (Q_1(t) - Q_2(t)) \tag{2.3}$$

The power transferred to the load R_o depends on the phase-shift angle φ between the MFT primary and secondary voltages v_p and v_s. Therefore, the LVS controller regulates the output voltage v_o by setting the phase-shift angle φ, while the LVS modulation send the gate signals to switches Q_1 and Q_2. The idealized waveforms of the MFT voltages v_p and v_s, the MFT secondary current i_s, the output voltage v_o and the output current i_o are presented in Figure 2.6 (b).

Figure 2.6 – LVS principle of operation: (a) 1-phase equivalent circuit and (b) idealized waveforms of MFT voltages v_p and v_s, the MFT secondary current i_s, output voltage v_o and output load current i_{Ro}.



(a) (b)

Source: author's right.

2.3 HVS Modeling

The main objective of the modeling is to obtain the equivalent circuits that represent the converter on its high-voltage side. Three variables are required: input voltage v_{an}, transformer primary voltage v_p and bus voltage v_{bus}. The following sections describe the modeling procedure in detail.

In summary, from the number of active submodules on each arm δ_1, δ_2, δ_3 and δ_4 in each phase, it is possible to obtain the switching states a_x and a_y. The combination of the average voltage on the submodules capacitors V_c and the switching states a_x and a_y provides the virtual voltages v_e and v_t, which are equivalent voltages produced by the submodules. The virtual voltages v_e and v_t do not exist physically, but they are respectively related to the input voltage v_{an}, the transformer primary voltage v_p, which can be measured.

In the same way, from the number of active submodules on each arm δ_1, δ_2, δ_3 and δ_4, the number of active submodules on each leg n_x and n_y are calculated. Thus, together with the circulating currents on each leg i_{cx} and i_{cy}, the bus voltage v_{bus} is obtained.

2.3.1 Leg mid-point voltages v_{xn} and v_{yn}

At the HVS, considering phase *a* and assuming that the submodules capacitors are regulated at V_c, the converter arm voltages are described by

$$\begin{cases} v_1(t) = \delta_1(t) \cdot V_c \\ v_2(t) = \delta_2(t) \cdot V_c \\ v_3(t) = \delta_3(t) \cdot V_c \\ v_4(t) = \delta_4(t) \cdot V_c \end{cases} \tag{2.4}$$

where, δ_1, δ_2, δ_3 and δ_4 are the number of active submodules in the respective arms 1, 2, 3 and 4. Defining the switching states a_x and a_y as

$$\begin{cases} a_x(t) \triangleq \delta_2(t) - \delta_1(t) \\ a_y(t) \triangleq \delta_4(t) - \delta_3(t) \end{cases} \tag{2.5}$$

Assuming that the upper arms voltages are equal to the lower arms voltages (Figure 2.5), *i.e.*,

$$v_{Cb1}(t) = v_{Cb2}(t) \tag{2.6}$$

Using the Kirchhoff´s laws in circuit of the Figure 2.5 (a), considering (2.4), (2.5) and (2.6), the pole voltages are obtained

$$\begin{cases} v_{xn}(t) = \dfrac{1}{2}\left(V_c\, a_x(t) + L\left(\dfrac{di_2(t)}{dt} - \dfrac{di_1(t)}{dt}\right)\right) \\ v_{yn}(t) = \dfrac{1}{2}\left(V_c\, a_y(t) + L\left(\dfrac{di_4(t)}{dt} - \dfrac{di_3(t)}{dt}\right)\right) \end{cases} \tag{2.7}$$

2.3.2 Input voltage v_{an} and MFT primary voltage v_p

Using Kirchhoff´s laws, the input voltage v_{an} is

$$v_{an}(t) = \frac{1}{2}\left(v_{xn}(t) + v_{yn}(t) - v_{Lx}(t) + v_{Ly}(t)\right) \tag{2.8}$$

where v_{Lx} and v_{Ly} are the voltage across the interphase transformer windings, given as

$$\begin{cases} v_{Lx}(t) = L_i \dfrac{di_x(t)}{dt} + M_i \dfrac{di_y(t)}{dt} \\ v_{Ly}(t) = L_i \dfrac{di_y(t)}{dt} + M_i \dfrac{di_x(t)}{dt} \end{cases} \tag{2.9}$$

The transformer primary voltage v_p is

$$v_p(t) = v_{xn}(t) - v_{yn}(t) \tag{2.10}$$

Also, from Figure 2.5 (a), the input current i_a and the interphase transformer currents i_x and i_y are given as in (2.11).

$$\begin{cases} i_a(t) = i_y(t) - i_x(t) \\ i_x(t) = i_1(t) - i_2(t) - i_p(t) \\ i_y(t) = i_4(t) + i_3(t) - i_p(t) \end{cases} \tag{2.11}$$

From (2.11), the relationship between the HVS currents are given by (2.12).

$$\begin{cases} i_a(t) = i_y(t) - i_x(t) \\ i_a(t) = i_2(t) - i_1(t) + i_4(t) - i_3(t) \\ i_p(t) + i_m(t) = \dfrac{1}{2}\left(i_1(t) - i_2(t) - i_3(t) + i_4(t)\right) \end{cases} \tag{2.12}$$

where, i_m is the differential current of interphase transformer, calculated by

$$i_m(t) \triangleq \frac{1}{2}\left(i_x(t) + i_y(t)\right) \tag{2.13}$$

Observe that the interphase transformer has a 1:1 turn ratio. Thus, the fundamental of currents i_x and i_y have the same amplitudes $I_{a\_p}/2$, where I_{a_p} is the input current amplitude, and are phase-shifted by 180º from each other. Assuming that the harmonics of currents i_x and i_y are small, the differential current i_m can be neglected. Then (2.12) can be rewritten as in (2.14).

$$\begin{cases} i_a(t) = i_y(t) - i_x(t) \\ i_a(t) = i_2(t) - i_1(t) + i_4(t) - i_3(t) \\ i_p(t) = \frac{1}{2}\left(i_1(t) - i_2(t) - i_3(t) + i_4(t)\right) \end{cases} \tag{2.14}$$

Defining the equivalent inductance L_e,

$$L_e \triangleq \frac{L_i - M_i}{2} + \frac{L}{4} \tag{2.15}$$

Defining the virtual voltages v_e and v_t, which are generated by the submodules switching states, given in (2.16) and (2.17), respectively,

$$v_e(t) \triangleq \frac{V_c}{4}\left(a_x(t) + a_y(t)\right) \tag{2.16}$$

$$v_t(t) \triangleq \frac{V_c}{2}\left(a_x(t) - a_y(t)\right) \tag{2.17}$$

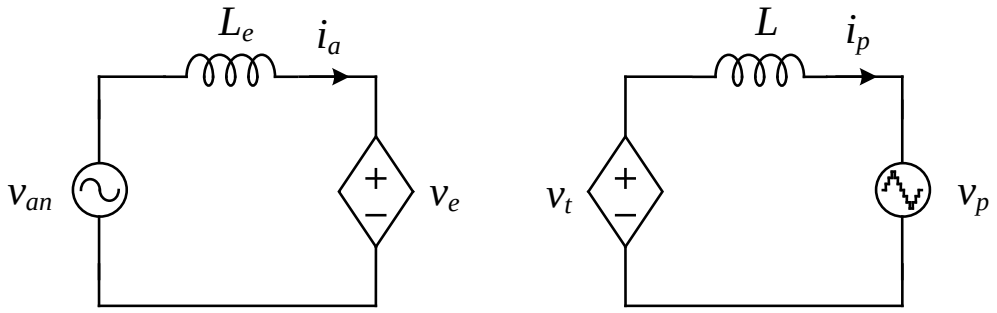
Substituting (2.7), (2.9), (2.14), (2.15), (2.16) and (2.17) in (2.8) and (2.10), it´s possible to obtain a decoupled equivalent model for the low-frequency side and the MFT primary voltage v_p, described by

$$v_{an}(t) = v_e(t) + L_e\frac{di_a(t)}{dt} \tag{2.18}$$

$$v_p(t) = v_t(t) - L\frac{di_p(t)}{dt} \tag{2.19}$$

From (2.18) and (2.19), it´s possible to obtain the equivalent circuits of Figure 2.7. It is observed that the virtual voltages v_e and v_t, resulting from the submodule states (a_x, a_y) directly related to the voltages v_{an} and v_p. Thus, it is possible to control these voltages through the modulation technique.

Figure 2.7 – HVS decoupled equivalent circuits: (a) low-frequency grid side circuit and (b) MFT primary side circuit.



(a) (b)

Source: author's right.

2.3.3 Bus voltage v_{bus}

Naming n_x and n_y the number of active submodules in each converter leg, then

$$\begin{cases} n_x(t) \triangleq \delta_1(t) + \delta_2(t) \\ n_y(t) \triangleq \delta_3(t) + \delta_4(t) \end{cases} \tag{2.20}$$

In the same way, using the Kirchhoff´s laws in the circuit of Figure 2.5 (a), the bus voltage v_{bus} is described as

$$v_{bus}(t) = \frac{V_c}{2}\Big(n_x(t) + n_y(t)\Big) + \frac{L}{2}\Big(\frac{di_1}{dt} + \frac{di_2}{dt} + \frac{di_3}{dt} + \frac{di_4}{dt}\Big) \tag{2.21}$$

By default, the circulating currents are due to existing unbalanced voltages among the voltages across the DC link and submodules capacitors (LI *et al.*, 2015). Since there are two

legs per phase in the proposed converter, each one has a circulating current component i_{cx} and i_{cy}, which can be calculated as

$$\begin{cases} i_{cx}(t) \triangleq \dfrac{1}{2}(i_1(t) + i_2(t)) \\ i_{cy}(t) \triangleq \dfrac{1}{2}(i_3(t) + i_4(t)) \end{cases} \tag{2.22}$$

Therefore, substituting (2.22) in (2.21)

$$v_{bus}(t) = \frac{V_c}{2}\Big(n_x(t) + n_y(t)\Big) + \frac{L}{2}\left(\frac{di_{cx}}{dt} + \frac{di_{cy}}{dt}\right) \tag{2.23}$$

This equation is used to develop the circulating current minimization algorithm.

2.4 HVS modulation technique

A HVS modulation must be developed to obtain the desired virtual voltages (v_e and v_t), which are respectively related to the input voltage v_{an} and MFT primary voltage v_p, in each phase.

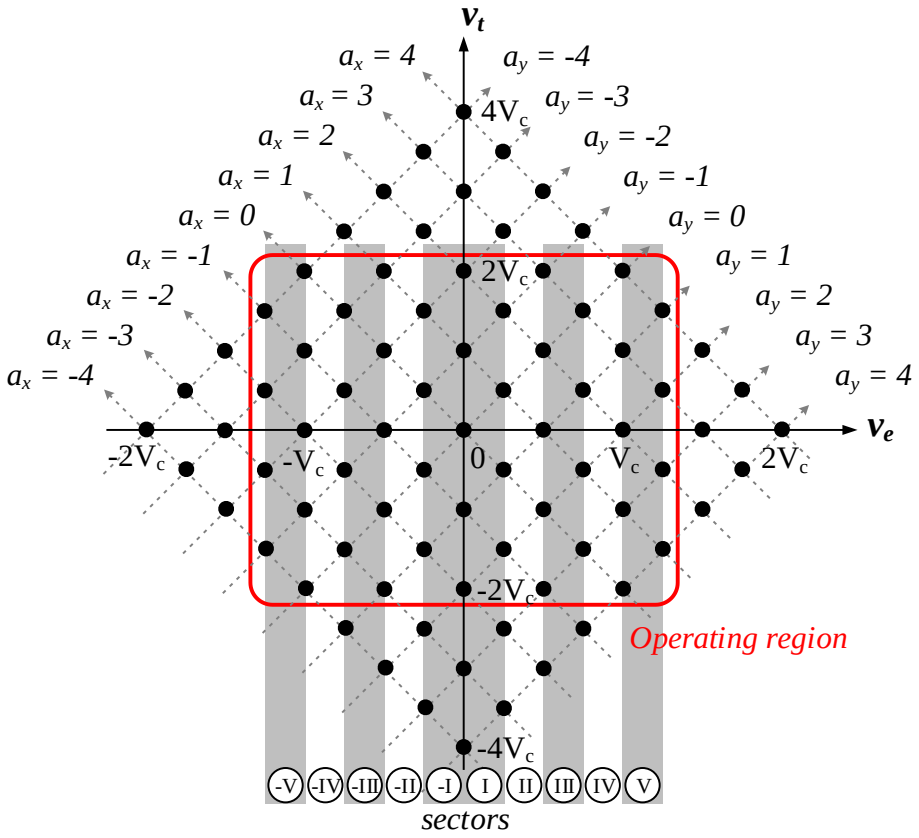
Among the possible techniques (DEBNATH *et al.*, 2015) (KONSTANTINOU; CIOBOTARU; AGELIDIS, 2013) (PICAS *et al.*, 2015) (DENG *et al.*, 2016), the adopted modulation technique is based on the space vector modulation. According to the number of submodules N present in each arm, the implementation begins by listing all the possible switching states in terms of the v_e and v_t voltages. This is possible since v_e and v_t are directly related to the submodules switching states by equations (2.16) and (2.17). Assuming 4 submodules per arm, the resulting space-state diagram is shown in Figure 2.8. The switching states are divided into sectors. One sector corresponds to a given level of v_e. Thus, the operation of the vector sequence follows the same pattern for all sectors.

The modulation indices M_e and M_t describe by how much the state-space diagram is modulated in each axis (v_e and v_t). They can be respectively calculated as:

$$\begin{cases} M_e = \dfrac{2\,V_{e\_p}}{N\,V_c} \\ M_t = \dfrac{V_{t\_p}}{N\,V_c} \end{cases} \tag{2.24}$$

where, V_{e_p} and V_{t_p} are the selected peak states of the voltages v_e and v_t, respectively.

Figure 2.8 – HVS modulation technique: space-state diagram.



Source: author's right.

For instance, the adopted operating region in Figure 2.8 results in

$$\begin{cases} M_e = \dfrac{2\,V_{e\_p}}{N\,V_c} = \dfrac{2\left(\frac{5}{4}V_c\right)}{4\,V_c} = 0.625 \\ M_t = \dfrac{V_{t\_p}}{N\,V_c} = \dfrac{2\,V_c}{4\,V_c} = 0.5 \end{cases} \tag{2.25}$$

From (2.24), the relation between both modulation indices is calculated by

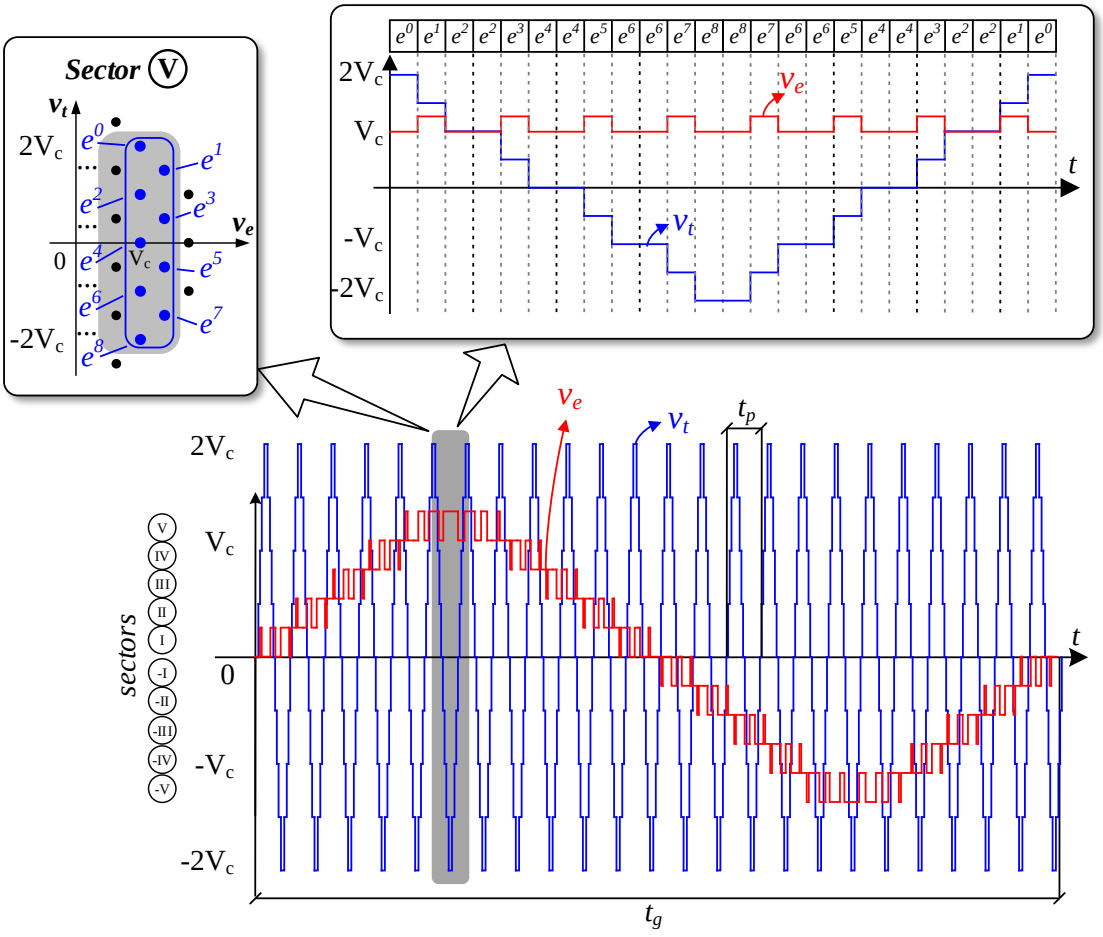
$$M_e = \frac{2N+1}{2N} - M_t \tag{2.26}$$

Among all the possible states, only a reduced number of states is chosen and constitutes an “operating region”. The choice of this region follows some restrictions:

- The MFT primary voltage v_p must have the same operation frequency in entire region, *i.e.*, the same number of states for any sector of v_e (rectangular region);
- Modulation indices M_e and M_t are limited by the chosen region and they must be compatible with the grid voltage levels and the number of submodules in each arm;
- The number of levels in the v_e and v_t voltages must be compatible with the desired THD.

Taking as an example in red color region of Figure 2.8, the vector sequence of one sector and the waveforms of the voltages v_e and v_t is illustrated in Figure 2.9.

Figure 2.9 – HVS modulation technique: vector sequence of one sector and the waveforms of the voltages v_e and v_t.



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2.5 LVS modulation technique

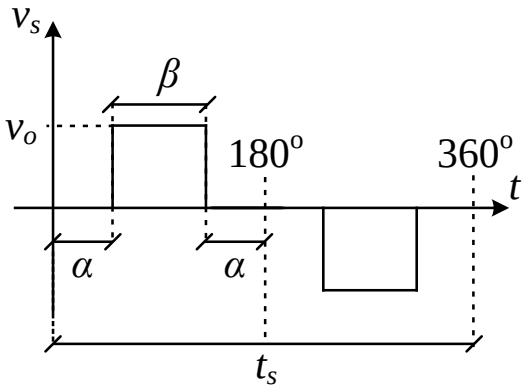
At the LVS, the choice of the modulation technique took into account that the full-bridge converter provides the maximum of three voltage levels in the MFT secondary voltage. Thus, the SHE-PWM (Selective Harmonic Elimination Pulse-Width Modulation) was chosen to suppress the third order harmonic component (and its multiples), due to it being the one with the smaller order, which enables the reduction of MFT voltage and current stresses (SANCHEZ-RUIZ *et al.*, 2017).

According to the SHE-PWM equations and choosing the third harmonic (h_e = 3) to be eliminated, the interval β is given by

$$\beta = \frac{2\pi}{h_e} = \frac{2\pi}{3}\ rad = 120^o \tag{2.27}$$

Therefore, the expected MFT secondary voltage v_s waveform is illustrated in Figure 2.10.

Figure 2.10 – LVS modulation technique: MFT secondary voltage waveform v_s.



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2.6 Capacitors voltage balancing and circulating currents minimization algorithm

As for any modular multilevel converter, the submodules capacitor voltage balancing is mandatory for its functional operation (GHETTI *et al.*, 2017). From (2.23), it is observed that the circulating currents derivatives changes according to n_x, n_y and v_{bus}. If v_{bus} is kept regulated by the control system, by setting the number of active submodules in each leg n_x and n_y, it is possible to change the direction of the circulating current in order to minimize it.

For that, since the average bus voltage v_{bus} is nearly equal to NV_c, the following equations must be respected

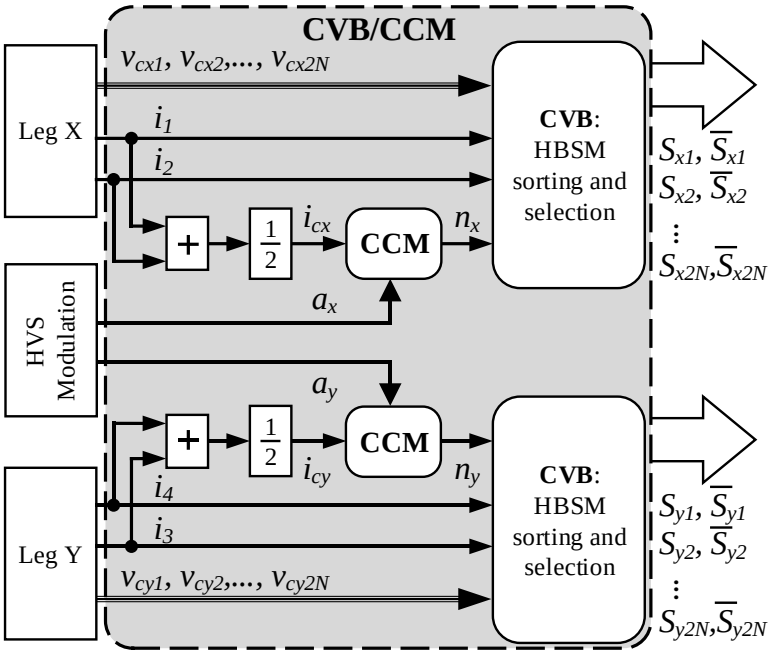
$$\begin{cases} \dfrac{di_{cx}(t)}{dt} = \dfrac{V_c}{2L}\big(N - n_x(t)\big) \\ \dfrac{di_{cy}(t)}{dt} = \dfrac{V_c}{2L}\Big(N - n_y(t)\Big) \end{cases} \tag{2.28}$$

Therefore, according to the circulating currents flow (i_{cx} and i_{cy}), there are two possible situations:

- If the circulating current is increasing, the number of active submodules in each leg (n_x and n_y) must be higher than N;
- If the circulating current is falling, the number of active submodules in each leg (n_x and n_y) must be lower than N.

From that, the capacitors voltage balancing (CVB) and the circulating currents minimization (CCM) can be combined together in a single algorithm (CVB/CCM), as illustrated in Figure 2.11. This is one important specificity of this converter. The algorithm is used in each leg and the steps are described as follows:

Figure 2.11 – CVB/CCM algorithm in each phase.



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i. The voltages of 2*N* submodules capacitors in each leg are measured and compared with each other;
ii. The arm currents (i_1, i_2, i_3 and i_4) are measured and the circulating currents are calculated using (2.22);
iii. The modulation technique block sends the switching states (a_x and a_y) to the CCM block;
iv. From the circulating currents flow and the modulation technique state variables, the number of active submodules in each leg (n_x and n_y) are calculated in CCM block and sent to the CVB block;
v. In CVB block, according to the arm currents flows and the capacitors voltages, is verified:
    - If the arm current is higher than zero, the arm is absorbing energy, therefore, the submodules with lower voltage across the capacitors are chosen and activated;
    - If the arm current is lower than zero, the arm is supplying energy, therefore, the submodules with higher voltage across the capacitors are chosen and activated.

2.7 Control scheme

2.7.1 HVS plant

Concerning the HVS plant, two transfer functions are obtained using the one-phase equivalent circuit from Figure 2.5.

Applying Laplace's transform to (2.17), the single-phase plant transfer function G_1 is obtained and represents the behavior of the input current by the equivalent inductor voltage given in (2.29).

$$G_1(s) = \frac{i_a(s)}{v_{an}(t) - v_e(t)} = \frac{1}{s\,L_e} \tag{2.29}$$

For the three-phase topology, (2.29) is expanded in dq-axis rotating reference frame (see Appendix A) (BAHRANI *et al.*, 2011), which results in

$$\begin{cases} v_{e,d} = v_d(t) - L_e \dfrac{di_d(t)}{dt} + \omega\, L_e\, i_q(t) \\ v_{e,q} = -L_e \dfrac{di_q(t)}{dt} - \omega\, L_e\, i_d(t) \end{cases} \tag{2.30}$$

Where $v_{e,d}$ and $v_{e,q}$ are, respectively, the direct axis and the quadrature axis of the virtual voltage v_e, v_d is the grid voltage direct axis, ω is the grid angular frequency, i_d and i_q are, respectively, the direct axis and the quadrature axis of the input current.

The bus voltage plant transfer function G_2 consider that the input power p_{in} and output power p_{out} are nearly equal: $p_{in} \cong p_{out}$. In Figure 2.5 is observed that the AC grid supplies the arm submodules, which in its turn supplies the low-voltage side through the MFT. Thus,

$$p_{in} \cong p_{arm1} + p_{arm2} + p_{arm3} + p_{arm4} \cong 4\, p_{arm} \cong p_{out} \tag{2.31}$$

Therefore,

$$\begin{cases} p_{in}(t) = v_g(t)\, i_a(t) \\ p_{out}(t) = 4\, v_{arm}(t)\, i_{arm}(t) \end{cases} \tag{2.32}$$

Since each arm is turned-on in every half-period of the grid voltage, *i.e.*, $T = t_g/2$, and assuming that capacitors voltages are balanced, the average voltage V_{arm} across the arms in steady-state is calculated by

$$V_{arm} = \frac{1}{T}\int_0^T N\, v_c\, dt = \frac{1}{t_g}\int_0^{\frac{t_g}{2}} N\, v_c\, dt = \frac{N\, V_c}{2} \tag{2.33}$$

Assuming that the capacitors voltages are balanced, n_x and n_y are "balanced" and kept around N. Thus, from (2.23), the bus voltage is equal to

$$v_{bus}(t) \cong \frac{v_c(t)}{2}\left(n_x + n_y\right) = \frac{v_c(t)}{2}(N + N) = N\, v_c(t) \tag{2.34}$$

From Figure 2.2, (2.1) and (2.34), the arms currents given by

$$i_{arm}(t) \cong i_{cap}(t) = C\frac{dv_c(t)}{dt} = \frac{C}{N}\frac{dv_{bus}(t)}{dt} \tag{2.35}$$

Substituting (2.33) and (2.35) in (2.32)

$$\begin{cases} p_{in}(t) = v_g(t)\, i_a(t) \\ p_{out}(t) = 2\, C\, V_c\, \dfrac{dv_{bus}(t)}{dt} \end{cases} \tag{2.36}$$

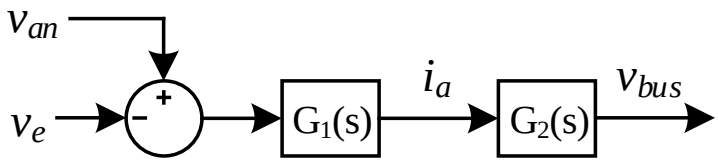
Applying the Laplace's transform to (2.36), it returns the plant transfer function G_2, which represents the behavior of the bus voltage by the input current

$$G_2(s) = \frac{v_{bus}(s)}{i_a(s)} = \frac{V_g}{s\ 2\ V_c\ C} \tag{2.37}$$

where, V_g is the grid RMS voltage.

From what precedes, the HVS can be modeled as cascaded plants (G_1 and G_2), as shown in Figure 2.12.

Figure 2.12 – HVS plant of the single-phase AC-DC IMMC.



Source: author's right.

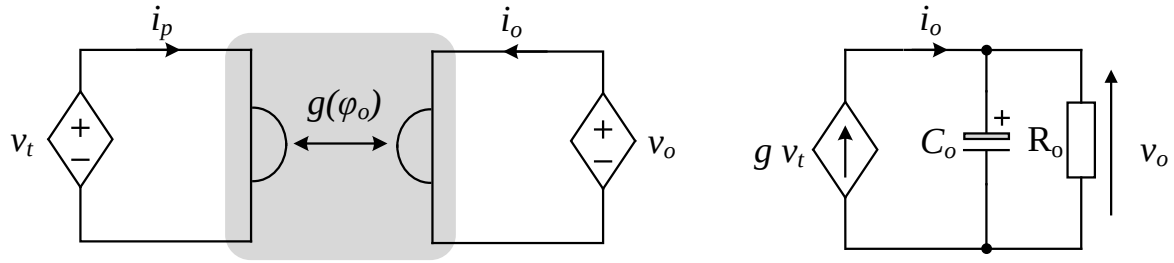
2.7.2 LVS plant

The LVS plant is obtained using the gyrator theory (TELLEGEN, 1948), which circuit model is described in Figure 2.13 (a), and then considering the FBC equivalent circuit, as illustrated in Figure 2.13 (b) (SANTOS *et al.*, 2011) (OLIVEIRA FILHO, 2015).

The gyrator conductance g is the gain, given in (2.38), representing the relationship between the output current (i_o) and the phase-shift angle φ for a linearized boundary condition of the LVS in steady-state situation.

$$g(\varphi_o) = \frac{\partial I_o}{\partial \varphi_o} = \frac{V_o}{k\ 2\pi\ f_t\ L_t} cos\varphi_o \tag{2.38}$$

Figure 2.13 – LVS plant transfer function: (a) gyrator model, (b) FBC equivalent circuit.



(a) (b)

Source: adapted from (SANTOS, 2011).

where f_t is the transformer frequency and L_t is equivalent inductance determined by

$$L_t = \frac{L}{k^2} + L_s \tag{2.39}$$

With this gyrator gain, the power flow between the primary and secondary sides is regulated by the phase-shift angle φ between the MFT primary voltage v_p and the secondary voltage v_s. Therefore, if the phase-shift angle φ increases, the transferred power increases, otherwise, it decreases. This angle can be either positive (rectifier mode) or negative (inverter mode).

From Figure 2.13 (b), the FBC transfer function G_{ivo} represents the behavior of the output voltage v_o and the output current i_o, given by

$$G_{vio}(s) = \frac{v_o(s)}{i_o(s)} = \frac{R_o}{s\ R_o\ C_o + 1} \tag{2.40}$$

Thus, the plant transfer function G_3 is the combination of the gyrator gain g and the transfer function G_{ivo} and represents the behavior of the output voltage v_o by the phase-shift angle φ_o, given by

$$G_3(s) = \frac{v_o(s)}{\varphi_o(s)} = \frac{g\ R_o}{s\ R_o\ C_o + 1} \tag{2.41}$$

2.7.3 HVS and LVS control scheme

The control schemes for the AC-DC IMMC three-phase and the single-phase topologies are shown in Figure 2.14 and Figure 2.15, respectively. In both control schemes, at the HVS, the controller monitors the input current and bus voltage. At the LVS, the output DC voltage is regulated using the gyrator theory. Both HVS and LVS controllers are independent.

The three-phase controller is applied in a medium-voltage high-power application, which is analyzed through simulation in Chapter 3. The single-phase controller was experimentally validated in Chapter 4.

The K factor method (VENABLE, 1983) was used in all controllers' design, following the constraints in Table 2.2. Even with the second order double zero pole cascaded plant (section 2.7), the controllers tuning was possible to realize due to the high capacitance value on the G_2, which makes it slow. Therefore, PI controllers could fulfill the application.

Figure 2.14 – Control scheme of the three-phase AC-DC IMMC.

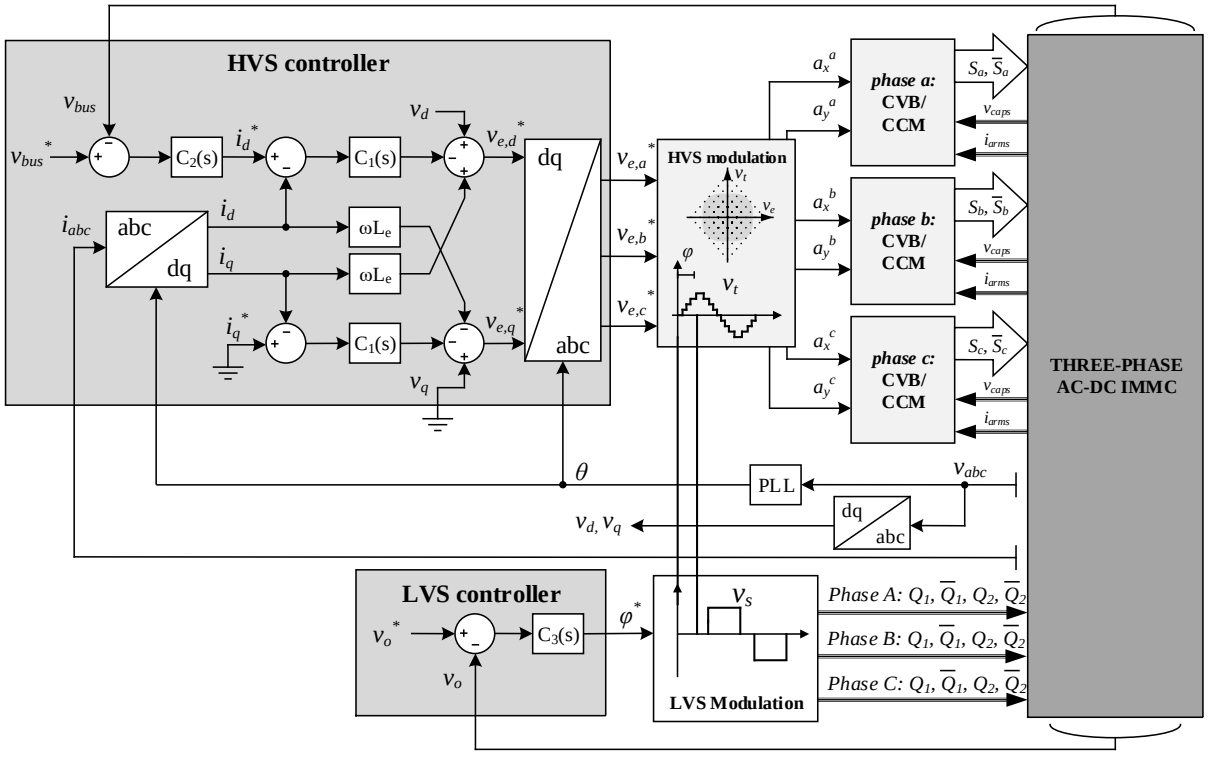


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Figure 2.15 – Control scheme of the single-phase AC-DC IMMC.

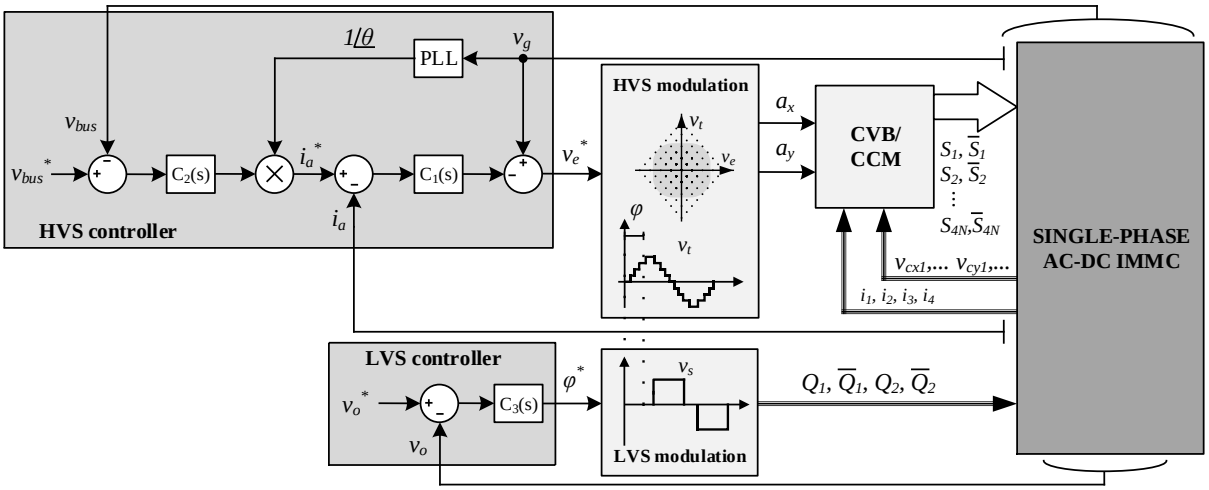

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Table 2.2 – Constraints of the controllers' design using K factor method.

Controller / Constraint	Input current C_1	Bus voltage C_2	Output voltage C_3
Crossing frequency	10 kHz	12 Hz	1.25 kHz
Phase margin	60º	90º	60º
Controller type	2	2	2

Source: author's right.

Following the HVS side cascaded transfer functions, both the single-phase and three-phase topologies control structures are cascaded and composed of inner and the outer loops with their respective controllers (C_1 and C_2). The voltages v_{an} and v_g (single-phase control scheme) and the voltages v_d, v_q (three-phase control scheme) are obtained from PLL (phase-locked loop) signals of from the AC grid.

The outer loop keeps the bus voltage (v_{bus}) as constant as possible, following its reference (v_{bus}*), and its output becomes the reference (i_a* for the single-phase control scheme, and (i_d*, i_q*) for the three-phase control scheme) for the inner loop. The inner loop measures and regulates the input currents (i_a for the single-phase control scheme, and (i_d, i_q) for the three-phase control scheme) according to their references (i_a*, i_d*, i_q*) in order to allow the submodule capacitors to be charged.

In single-phase control scheme, the modulating signal v_e* are directly applied to the HVS modulation technique block. In the three-phase control scheme, it is necessary to employ

the inverse Park transform (dq – abc) to provide the modulating signals $v_{e,a}$*, $v_{e,b}$*, $v_{e,c}$* and apply them to the HVS modulation block.

Therefore, the HVS modulation block sends the switching states (a_x and a_y) to the CVB/CCM block in order to sort, to select and to drive the HBSMs.

At the LVS, the control structure is the same for both single-phase and three-phase topologies, which are composed of one loop with a controller (C_3). The phase-shift angle φ is calculated by the output voltage controller C_3, in order to regulate the output voltage v_o to follow to its reference v_o*, and sent to the LVS modulation block, which generates the FBC drive signals.

2.8 Final comments

This chapter presented the study of the proposed an AC-DC interleaved modular multilevel converter with medium-frequency transformer. The theoretical analysis consisted on the converter structure, principle of operation and modeling. From that, the high-voltage side equivalent circuits described the how the simultaneous generation of the low-frequency grid voltage and the medium-frequency transformer primary voltage can be achieved. Further, this feature was used in the proposed modulation technique.

The capacitors voltage balancing and the circulating currents minimization are combined together in a single algorithm. This is another important characteristic, which simplifies the hardware implementation.

The transfer functions of the converter plants allowed to regulate the AC current and the DC bus voltage, on the high-voltage side, and the DC voltage and power flow, on the low-voltage side. Thus, the control system can be employed by using proportional-integral controllers and requiring less hardware resources.

3 CONVERTER ANALYSIS, DESIGN AND SIMULATION

Based on the converter study and the modulation analysis, some analyses are developed here in order to obtain the optimum number of submodules per arm N_{opt}, the optimum transformer ratio k_{opt}, to evaluate the virtual voltage v_t behavior, concerning its RMS value and total harmonic distortion, and to understand the converter losses under full-load and no-load conditions. Also, the AC-DC IMMC design is described and tested through simulation for a 100 kVA three-phase converter applied as an AC-DC stage of a DC power distribution system. The steady-state and the power flow inversion conditions are simulated.

3.1 Converter analysis

3.1.1 Optimum number of submodules per arm N_{opt}

As described in chapter 2, section 2.4, the modulation technique was developed in order to obtain the desired submodules voltages (v_e and v_t), which are respectively related to the input voltage and the MFT primary voltage (v_{an} and v_p), in each phase. The operating region is highly appropriate, because the overall submodules frequency f_{sm} is constant and sub-harmonics can be neglected.

From the modulation technique point of view, the required number of active submodules per arm depends on of the grid voltage level and the voltage in each submodule capacitor. However, the total converter current effort must be considered to find a current balance across the input elements (input inductor, interphase transformer), the arm elements (arm inductors, submodule capacitors and switches) and the MFT.

Concerning the current efforts, the one-phase HVS equivalent circuit illustrated in Figure 2.5 was used. Assuming the steady-state condition without losses and the number of submodules per arm N is set to a large value. The following equations are used to describe the approximated RMS currents efforts on the input inductor I_a, interphase transformer windings I_x and I_y, the MFT primary I_p and the arms I_{arm} (KORN *et al.*, 2011).

$$I_a = \frac{\sqrt{2}\, P_{hvs}}{V_{e\_p}} \tag{3.1}$$

$$I_x = I_y = \frac{I_a}{2} \tag{3.2}$$

$$I_p = \frac{\sqrt{2}\, P_{hvs}}{V_{t\_p}} \tag{3.3}$$

$$I_{arm} = \sqrt{\left(\frac{I_a}{4}\right)^2 + \left(\frac{I_p}{2}\right)^2} \tag{3.4}$$

where, P_{hvs} is the HVS output power.

Therefore, the converter total RMS current effort I_{total} is given by

$$I_{total} = 4\, N\, I_{arm} \tag{3.5}$$

From the modulation indexes M_e and M_t equations, given by (2.24), the peak states of the voltages v_e and v_t, respectively, are calculated as

$$V_{e\_p} = \frac{N\, M_e\, V_c}{2} \tag{3.6}$$

$$V_{t\_p} = M_t\, N\, V_c \tag{3.7}$$

Substituting (3.6) and (3.7) in (3.1) and (3.3), respectively, and assuming that the HVS output power P_{hvs} is nearly equal to the converter output power P_o, the input current and the MFT primary current are calculated by

$$I_a = \frac{2\sqrt{2}P_o}{M_e\, N\, V_c} \tag{3.8}$$

$$I_p = \frac{\sqrt{2}P_o}{M_t\, N\, V_c} \tag{3.9}$$

Substituting (3.8) and (3.9) in (3.4):

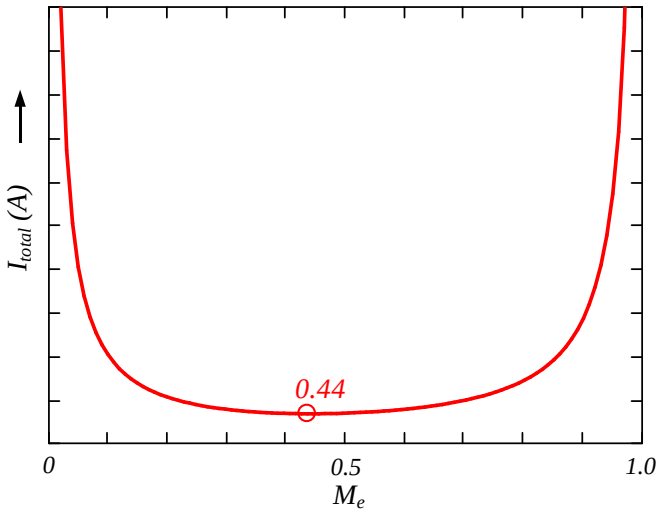
$$I_{arm} = \frac{\sqrt{2}\, P_o}{2\, N\, V_c}\sqrt{\frac{0.5}{M_e^2} + \frac{1}{M_t^2}} \tag{3.10}$$

Then, substituting (3.10) in (3.5), it results in:

$$I_{total} = \frac{2\sqrt{2}\,P_o}{V_c}\sqrt{\frac{0.5}{M_e^2}+\frac{1}{M_t^2}} \tag{3.11}$$

From (3.11), it is observed that the total current effort depends on the converter power, the submodule voltage and the modulation indices. Since the modulation indices are related to each other by (2.26), using (3.11), Figure 3.1 is obtained and describes the relation of the total current effort I_{total} versus modulation index M_e on the converter. It should be noted that these efforts are only related to the conduction losses.

Figure 3.1 – Converter total current effort I_{total} versus modulation index M_e.



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It is observed that the smaller current effort occurs when the converter operates with M_e = 0.44. For instance, by modifying the input modulation index to M_e = 0.70, the current stresses increase by 45%, while the number of submodules per arm is reduced by 37.1%.

Thus, (3.6) can be rewritten as

$$N = \frac{2\,V_{e\_p}}{M_e\,V_c} \tag{3.12}$$

In (3.12), it is assumed that the peak voltage V_{e_p} is nearly equal to the peak grid voltage V_{g_p}. Also, substituting the modulation index $M_e = 0.44$, which is the value that produces the smaller total current effort on the converter, the optimum number of submodules per arm N_{opt} can be derived and calculated by

$$N_{opt} = \frac{2\,V_{g\_p}}{M_e\,V_c} \cong \frac{2\sqrt{2}\,V_g}{0.44\,V_c} \cong 6.43\,\frac{V_g}{V_c} \tag{3.13}$$

3.1.2 Optimum transformer turns ratio k_{opt}

It is well-known that the transformer turns ratio k can be calculated by

$$k = \frac{V_p}{V_s} \tag{3.14}$$

where, V_p and V_s are the RMS primary and secondary voltages, respectively, of an ideal transformer.

The application of a sinusoidal or a square wave on the primary side will be reflected on the secondary side, *i.e.*, the full power generated by the primary voltage and current harmonics are all carried together to the secondary side.

In the AC-DC IMMC, the transformer works in the same way. As seen in the equivalent MFT primary side equation and circuit, described in (2.19) and shown in Figure 2.7 (b), respectively, the virtual voltage v_t works as the "voltage source" who supplies the transformer primary terminals. Since there is a voltage drop on the inductance L, which decreases the power transfer capability, the analysis is extended to the HVS decoupled equivalent combined with the LVS equivalent circuit (Figure 3.2). Thus, in order to adjust the voltage difference, one solution is using the fundamental values of the voltages v_t and v_s to calculate optimum transformer turns ratio k_{opt} (LEIBL; ORTIZ; KOLAR, 2017).

To obtain the analytical expressions of the voltages v_t and v_s, a new concept should be included, named here as "effective duty cycle". The effective duty cycle d is the function in time related to the intervals Δd and $\Delta d'$ of the virtual voltage v_t which transfers active power. It is understood in a similar way of the DC-DC converters duty cycle (BARBI, 2007). Figure 3.3 presents the waveforms of the grid voltage v_g, HVS and LVS carriers, virtual voltages v_e and v_t and MFT secondary voltage v_s.

Figure 3.2 – HVS decoupled MFT primary side equivalent circuit with the LVS circuit.

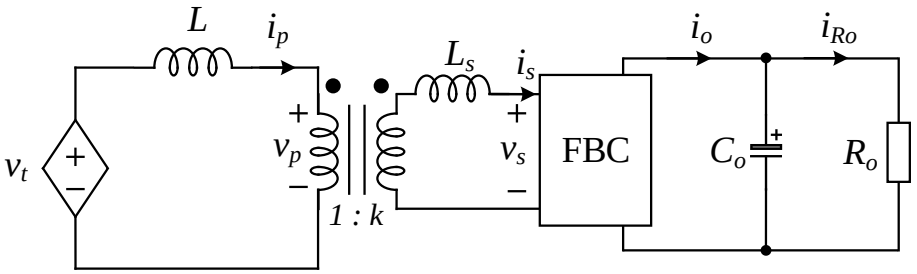

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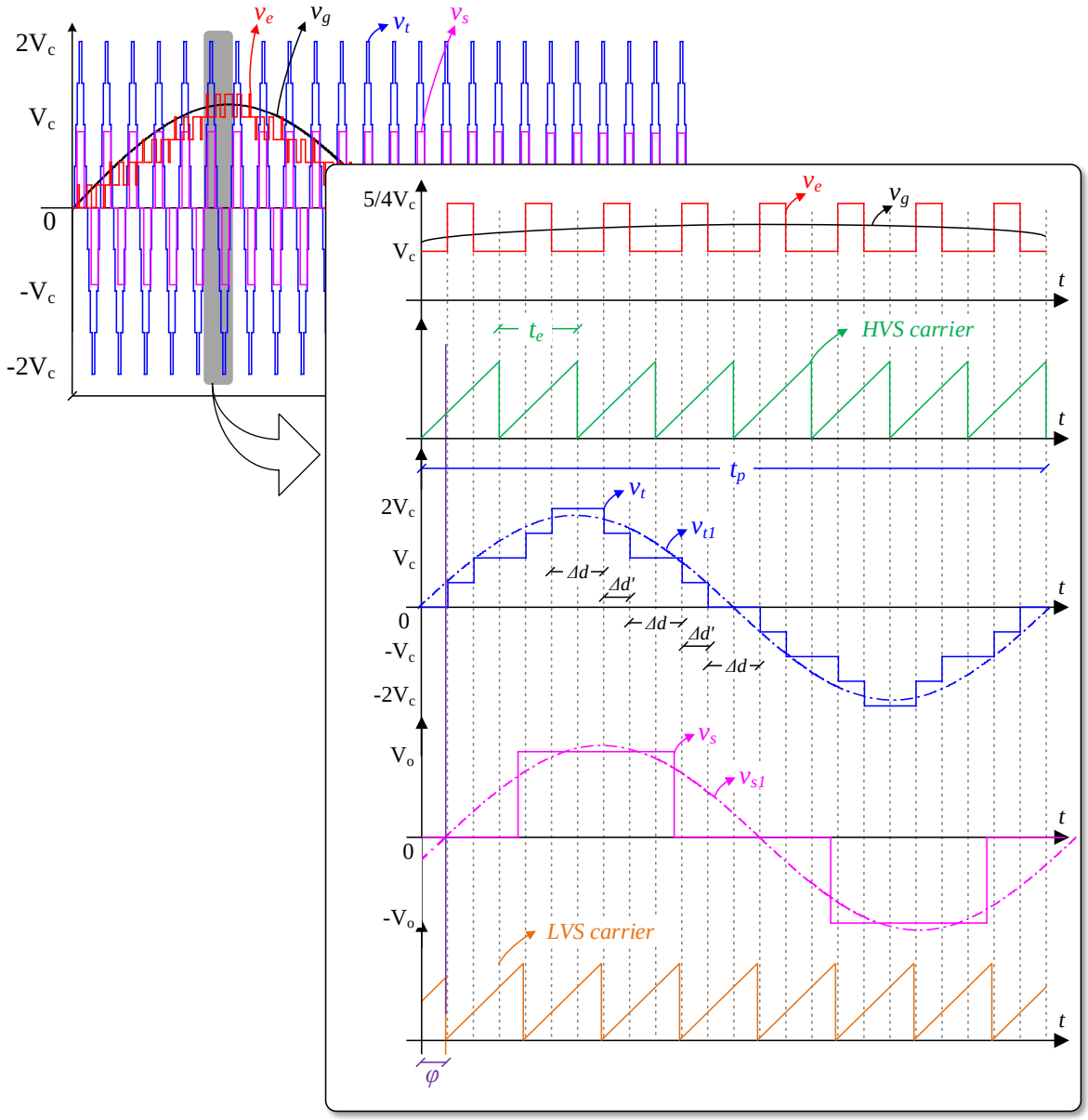
Figure 3.3 – Waveforms of the grid voltage v_g, HVS and LVS carriers, virtual voltages v_e and v_t and MFT secondary voltage v_s versus time.



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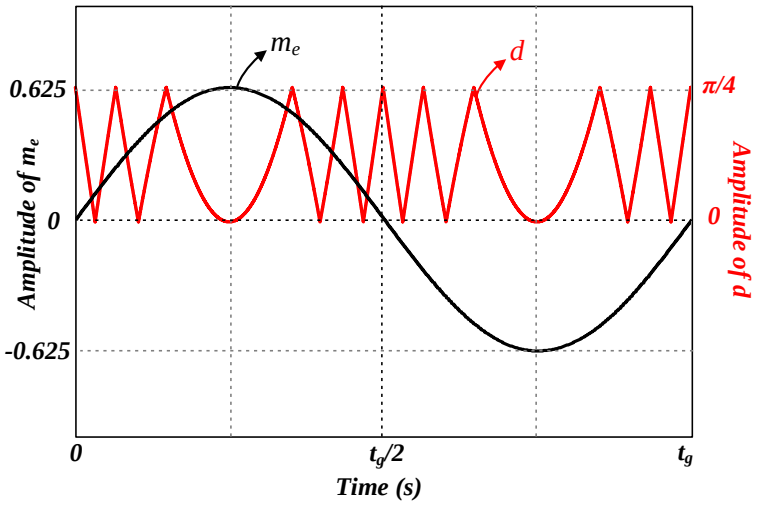
According to the input modulation index m_e versus time, given by (3.15), and the sector of the voltage v_e, the effective duty cycle trends to 0 or t_e. Thus, assuming the selected operation region from chapter 2, section 2.4, with $N = 4$ submodules per arm, the effective duty cycle is given by (3.16). The waveforms of the effective duty cycle and the input modulation index versus time are shown in Figure 3.4.

$$m_e(t) = M_e \, sin(\omega_g \, t) \tag{3.15}$$

where, ω_g is the angular frequency of the grid voltage.

$$d(t) = \begin{cases} 5\,t_e(1 - |m_e(t)|), & if\ |m_e(t)| \geq 0.8 \\ 5\,t_e(|m_e(t)| - 0.6), & if\ 0.6 \leq |m_e(t)| < 0.8 \\ 5\,t_e(0.6 - |m_e(t)|), & if\ 0.4 \leq |m_e(t)| < 0.6 \\ 5\,t_e(|m_e(t)| - 0.2), & if\ 0.2 \leq |m_e(t)| < 0.4 \\ 5\,t_e(0.2 - |m_e(t)|), & if\ 0 \leq |m_e(t)| < 0.2 \end{cases} \tag{3.16}$$

Figure 3.4 – Waveforms of input modulation index m_e and effective duty cycle d versus time.



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The virtual voltage v_e waveform has a low-frequency, with period t_g, and a medium-frequency component, with period t_e, which depends on the modulation technique operating region. The virtual voltage v_t waveform has only a medium-frequency component, with period t_e as well. According to each voltage level of v_t and the given intervals Δd and $\Delta d'$, since the

voltages v_t and v_s are periodic, the analytical expressions of the voltages v_t and v_s can be calculated using the Fourier transform equation and given as (3.17) and (3.18), respectively.

$$v_t(t) = \sum_{h=1,2,3\ldots}^{\infty} \frac{2\,V_c}{h\,\pi}\left(\begin{array}{c}\left(2\cos\left(\frac{h\,\pi}{4}\right)+1\right)\cos\left(\frac{h\,d(t)}{2}\right)+\\ \sin\left(\frac{h\,\pi}{2}\right)\sin\left(\frac{h\,d(t)}{2}\right)\end{array}\right)\cdot\sin(h\,\omega_t\,t) \tag{3.17}$$

$$v_s(t) = \sum_{h=1,2,3\ldots}^{\infty} \frac{4\,V_o}{h\,\pi}\cos\left(\frac{h\,\pi}{6}\right)\cdot\sin\big((h\,\omega_s-\varphi)t\big) \tag{3.18}$$

where, h is the order of the harmonic component, ω_t is the angular frequency of the voltage v_t and ω_s is the angular frequency of the voltage v_s (RASHID, 1999, p.764).

From (3.14), the transformer turns ratio k appears in the equation by obtaining the MFT primary voltage, which is

$$v_p(t) = \sum_{h=1,2,3\ldots}^{\infty} \frac{4\,k\,V_o}{h\,\pi}\cos\left(\frac{h\,\pi}{6}\right)\cdot\sin\Big(\big(h\,\omega_p-\varphi\big)t\Big) \tag{3.19}$$

where, ω_p is the angular frequency of the voltage v_p and equal to ω_s.

Considering only the first harmonic component in (3.17) and (3.19), *i.e.*, $h = 1$, the fundamental voltages of v_t and v_p are given by, respectively,

$$v_{t1}(t) = \frac{2\,V_c}{\pi}\left(\left(\sqrt{2}+1\right)\cos\left(\frac{d(t)}{2}\right)+\frac{\sqrt{2}}{2}\sin\left(\frac{\pi}{8}-\frac{d(t)}{2}\right)\right)\cdot\sin(h\,\omega_t\,t) \tag{3.20}$$

$$v_{p1}(t) = \frac{2\sqrt{3}\,k\,V_o}{\pi}\cdot\sin\big((h\,\omega_s-\varphi)t\big) \tag{3.21}$$

From Figure 3.4, the effective duty cycle varies from 0 to π/4. Thus, assume that the average value of the effective duty cycle d is equal to π/8, and neglect the sinusoidal components. By making (3.20) equal to (3.21), the optimum transformer turns ratio k_{opt} is given by

$$k_{opt} = \frac{v_{t1}}{v_{p1}} = \frac{V_c}{\sqrt{3}\,V_o}\left(\left(\sqrt{2}+1\right)\cos\left(\frac{\pi}{16}\right) + \frac{\sqrt{2}}{2}\sin\left(\frac{\pi}{16}\right)\right) \tag{3.22}$$

This equation is used further in the MFT design.

3.1.3 RMS value and THD of the voltage v_t

Also using the Fourier transform, the RMS values of the voltages v_t versus time can be calculated and given by

$$V_{t\_rms}(t) = \frac{V_c}{2}\sqrt{\frac{5\pi + 4\,d(t)}{\pi}} \tag{3.23}$$

In Figure 3.5 is illustrated the RMS voltage v_t, in per unit (pu), versus time. It is observed that the RMS voltage v_t waveform has a quasi-constant RMS value, which shows low ripple (smaller than 9.5%) in medium-frequency component and characterizes a stable power transfer.

Concerning the voltage total harmonic distortion (THD_v), it´s also obtained from the Fourier's transform, their respective values are summarized by:

$$THD_v = \sqrt{\sum_{h=2,3,\ldots}^{\infty}\left(\frac{V_h}{V_1}\right)^2} \tag{3.24}$$

where, V_1 is the fundamental RMS voltage and V_h is the respective *h*-harmonic RMS voltage.

Figure 3.6 shows the THD_v values of the voltages v_t, in pu, versus time. It is noted a ripple around 11.1% and the average value around 21.2%. Thus, the chosen modulation technique contributes to a low current effort on the MFT.

Figure 3.5 – RMS voltage v_t versus time.

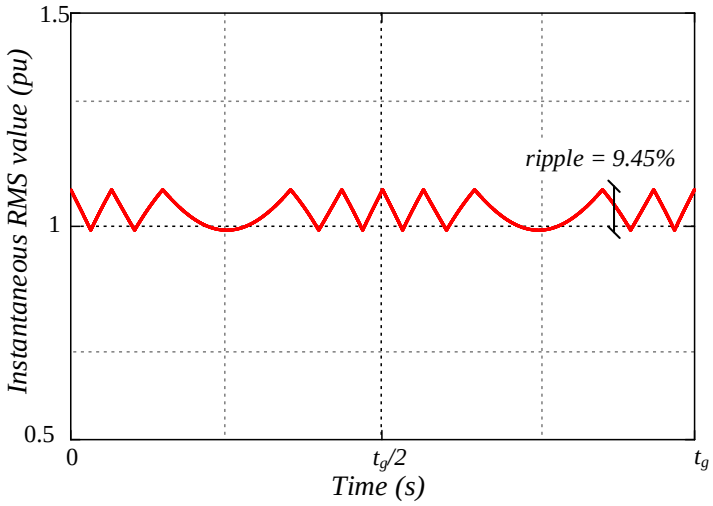

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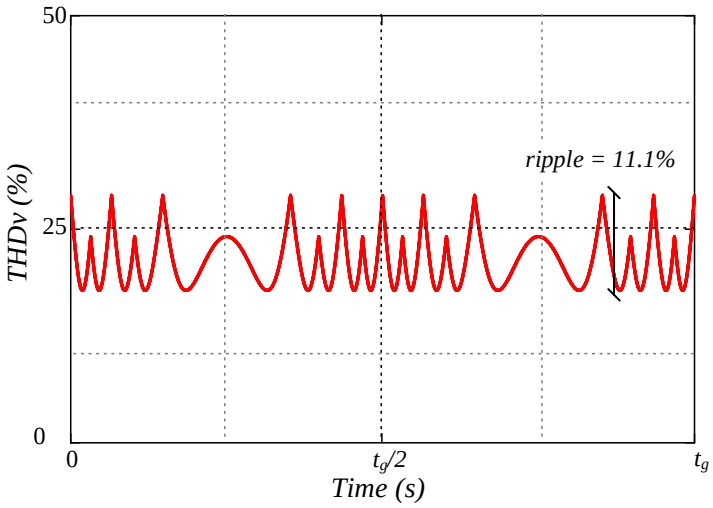
Figure 3.6 – THD_v values of the voltage v_t versus time.



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3.1.4 Losses

The converter losses can be divided as follows:

- Semiconductors conduction and switching losses
- Transformers core and windings losses
- Inductors core and windings losses

Although these losses are not described in this manuscript, a study of the proposed converter losses was presented in Joca *et al.* (2017), where a comparison was developed between the proposed three-phase IMMC and the conventional two-level voltage source

converter both operating at 100 kVA rated power and applied in the connection of low-voltage DC microgrids (380 V) to the medium voltage utility grid (13.8 kV).

Regarding the full-load converter operation, the semiconductors (switches and diodes) conduction and switching losses were calculated using the method described by Drofenik and Kolar (2005). The transformer losses were obtained after developing its design using the core geometry approach as described by McLyman (2004). Considering the transformer losses and the semiconductor losses, the converter efficiency was estimated to 88.2%. These study is probably optimistic, and more work is required to decrease the AC-DC IMMC losses in order to make it competitive. A possible solution is developing a modulation technique that could provide soft-switching operation.

When operating in no-load condition, both transformers (interleaving and MFT) still have core losses. Also, there have the interleaving transformer windings losses and the semiconductors switching and conduction losses due to being necessary to keep the submodules capacitors and the output capacitor always charged.

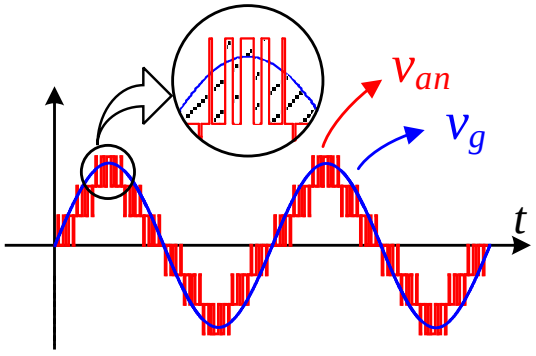
3.2 Design

The converter design is based on the converter modeling, described in chapter 2. It is divided by each component: input inductor L_g, arm inductor L, submodule capacitor C, bus capacitors C_{b1} and C_{b2} (only for single-phase topology), MFT and output capacitor C_o.

3.2.1 Input inductor L_g

The input inductor L_g is calculated following the RMS values of the difference between the grid voltage v_g and the input voltage v_{an}, as seen in Figure 3.7.

Figure 3.7 – Grid voltage v_g and input voltage v_{an} waveforms for input inductor calculation.



Source: author's right.

From Figure 2.5 and Figure 3.7,

$$v_{an}(t) = v_g(t) - L_g \frac{di_a(t)}{dt} \tag{3.25}$$

where, v_g is the grid voltage. Assuming that the peak value of the input voltage v_{an} and voltage v_e are equal. Insert (2.24) into (3.25) is rewritten as

$$\frac{M_e\, N\, V_{DC}}{2} \sin(\omega t) = \sqrt{2}\, V_g \sin(\omega t) - L_g \frac{\Delta i_a}{\Delta t} \tag{3.26}$$

where, Δi_a is the input current ripple during the interval Δt. Thus, linearizing the equation at the peak of sine wave, (3.25) becomes

$$L_g = \frac{\left|2\sqrt{2}\, V_g - M_e\, N\, V_{DC}\right|}{2\, \Delta i_a\, f} \tag{3.27}$$

where, f is the fundamental medium-frequency of the input voltage v_{an}.

3.2.2 Arm inductor L

From (2.19) and Figure 2.7, it possible to obtain a decoupled equivalent model for the MFT primary voltage v_p. The virtual voltage v_t is the "voltage source" who supplies the MFT primary, and consequently, the MFT secondary by a turn ratio k. It was already observed that its RMS analytical expression showed a low ripple and featured a stable power transfer. This proves the relationship between the value of the arm inductor L and the transferred power to the LVS according to the phase-shift angle φ.

Thus, the value of the arm inductor L is found by using power transfer equation, from the gyrator theory (SANTOS *et al.*, 2011) (OLIVEIRA FILHO, 2015), which is very similar to the synchronous generator equation and given by

$$L = \frac{V_{t\_rms}\, V_{p\_rms} \sin\varphi}{2\pi\, f_t\, P_o} \tag{3.28}$$

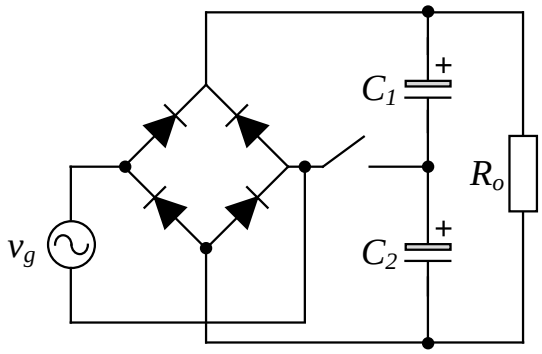
where, V_{t_rms} is the RMS value of the voltage v_t, described in (3.23), f_t is the MFT frequency, P_o is the LVS output power and V_{p_rms} is the RMS value of the voltage v_p, which is calculated using the Fourier's transform and given by

$$V_{p\_rms} = \sqrt{\frac{2}{3}}\, V_o\, k_{opt} \tag{3.29}$$

3.2.3 Submodule capacitor C

In a simplified way, the HVS of the AC-DC IMMC operates likewise the full wave rectifier as a voltage doubler, which circuit is shown in Figure 3.8 (BARBI, 2007, p. 33). Thus, submodule capacitors *C* can be obtained using the same methodology of the voltage doubler capacitors C_1 and C_2. This method is called hold-up time (BARBI, 2007, p. 34-35).

Figure 3.8 - Full wave rectifier circuit as a voltage doubler.



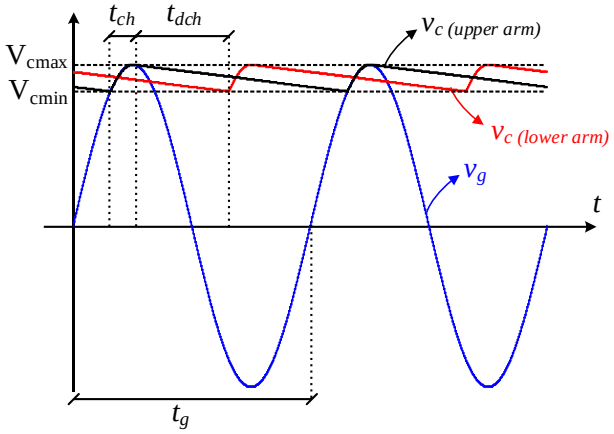
Source: adapted from Barbi (2007, p. 33).

In Figure 3.9, it is illustrated the waveforms of the grid voltage v_g and one submodule capacitor voltage of each arm (upper and lower) in the same leg. From that, the mathematical minimum submodule capacitor voltage is given by

$$V_{cmin} = V_{cmax} \cos\left(2\pi\, f_g\, t_{ch}\right) \tag{3.30}$$

where, V_{cmin} and V_{cmax} are minimum and maximum values, respectively, of the submodule capacitors voltage v_c, f_g is the grid frequency and t_{ch} is the charge time.

Figure 3.9 – Grid voltage v_g and submodule capacitor voltages v_c of the upper and lower arms (same leg) waveforms for capacitance calculation.



Source: adapted from BARBI (2007, p. 34).

Therefore, as seen in Figure 3.9, the submodule capacitors are charged in the interval t_{ch}, given by

$$t_{ch} = \frac{t_g}{2\pi} \operatorname{acos}\left(\frac{V_{cmin}}{V_{cmax}}\right) \tag{3.31}$$

From (3.31), the discharge time t_{dch} is the interval when the submodule capacitors supply the MFT, which is given as

$$t_{dch} = \frac{t_g}{2\pi}\left(2\pi - \operatorname{acos}\left(\frac{V_{cmin}}{V_{cmax}}\right)\right) \tag{3.32}$$

Since the submodule discharge energy can be calculated by

$$W_{dch} = \frac{1}{2} C \left({V_{cmax}}^2 - {V_{cmin}}^2\right) \tag{3.33}$$

Assuming the converter without losses, therefore, the converter output power P_o is equal to the HVS output power P_{HVS}. Also, considering that the HVS output power is nearly equal to the power provided by the four arms, thus

$$P_o = P_{hvs} \cong 4\, P_{arm} \tag{3.34}$$

Since each arm power is calculated by

$$P_{arm} = \frac{W_{dch}}{f_g} \tag{3.35}$$

Substituting (3.35) in (3.34)

$$P_o \cong 4\frac{W_{dch}}{f_g} \tag{3.36}$$

Then, substituting (3.33) in (3.36), the resulting submodule capacitance is

$$C = \frac{P_o \left(2\pi - \text{acos}\left(\frac{V_{cmin}}{V_{cmax}}\right)\right)}{4\pi\, f_g \left({V_{cmax}}^2 - {V_{cmin}}^2\right)} \tag{3.37}$$

3.2.4 Bus capacitors C_{b1} and C_{b2}

For the single-phase topology, the bus capacitors C_{b1} and C_{b2} are required. The value of their capacitance is obtained using the equivalent capacitance in the AC-DC IMMC topology likewise the full wave rectifier circuit as voltage doubler (Figure 3.9). Since C_{b1} and C_{b2} have the same value, the equivalent capacitance C_{bus} is given by

$$C_{bus} = \frac{C_{b1}\, C_{b2}}{C_{b1} + C_{b2}} = \frac{C_{b1}}{2} \tag{3.38}$$

Since the equivalent capacitance C_{bus} is equal to the arm equivalent capacitance

$$C_{bus} = \frac{C_{b1}}{2} = C_{arm} = \frac{C}{N} \tag{3.39}$$

Thus,

$$C_{b1} = C_{b2} = \frac{2\,C}{N} \tag{3.40}$$

3.2.5 Medium-frequency transformer

Basically, the design of the MFT needs only of the fundamental peak value of the primary voltage together with the transformer turns ratio k_{opt}, which can be found from (3.21) and (3.22), respectively. Therefore, the fundamental peak values of the MFT primary and secondary voltages are given by

$$v_{p1} = \frac{2\sqrt{3}\, k_{opt}\, V_o}{\pi} \tag{3.41}$$

$$v_{s1} = \frac{v_{p1}}{k_{opt}} = \frac{2\sqrt{3}\, V_o}{\pi} \tag{3.42}$$

3.2.6 Output capacitor C_o

The output capacitor C_o in the single-phase topology is calculated using the stored energy equation described by Barbi (2007, p. 35):

$$C_o = \frac{P_o}{f_t \left({V_{omax}}^2 - {V_{omin}}^2\right)} \tag{3.43}$$

where, V_{omax} and V_{omin} are the maximum and the minimum allowable values at the output voltage.

In the three-phase topology there is just one output capacitor C_o, which is calculated by:

$$C_o = 3\frac{P_o}{f_t \left({V_{omax}}^2 - {V_{omin}}^2\right)} \tag{3.44}$$

3.3 Simulation

Based on the converter design from section 3.2, simulations have been carried out for the three-phase AC-DC IMMC topology (Figure 2.1) presenting the parameters and specifications of Table 3.1. These specifications correspond to a 100 kVA AC-DC step-down solid-state transformer for low-voltage DC power distribution system. Note that the chosen

input modulation index M_e that provides the smallest current effort from section 3.1.1 was not considered.

Table 3.1 – Parameters and specifications for the three-phase AC-DC IMMC simulation.

Parameters	Value
Input modulation index (M_e)	0.625
Input inductor current medium-frequency ripple (Δi_a)	30%
Submodules per arm (N)	4
Submodule capacitors voltage ripple (Δv_c)	10%
Submodule switching frequency (f_{sm})	10 kHz
FBC switching frequency	20 kHz
Output capacitor voltage ripple (Δv_o)	1%
Specifications	**Value**
Grid RMS line voltage	13.8 kV / 60 Hz
Input inductor (L_g)	8.38 mH
Arm inductors (L)	53.9 mH
Submodules capacitors average voltage (V_c)	11.27 kV
Submodule capacitor (C)	5.42 µF
Transformer turns ratio (k)	44.78
Output power (P_o)	100 kW
Output voltage (V_o)	380 V
Output capacitor (C_o)	3.46 µF

Source: author´s right.

In Appendix B, the simulation schematics and parameters are shown. The simulated results are slightly different from the idealized waveform from chapter 2, where the leakage inductance effects of the interphase transformer and the arm inductors were neglected.

3.3.1 Steady-state operation

The steady-state operation of the converter can be seen in the following figures. In Figure 3.10 are shown the grid phase voltages ($v_{g,a}$, $v_{g,b}$, $v_{g,c}$) and the input currents (i_a, i_b, i_c) waveforms. The power factor is 0.999, the THD_i (current Total Harmonic Distortion) is 2.71% and the $WTHD_i$ (current Weighted Total Harmonic Distortion) is 1.71%. Thus, the converter

meets the requirements for THD_i limits (<5%), standardized by IEEE STD 519-2014 (IEEE, 2014, p. 7). The current ripple calculated by the simulation software is around 21.3%.

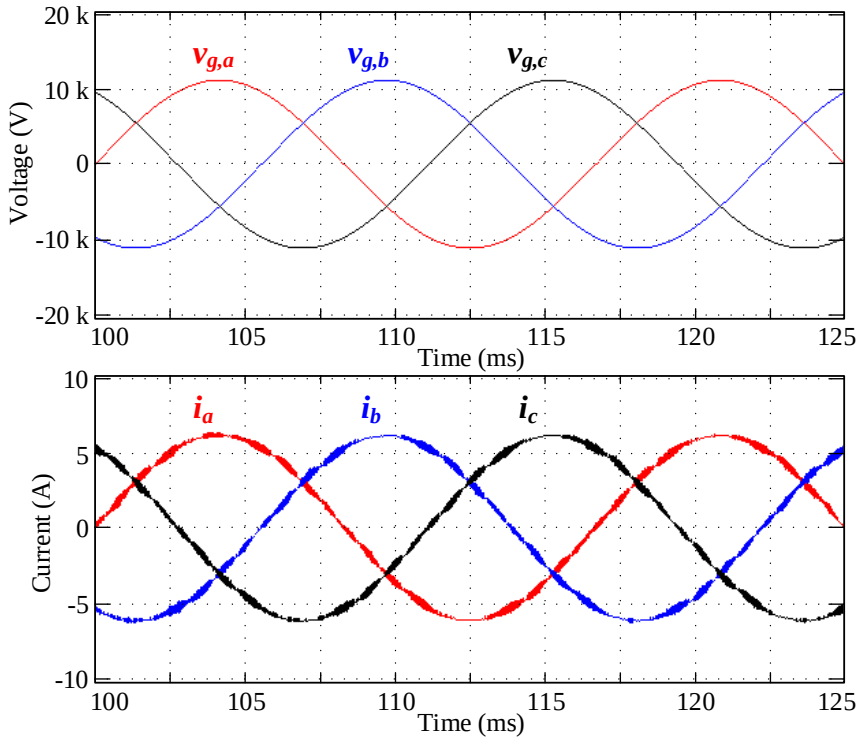
Figure 3.11 illustrates the input voltages waveforms v_{an}, v_{bn}, v_{cn}. There are 11 voltage levels, their THD_v is 13.65% and their $WTHD_v$ (voltage Weighted Total Harmonic Distortion) is 0.1%.

Figure 3.12 shows the instantaneous voltages across submodule capacitors in each phase. The average voltage per arm is regulated at 11.2 kV, whose voltage ripple is about 8.1%. It meets the requirements since it was design to obtain 10%.

Figure 3.13 shows the waveforms of the virtual voltage v_t, the MFT primary voltage v_p. The phase-shift angle φ between them is kept at 21°, and the MFT primary current in phase a. The results in other phases are similar.

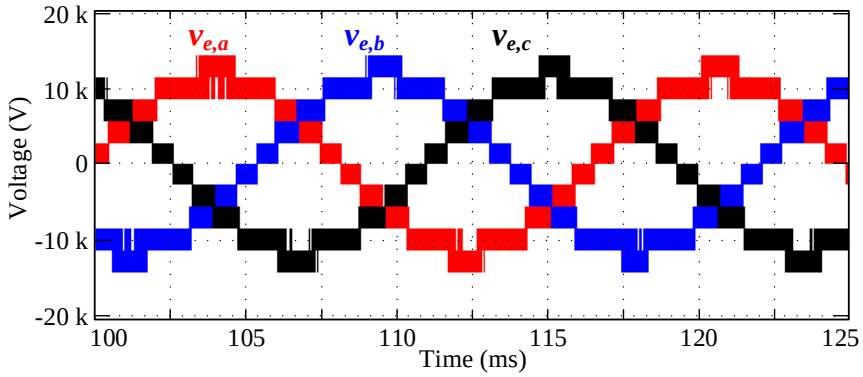
Figure 3.14 presents the waveforms of the circulating currents i_{cx} and i_{cy} through each phase, whose average and RMS values are about 0 A and 67 mA, respectively. It meets the requirement since designed values should be near zero.

Figure 3.10 – Simulated 3-phase grid voltages ($v_{g,a}$, $v_{g,b}$, $v_{g,c}$) and input currents (i_a, i_b, i_c).



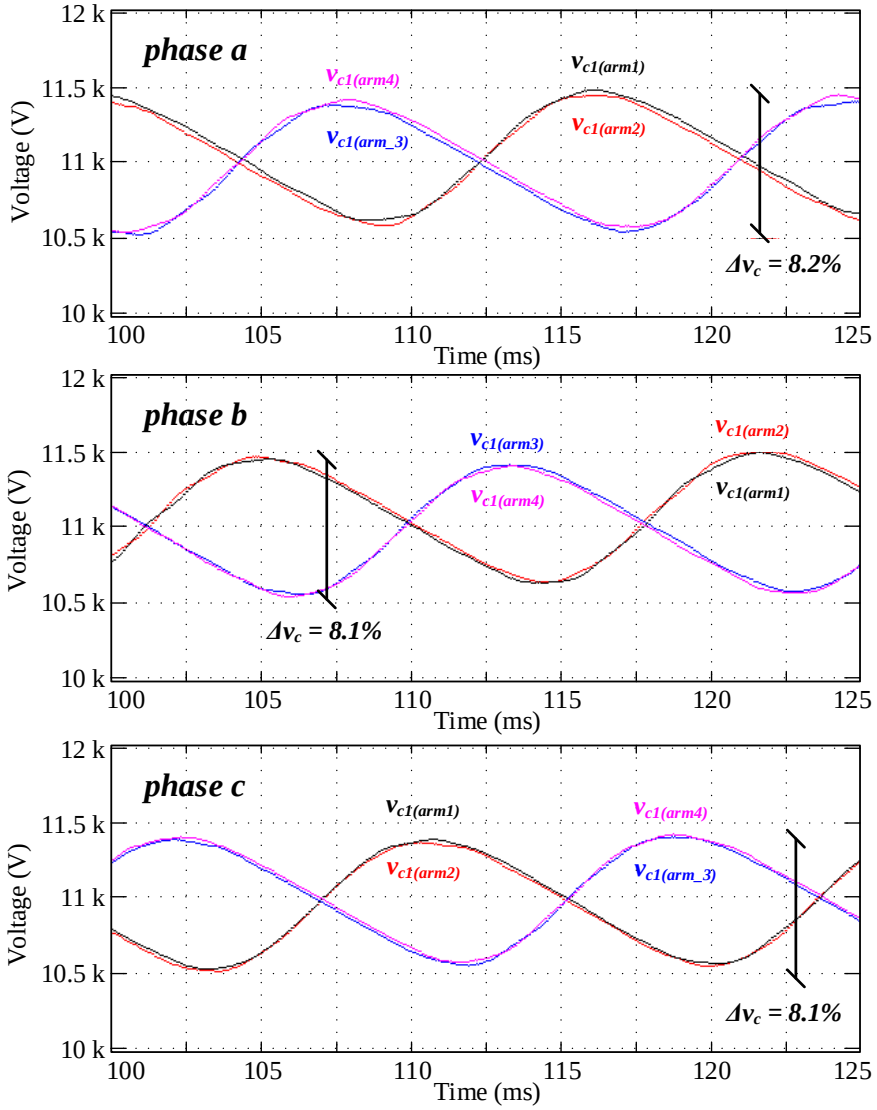
Source: author's right.

Figure 3.11 – Simulated 3-phase virtual voltages $v_{e,a}$, $v_{e,b}$ and $v_{e,c}$.



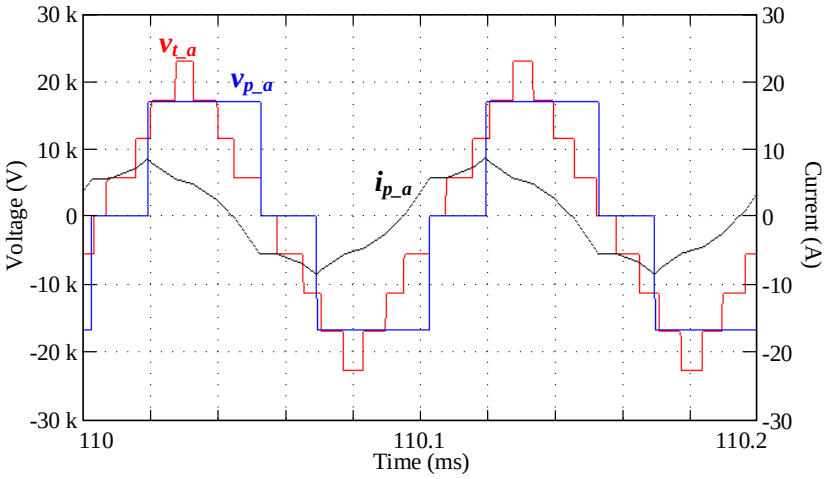
Source: author's right.

Figure 3.12 – Simulated voltages across one submodule capacitor in each arm.



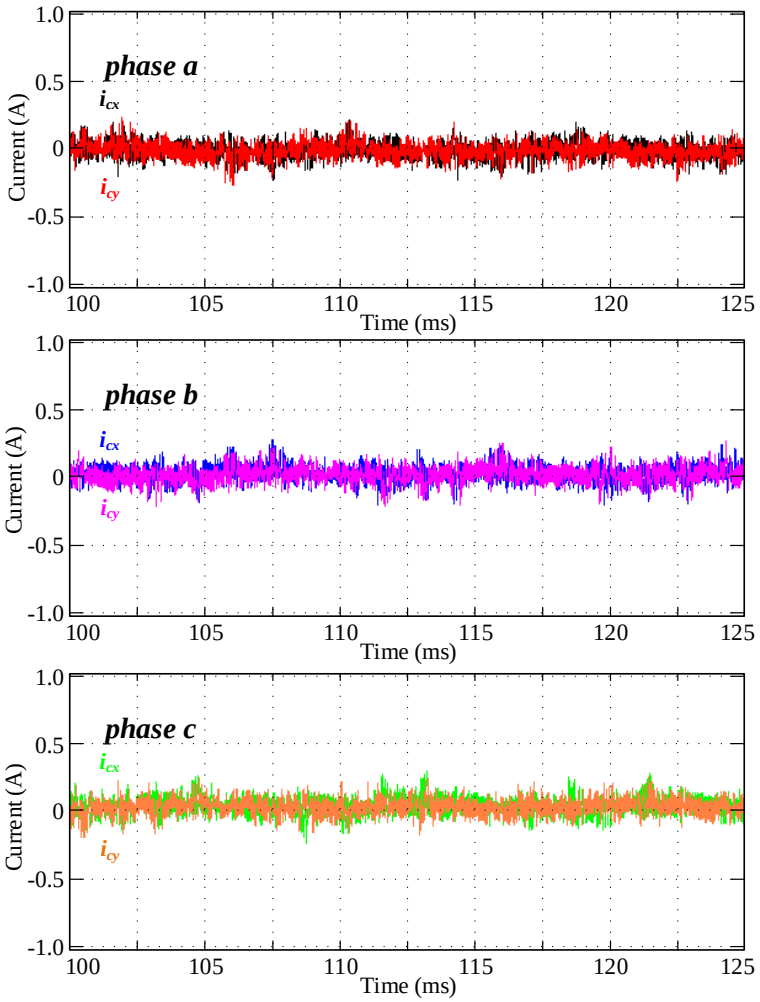
Source: author's right.

Figure 3.13 – Simulated voltage v_t, the MFT primary voltage v_p and the MFT primary current in phase *a*.



Source: author's right.

Figure 3.14– Simulated circulating currents i_{cx} and i_{cy}.



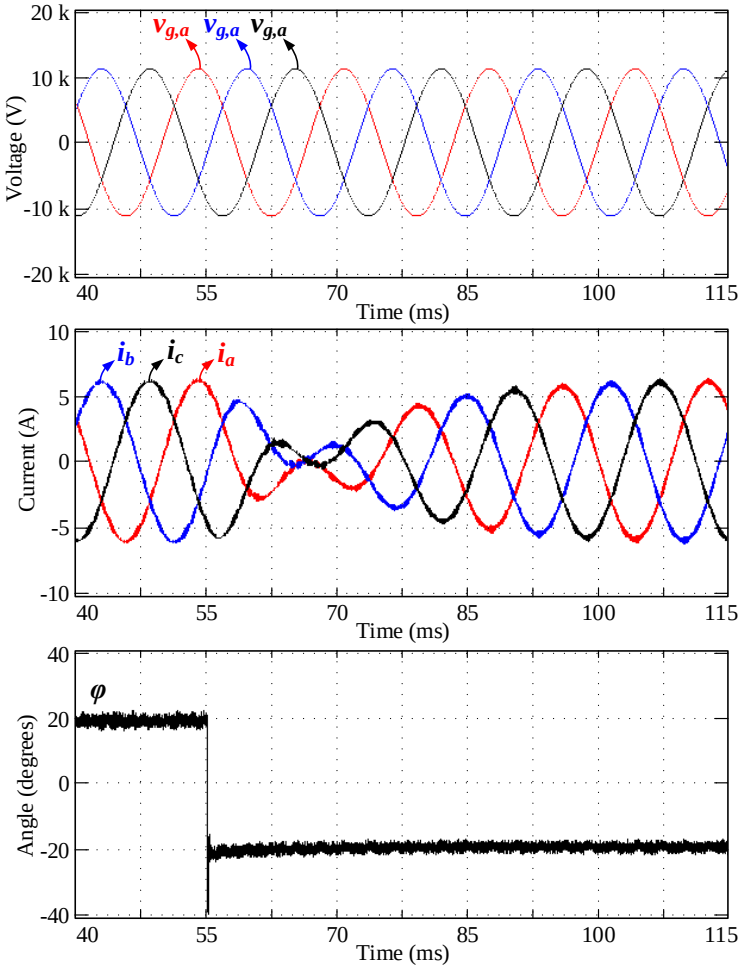
Source: author's right.

3.3.2 Power flow inversion operation

A power flow inversion sequence was performed to evaluate the control scheme stability and the bidirectionality feature, both in the worse-case scenario: at the peak point of the one phase voltage and at nominal power.

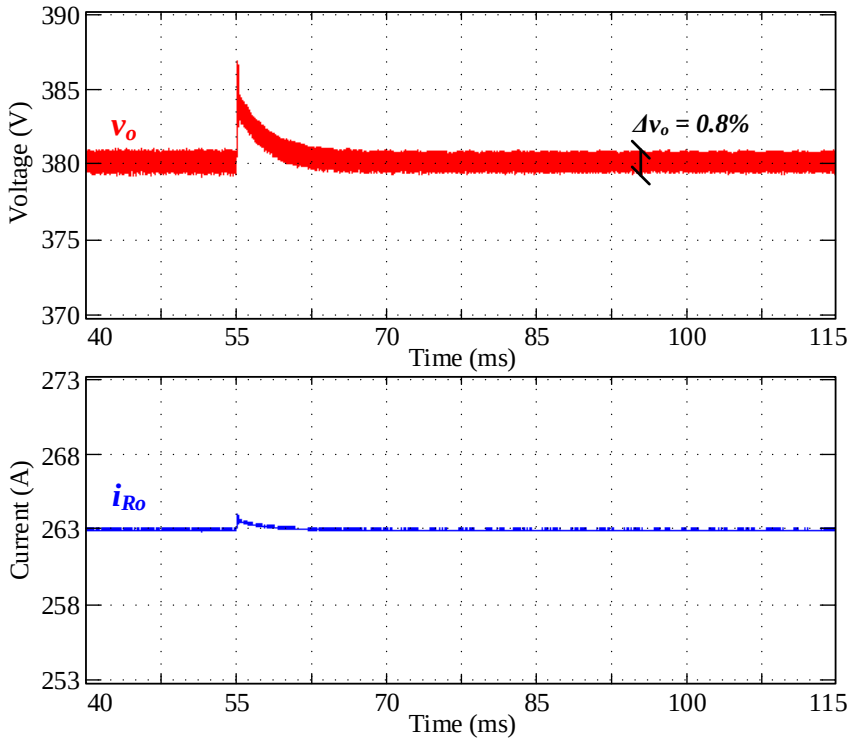
Results are shown in Figure 3.15 and Figure 3.16. From t = 40 ms to t = 55 ms, the grid 3-phase voltages ($v_{g,a}$, $v_{g,b}$, $v_{g,c}$), the input currents (i_a, i_b, i_c) waveforms and the MFT phase-shift angle φ between the primary and the secondary side show that the converter operates in rectifier mode. This means that the converter is absorbing active power from the AC grid to the DC grid. the output voltage v_o is regulated at 380 V, and the load current i_{Ro}, kept around 263 A. Both of them have a ripple smaller than 0.2% and the supplied power to the DC load is 100 kW.

Figure 3.15 – Simulated grid phase voltages and the input currents in power flow inversion condition.



Source: author's right.

Figure 3.16 – Simulated output voltage v_o and the load current i_{Ro} in power flow inversion condition.



Source: author's right.

At t = 55 ms, the power flow is inverted to 100% of the nominal power. The converter operates in inverter mode. This means that the converter is supplying active power from the DC grid to the AC grid. This power flow inversion represents a worst-case scenario and thus demonstrates that the proposed AC-DC IMMC controller is stable. The input currents stabilize at their nominal values in a time interval of less than 60 ms, while the output voltage and the load current achieves their nominal values in about 5 ms.

3.4 Final comments

This chapter presented three analyses, the design and the simulation of the proposed AC-DC interleaved modular multilevel converter with medium-frequency transformer.

This first analysis was realized to obtain the optimized number of submodules. The analysis took into account the chosen operating region in the modulation technique and finding the smaller total current efforts. This feature is important for the current sharing across the converter input and arms.

The second analysis was developed to obtain the optimized transformer turns ratio, considering the HVS and LVS structures behavior.

The last analysis consisted of verifying the virtual voltage v_t behavior, since this voltage works as a “voltage source” who supplies the MFT terminal. As a result, it was found out that it presents a stable operation for the entire converter operation.

Considering the converter study and the three analyses presented in this chapter, the converter design was developed. Even though some assumptions were adopted, the converter elements (inductors, capacitors, transformer, etc.) were obtained using fundamental concepts presented in strong power electronics references.

The design could be verified through simulation made with a three-phase 100 kVA AC-DC IMMC. The parameters were respected and matched with the simulation results. The steady-state and the dynamic operations were implemented, which respect the requirements standardized by IEEE STD 519-2014 for the connection of a medium-voltage AC grid to a low-voltage DC grid.

All the important voltages (grid, capacitors, virtual voltages, transformer and output) and currents (input, arms, circulating, transformer and load) were analyzed in software simulation and matched with the study developed in chapter 2 and chapter 3. Also, the control system was validated, since the load step and the power flow inversion conditions provided the stability and the bidirectionality features.

4 EXPERIMENTAL VALIDATION

4.1 Prototype specifications and overview

A single-phase prototype was developed for the experimental validation of the proposed AC-DC IMMC with medium-frequency transformer topology. The prototype was built at Laboratory GeePs (Group of Electrical Engineering – Paris), France. The author visited this group from 3rd October, 2016 to 12th January 2018 as part of an Erasmus Mundus partnership between Brazil and France, Project Smart[2].

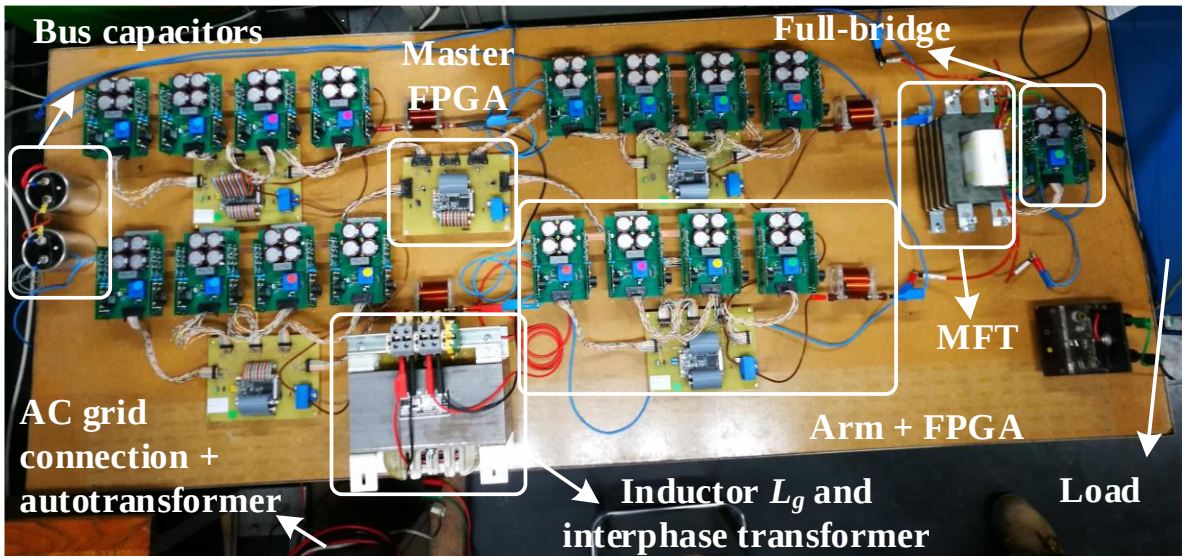
For this prototype, considering various constraints (material availability, delay of fabrication, technical skills of the technicians, budget, laboratory voltage limits, etc.), the parameters and specifications summarized in Table 4.1 were decided. A photo of the prototype is shown in Figure 4.1 and its schematic circuit is illustrated in Figure 4.2.

Table 4.1 – Parameters and specifications for the single-phase AC-DC IMMC prototype.

Parameters	Desired value	Prototype value
Input modulation index (M_e)	0.625	
Input inductor current medium-frequency ripple (Δi_a)	30%	
Submodules per arm (N)	4	
Submodule capacitors voltage ripple (Δv_c)	10%	
Submodule switching frequency (f_{sm})	10 kHz	
Output capacitor voltage ripple (Δv_o)	1%	
Specifications	**Desired value**	**Prototype value**
Grid RMS phase voltage (V_g)	220 V / 50 Hz	27 V / 50 Hz
Input inductor (L_g)	1.5 mH	2 mH
Interphase transformer	1.8 kVA 94/94 V – 50 Hz	
Bus capacitors (C_{b1} and C_{b2})	840 µF/400V	2200 µF/400V
Arm inductors (L)	9 µH	9.4 µH
IGBT modules	600 V/40A	600 V/40A
Submodules capacitors (C)	420 µF/400V	4x 550 µF/250V
Voltage across submodules capacitors (V_c)	320 V	25 V
Medium-Frequency Transformer	4.5 kVA 190/300 V – 10 kHz	
Output capacitor (C_o)	200 µF/250V	4x 550 µF/250V
Output voltage (V_o)	380 V	20 V
Output power (P_o)	2 kW	720 W

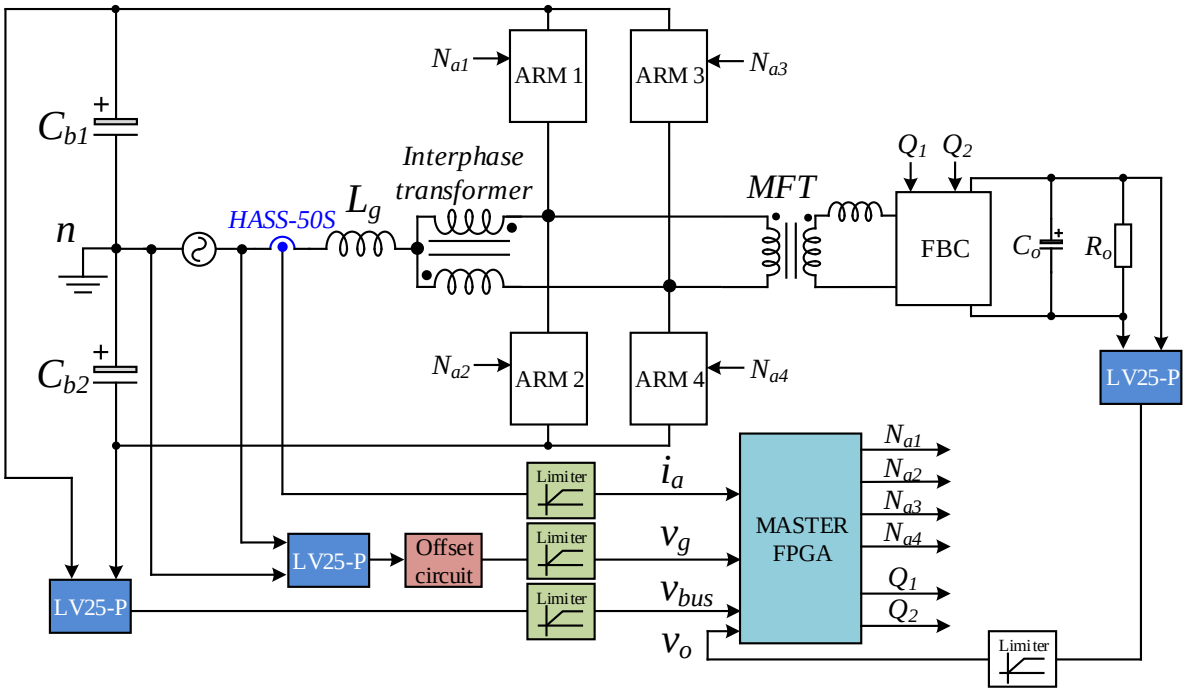
Source: author´s right.

Figure 4.1 – Photo of the single-phase AC-DC IMMC prototype with MFT.



Source: author's right.

Figure 4.2 – Schematic of the single-phase AC-DC IMMC with MFT.



Source: author's right.

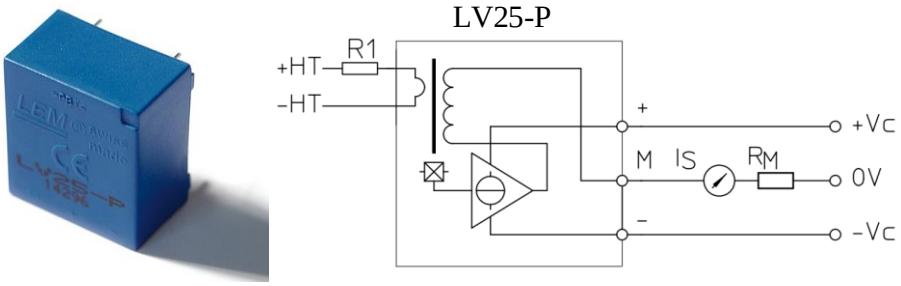
4.1.1 Overview of the prototype

The utility grid is connected to an autotransformer to operate manually the converter input voltage. The HVS is composed of two bus capacitors (C_{b1} and C_{b2}), the input

inductor (L_g) and has two MMC legs. Each leg has two arms. Each arm has an arm inductor and four half/full-bridge submodules, which are controlled by an arm FPGA. The medium-frequency transformer connects the HVS to the LVS. The LVS is composed of one full-bridge submodule, which is connected to the load. The master FPGA manages the four arm FPGAs, the controllers of the input current, bus voltage and the output voltage, and the HVS and LVS modulation techniques.

The grid voltage v_g, the submodule capacitors voltages v_c, and the output voltage v_o are measured using the voltage sensor: "LV25-P" from LEM® (Figure 4.3 shows the its photo and its circuit). The gain depends on the measured voltage, the voltage supply (±12 V or ±15 V), the input resistance R_1 and the measuring resistance R_M. The Table 4.2 describes the gains for each voltage measurement. Since the grid voltage achieves positive and negative values, and the FPGA works only with between 0 and 3.3 V, an external offset circuit was implemented and set to 1.65 V.

Figure 4.3 – Voltage sensor LEM® LV25-P: (a) photo and (b) connection circuit.



(a) (b)

Source: LEM® (2018) (www.lem.com).

Table 4.2 – Specifications for the voltage sensors.

Voltage measurement	Maximum voltage	R_1	R_M	Gain
Grid phase voltage (v_{grid})	130 V	13 kΩ	130 Ω	0.025
Submodule capacitors voltage (v_{cap})	150 V	15 kΩ	130 Ω	0.0217
Output voltage (v_o)	150 V	15 kΩ	130 Ω	0.0217

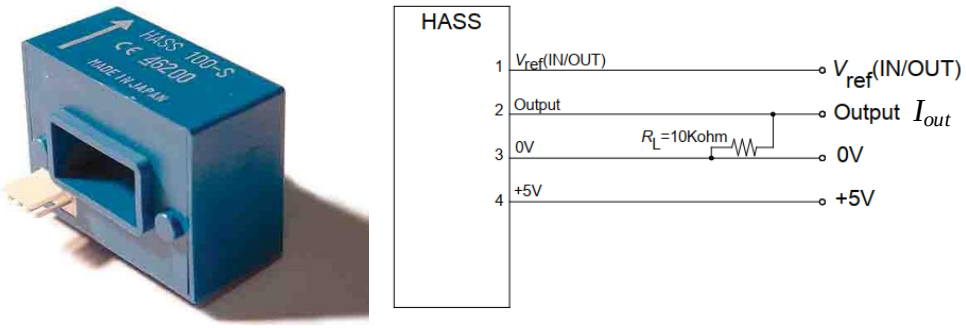
Source: author´s right.

As seen in Figure 4.1 and Figure 4.2, the input current i_a and the arm currents (i_1, i_2, i_3, i_4) are measured through the hall effect current sensors "HASS 50-S" from LEM®, which photo is shown in Figure 4.4. The measured current I_{in} in the sensor can be either positive or

negative between -50 A and 50 A, and its output I_{out} is a voltage signal ranged between 0 and 5 V with a 2.5 V offset and calculated by (4.1):

$$I_{out} = I_{in} \times 0.625 + 2.5 \quad V \tag{4.1}$$

Figure 4.4 – Current sensor LEM® HASS-50S: (a) photo and (b) connection circuit.



(a) (b)

Source: LEM® (2018) (www.lem.com).

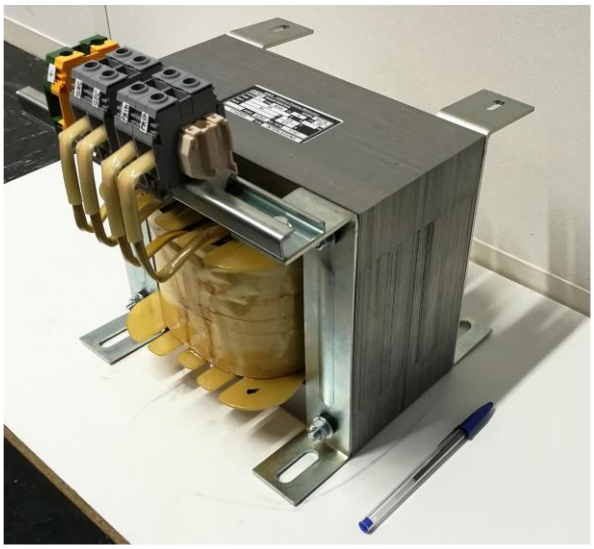
The interphase transformer was developed by the company SERDI® (2018), which followed the converter voltages, currents and frequency operation. It is rated at 1.8 kVA 94/94 V 50 Hz. The designed and the measured specifications are detailed in Table 4.3. Its photo is shown in Figure 4.5.

Table 4.3 – Designed and measured specifications for the interphase transformer produced by SERDI®.

Measurement	**Designed**		**Measured**		
	Primary	**Secondary**	**Primary**	**Secondary**	**Measured at**
Nominal voltage	94 V	94 V	94 V	94 V	@ 100 Hz
Nominal current	9.5 A	9.5 A	9.5 A	9.5 A	@ 100 Hz
Winding series resistance	-	-	4 Ω	4 Ω	@ 100 Hz
Winding series inductance	-	-	75 mH	75 mH	@ 100 Hz
			10 mH	10.45 mH	@ 10 kHz

Source: author´s right.

Figure 4.5 – Photo of the interphase transformer.



Source: author's right.

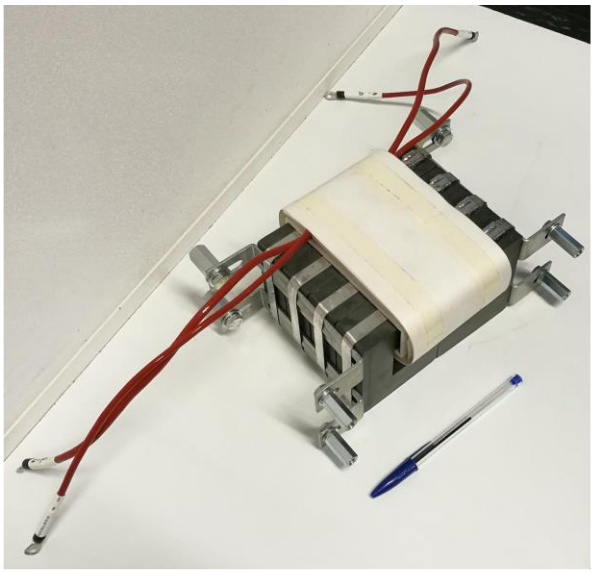
In the same way, the medium-frequency transformer was developed by the company SERDI®, which followed the frequency operation and the simulation voltages and currents. It is rated at 4.5 kVA 190/300 V 10 kHz. The designed and the measured specifications are detailed in Table 4.4. Its photo is shown in Figure 4.6.

Table 4.4 – Designed and measured specifications for the MFT produced by SERDI®.

Measurement	**Designed**		**Measured**		
	Primary	**Secondary**	**Primary**	**Secondary**	**Measured at**
Nominal voltage	190 V	300 V	190 V	300 V	@ 100 Hz
Nominal current	12 A	7.2 A	12 A	7.2 A	@ 100 Hz
Winding series resistance	-	-	51.9 mΩ	75 mΩ	@ 100 Hz
			70 mΩ	124 mΩ	@1 kHz
			220 mΩ	650 mΩ	@10 kHz
			18.4 Ω	45.5 Ω	@100 kHz
Winding series inductance	-	-	1.15 mH	2.82 mH	@ 100 Hz
			1.15 mH	2.86 mH	@1 kHz
			1.15 mH	2.84 mH	@10 kHz
			1.21 mH	3.02 mH	@100 kHz

Source: author´s right.

Figure 4.6 – Photo of the medium-frequency transformer.

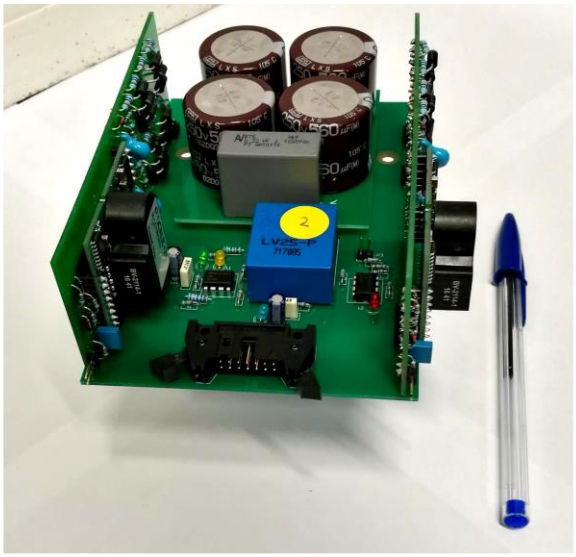


Source: author's right.

4.1.2 Overview of one submodule

The photo of the one half/full-bridge submodule is illustrated in Figure 4.7. Since all the submodules can work either as a half-bridge or full-bridge converter by selecting the proper gate-emitter signals, the converter arm is composed by four half-bridge submodules and the LVS converter uses the same submodule working as a full-bridge converter.

Figure 4.7 – Photo of one half/full-bridge submodule.



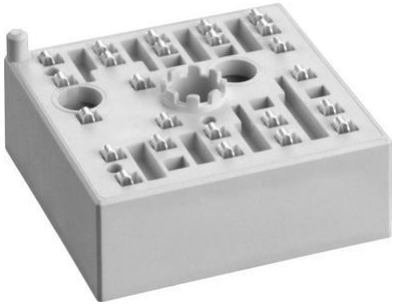
Source: author's right.

Each submodule was composed by two drivers “Dual-Channel SCALE™-2+ 2SC0108T-17” from PowerIntegrations® (2018) (Figure 4.8) and its auxiliary components, one full-bridge IGBT module “SKiiP 16GH066V1” rated at 600 V/40A from SEMIKRON® (2018) (Figure 4.9), one voltage sensor “LV25-P” from LEM® (2018), one overvoltage protection circuit and one overheat protection circuit.

Figure 4.8 – Photo of the driver “Dual-Channel SCALE™-2+ 2SC0108T-17” from PowerIntegrations®.

Source: PowerIntegrations® (2018) (www.power.com).

Figure 4.9 – Photo of the full-bridge IGBT module “SKiiP 16GH066V1” from SEMIKRON®,



Source: SEMIKRON® (2018) (www.semikron.com).

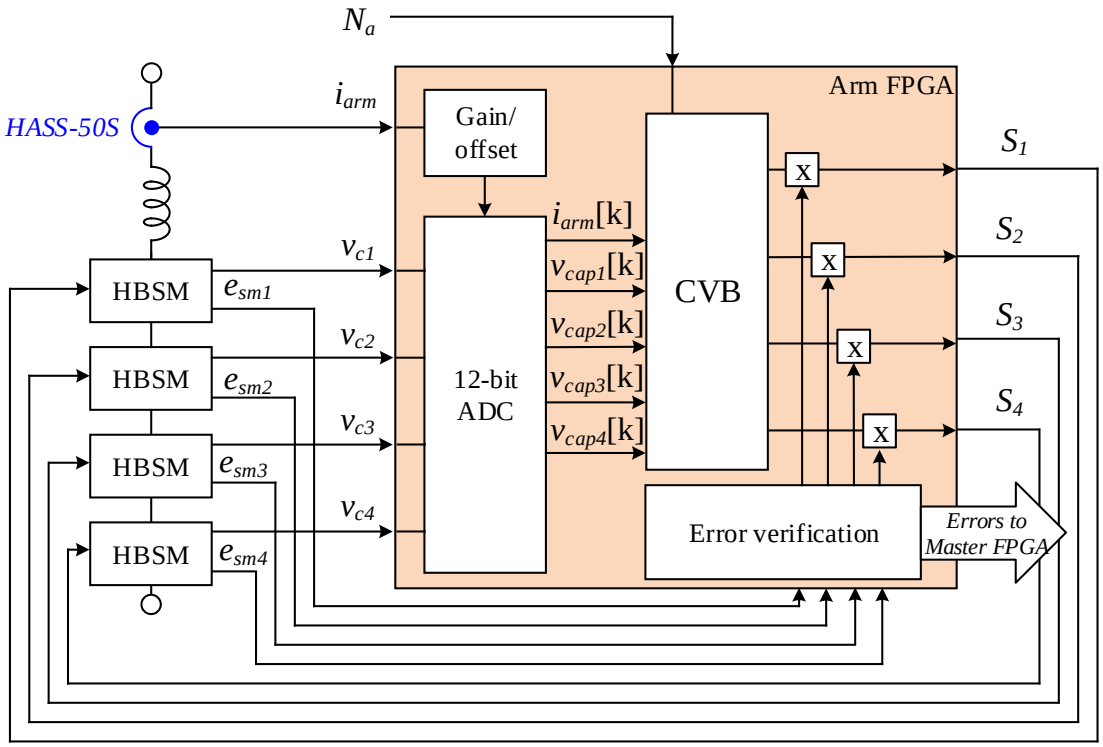
4.1.3 Overview of the arm FPGA

The operation of the arm FPGA in steady-state mode is illustrated in Figure 4.10. The chosen FPGA model was the “Cyclone IV DE0-Nano EP4CE22F17C6N” from INTEL/ALTERA® (2018) company, which photo is shown in Figure 4.11. Each arm has its respective FPGA (same model), which task set is:

- Verifying the submodule errors (e_{sm}): driver status output (SO), which indicates any problem related to power supply, IGBT OH (overheat) pin and IGBT OV (overvoltage);
- Measuring the arm current (i_{arm}) through the hall effect current sensors "HASS 50-S" from LEM®;
- Measuring the voltage of each submodule capacitor of the arm (v_{c1}, v_{c2}, v_{c3}, v_{c4});
- Receiving the number of active submodules (N_a);
- Sorting the submodules capacitors voltage (CVB - capacitor voltage balancing);
- Sending the signals (S_1, S_2, S_3, S_4) according to the capacitor voltage balancing algorithm to the submodule drivers.

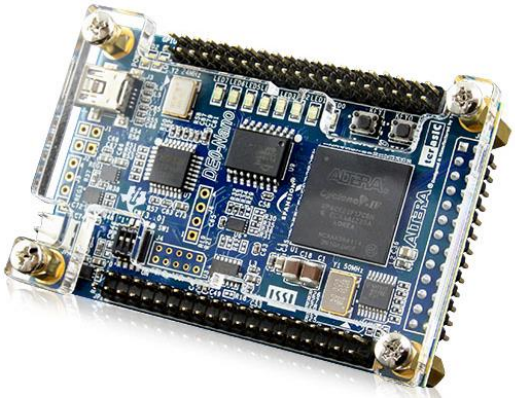
Since the selected FPGA works only with values between 0 and 3.3 V, there is a 0-3.3 V limiter at its inputs (Figure 4.2). In the arm FPGA code, there is a "gain/offset" block (Figure 4.10) to adjust the gain and the offset values to enable the calculation in positive and negative values.

Figure **Error! No text of specified style in document.**.10 – The converter arm with its FPGA code schematic.



Source: author's right.

Figure **Error! No text of specified style in document.**.11 – Photo of the "Cyclone IV DE0-Nano EP4CE22F17C6N" FPGA.



Source: INTEL® (2018) (www.intel.com).

4.1.4 Overview of the master FPGA

The converter is monitored and controlled by the master FPGA. The chosen FPGA model was also the "Cyclone IV DE0-Nano EP4CE22F17C6N" from INTEL/ALTERA® (2018) company. The master FPGA has three operation modes:

a) Initialization mode: error verification in each arm, input or output signals;
b) Charge mode: charging of the submodules capacitors;
c) Steady-state mode: operation with open loop control or closed loop control.

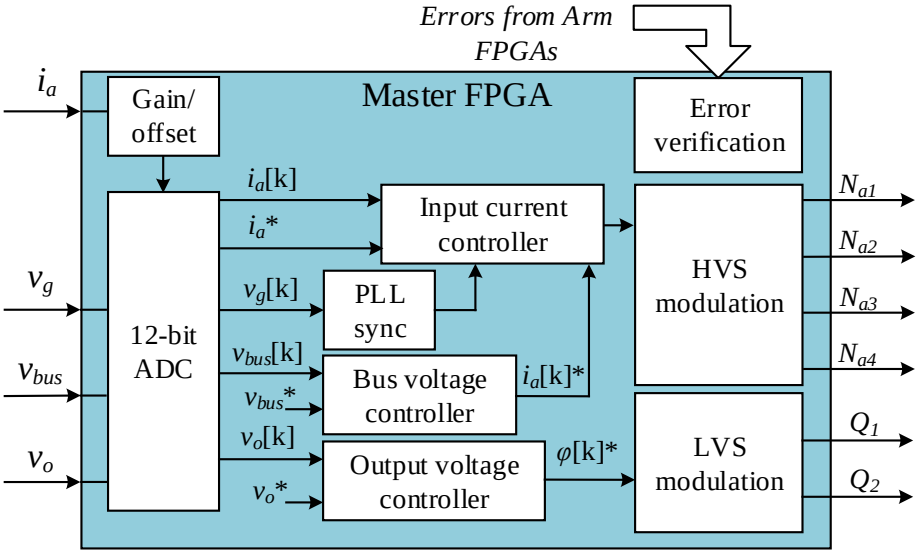
The operation of the master FPGA in steady-state mode is illustrated in Figure 4.12. It is responsible for:

- Checking if any arm has a problem (disconnection, driver power supply, IGBT module overvoltage or IGBT module overheat);
- Synchronizing the modulator signal with the grid voltage through the phase-locked loop (always turned on);
- sending the number of active submodules (N_{a1}, N_{a2}, N_{a3} and N_{a4}) determined by the HVS modulation to the arm FPGAs (charge and steady-state conditions only);
- Measuring and regulating the AC input current (input current controller) (steady-state condition only);
- Measuring and regulating the DC bus voltage (bus voltage control) (steady-state condition only);

- Measuring and regulating the DC output voltage (output voltage control) (steady-state condition only);
- Sending the gate-emitter signals (Q_1 and Q_2) determined by the LVS modulation to the full-bridge converter drivers (steady-state condition only).

As seen in Figure 4.2, there is a 0-3.3 V limiter at its inputs, since the selected FPGA works only with values between 0 and 3.3 V. Thus, in the master FPGA code, there is also a "gain/offset" block (Figure 4.12) to adjust the current sensor gain and the offset values to enable the calculation in positive and negative values.

Figure 4.12 – Master FPGA code schematic.



Source: author's right.

4.2 Experimental results

Four tests were developed for the converter experimental validation:

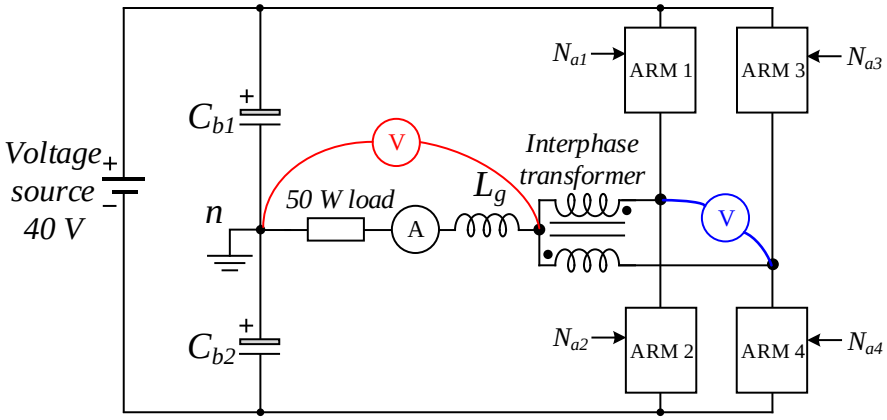
1) Steady-state operation with open loop control;
2) Steady-state operation with closed loop control;
3) Dynamic operation with closed loop control under load switching condition;
4) Dynamic operation with closed loop control under power flow inversion condition.

Each test had a different experimental setup.

4.2.1 Steady-state operation

The results of the steady-state operation with open loop control were obtained using the configuration setup shown in Figure 4.13. In this first test, it was performed the verification of the HVS modulation technique and the prototype HVS behavior. A voltage source was inserted in the bus voltage terminals and set to 40 V. The load was placed in the grid connection point and set to 50 W.

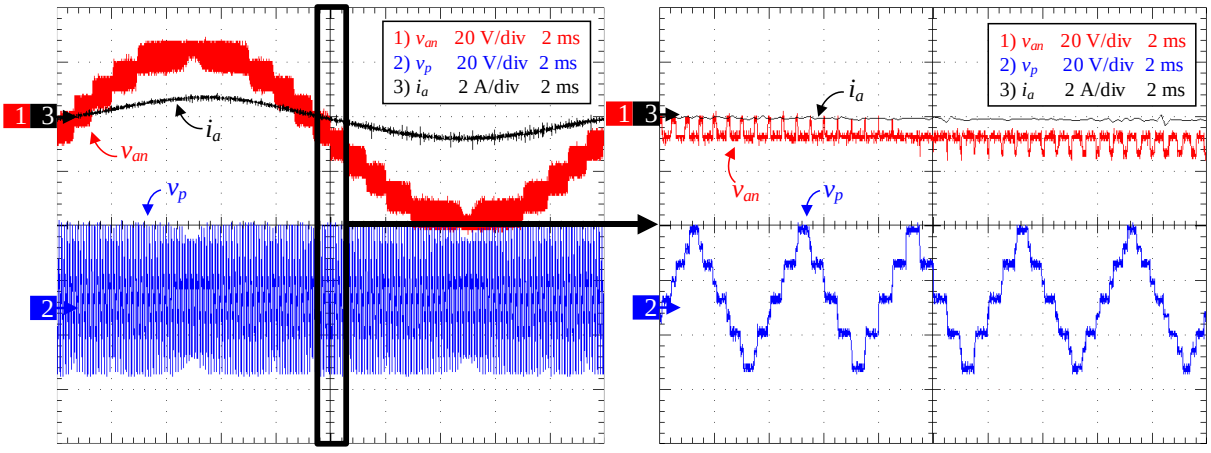
Figure 4.13 – Configuration setup for the steady-state operation with open loop control.



Source: author's right.

Figure 4.14 shows the input voltage v_{an}, the MFT primary voltage v_p and the input current i_a. The waveforms are exactly equivalent to those obtained in software simulation. This means that the modulation technique developed in the FPGA was correctly done.

Figure 4.14 – Measured steady-state operation on HVS: input voltage v_{an}, MFT primary voltage v_p and the input current i_a.

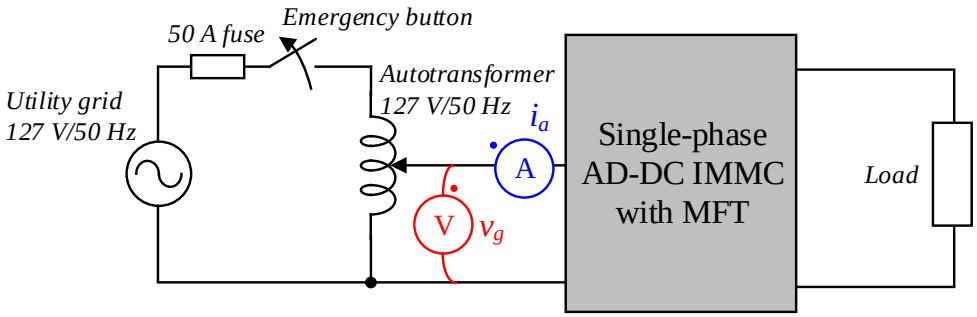


Source: author's right.

In the second test, the results were obtained from the steady-state operation with closed loop control and rated power condition using the configuration setup shown in Figure 4.15. The converter was fully assembled, *i.e.*, HVS and the LVS were connected to the MFT primary and secondary terminals, respectively. The utility grid was connected to the 127 V/50 Hz autotransformer. An emergency button and a 50 A fuse were added for security reasons. The terminals of the autotransformer were connected to the converter input terminals. The load was placed at the converter output and set to 0 W, initially.

When the master FPGA was in charge mode, the input peak voltage was increased to 40 V, which allowed the submodule capacitors to be charged and the PLL synchronization. When the submodules capacitors were charged, the master FPGA was switched to steady-state mode, where the load could be set to 720 W.

Figure 4.15 – Configuration setup for the steady-state operation with closed loop control and rated power condition.



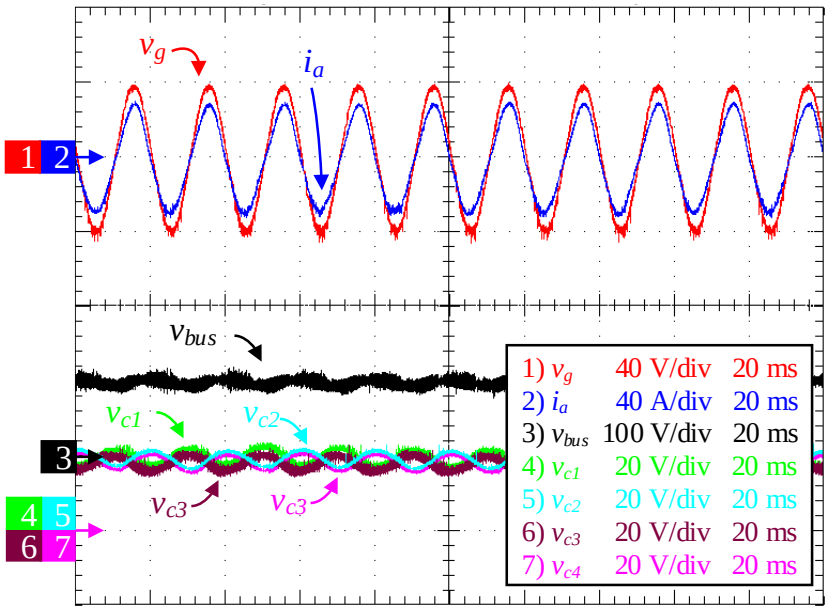
Source: author's right.

Thus, results of the steady-state operation with closed loop control are shown in Figure 4.16, the single-phase grid voltage v_g, the input current i_a, the bus voltage v_{bus}, and the voltages across one submodule capacitor of each arm v_{c1}, v_{c2}, v_{c3} and v_{c4}. The input power factor was 0.99 and the THD_i was 3.47% when the DC bus voltage v_{bus} was regulated at 100 V. The prototype met the requirements for THD_i limits (<5%), standardized by IEEE STD 519-2014 (IEEE, 2014, p. 7). The measured DC bus voltage ripple is around 9.8% and the submodules capacitors voltages ripples are around 9.2%.

Figure 4.17 shows the primary voltage v_p, the secondary voltage v_s and the secondary current i_s of the 10 kHz MFT. Note that the phase-shift angle φ between the primary and secondary voltages is regulated by the output voltage control, which controls the power transfer to the load in the rectifier mode. The step-like oscillating primary voltage v_p is due to

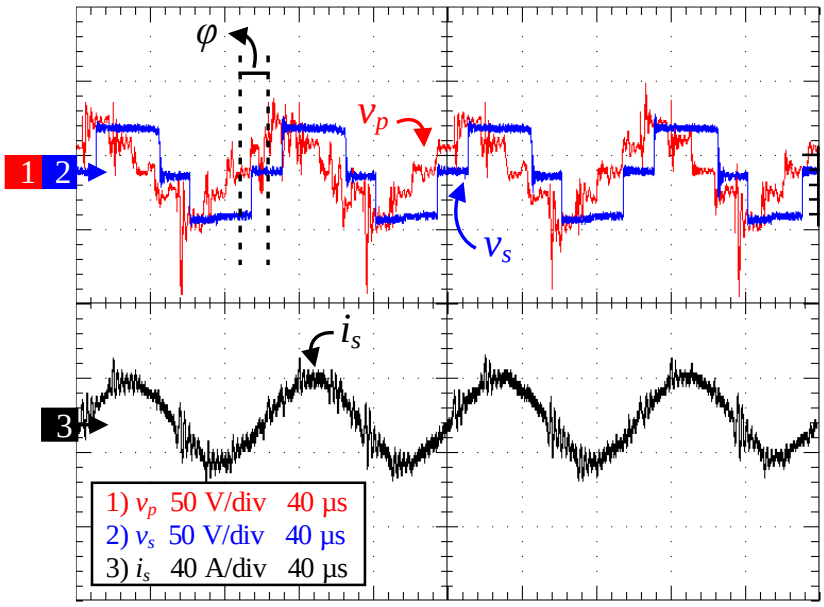
the switching of the submodules and to the medium-frequency current components through the MFT.

Figure 4.16 – Measured steady-state operation on HVS: grid voltage v_g, input current i_a, bus voltage v_{bus} and voltages across one submodule capacitor of each arm v_{c1}, v_{c2}, v_{c3} and v_{c4}.



Source: author's right.

Figure 4.17 – Measured steady-state operation on MFT: primary voltage v_p, secondary voltage v_s, phase-shift angle φ and secondary current i_s.



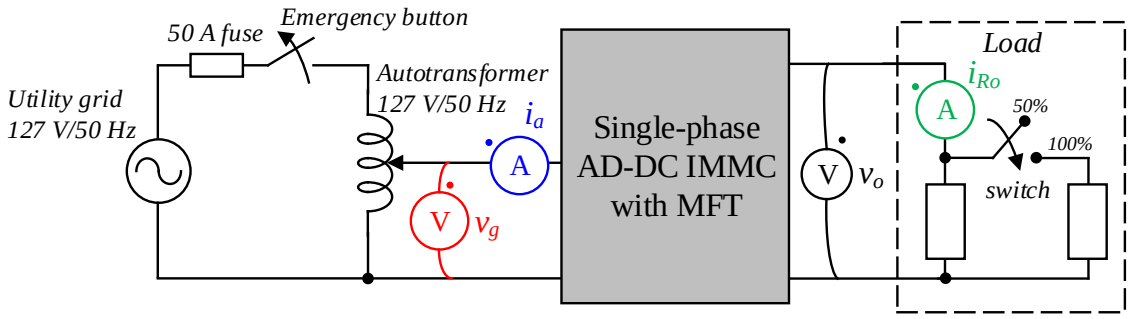
Source: author's right.

4.2.2 Dynamic operation

For the dynamic operation, two sequences were considered: load switching and power flow inversion.

The load step configuration setup is shown in Figure 4.18. It consisted of the same configuration of the steady-state operation with closed loop control including another load in parallel. Each load demanded 50% of the rated power and it was triggered by a manual switch.

Figure 4.18 – Configuration setup for the steady-state operation with closed loop control and load switching condition.



Source: author's right.

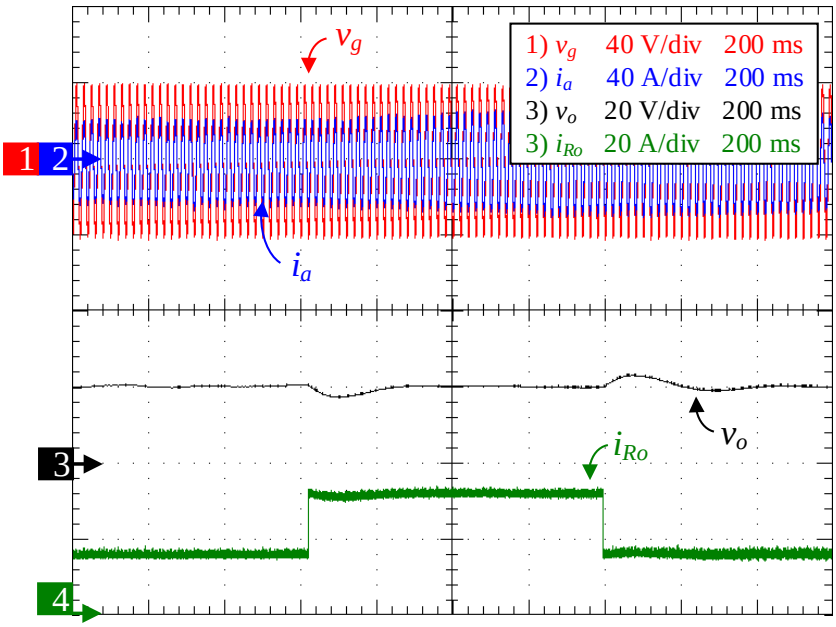
The results of the load switching from 360 W to 720 W (50% to 100% of the rated power) are shown in Figure 4.19. The grid voltage v_g, the input current i_a, the output voltage v_o and the load current i_{Ro}. The controller regulates successfully the output voltage at 20 V. The efficiency obtained at rated power was 87.4%.

Even though the test was not easy to elaborate, the results were a success. The issues were caused due to the interphase transformer and the medium-frequency transformer leakage inductances, which weren't expected to be so high and some noises were obtained in the measurements. The control system had to be recalculated to adjust the converter operation and digital filters were added in FPGA program code.

For the power flow inversion test, since in the laboratory there weren't bidirectional supplies, the configuration setup was prepared according to the circuit in Figure 4.20. To prevent the reverse current flow, which could cause damage to the voltage source, the diode D_x and the resistor R_x were placed in series with it. This setup allows the voltage source to work as

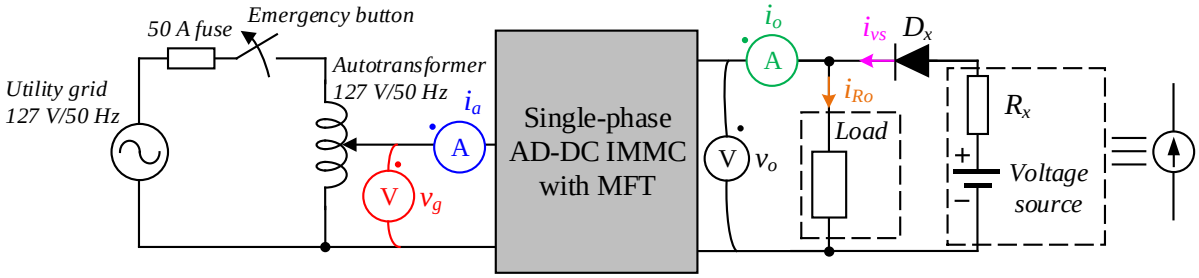
a “current source” and it ensured that the AC-DC IMMC control system could regulate the output voltage v_o without interference from the voltage source internal regulator.

Figure 4.19 – Measured dynamic operation: condition with load switching: grid voltage v_g, input current i_a, output voltage v_o and load current i_{Ro}.



Source: author’s right.

Figure 4.20 – Configuration setup for the steady-state operation with closed loop control and power flow inversion condition.



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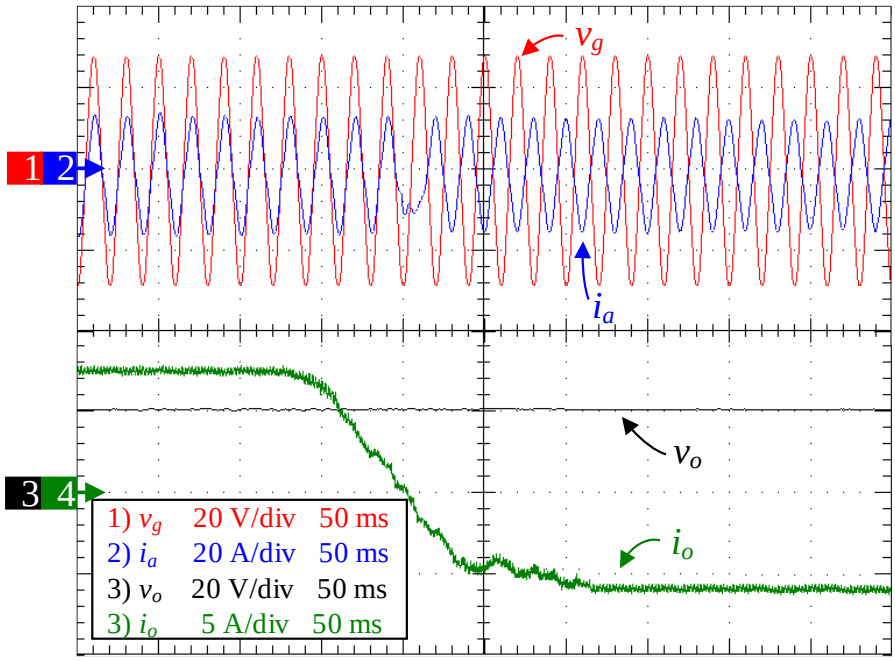
The power flow inversion test was performed when the voltage source value was increased, then the current i_{vs} was increased as well. The load was supplied by the current i_{vs} and demanded less output current i_o from the AC-DC IMMC. When the current i_{vs} was higher than the load current i_{Ro}, the phase-shift angle φ reversed as well as the input current i_a and the output current i_o. The results of the power flow inversion from 150 W to -120 W (20% to -18% of the rated power) are shown in Figure 4.21, where the grid voltage v_g, the input current i_a, the

output voltage v_o and the load current i_{Ro} are presented. This means that the converter was absorbing active power from the AC grid and supplying the DC grid, then it reverses the power flow. Thus, it was supplying active power from the DC grid to the AC grid. This demonstrates the fourth quadrant operation of the converter.

Figure 4.21 – Measured dynamic operation: power flow inversion: grid voltage v_g, input current i_a, output voltage v_o and output current i_o.

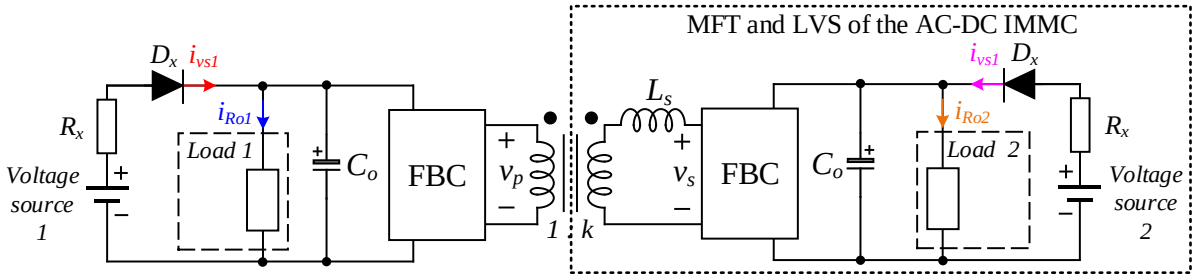


Source: author's right.

Some issues were also faced in this test concerning the difficulty to employ the power flow inversion test, such as the interference generated by the medium-frequency transformer and the transformers high leakage inductance, and the test itself complexity. To overcome these problems, a dual-active bridge converter was built separately, using two full-bridge converters and the medium-frequency transformer (Figure 4.22) (QIN; KIMBALL, 2013) and the same specifications of the proposed converter.

The LVS controller settings were adjusted and the dual-active bridge was tested in open and closed loop control including the load switching and the power flow inversion tests. This way, the full-bridge converter was placed back in the AC-DC IMMC using the new LVS controller settings and the power flow inversion test was successfully performed.

Figure 4.22 – Dual-active bridge converter built for adjusting the proposed LVS controller settings.



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4.3 Final comments

This chapter presented the prototype and experimental validation of the proposed AC-DC IMMC with a medium-frequency transformer. The converter parameters and specifications were designed but some constraints, such as material availability, delay of fabrication, technical skills of the technicians, laboratory voltage limits, and budget, forced a downgrade of the voltages and the rated power.

The prototype structure was presented and could be verified through experimental tests performed with a single-phase 720 W AC-DC IMMC. The steady-state and the dynamic operations were implemented, which attend the requirements standardized by IEEE STD 519-2014 for the connection of an AC grid to a DC grid.

The results were successfully obtained. The main voltages (grid, capacitors, transformer and output) and currents (input, transformer, output and load) matched with the simulation results. The control system was validated, since the load step and the power flow inversion conditions provided the stability and the bidirectionality features.

During the tests, some issues were addressed, such as the medium-frequency transformer interference and the high leakage inductance of the interphase and the medium-frequency transformer which forced the recalculation of the controller settings. In order to overcome these problems, a deep magnetics design must be developed.

5 CONCLUSIONS

Multilevel converters are gaining popularity for high-power medium-voltage applications due to their several characteristics such as high number of voltage levels, THD reduction, etc. The modular multilevel converters are becoming a consolidated solution in the industry for HVDC applications and the new state-of-the-art for new topologies applied in AC and DC power distribution systems. Also, a group of power converter uses not only the MMC-based structure, but also brings a new interleaving feature combined together with the medium-frequency transformer. If the three topologies advantages could be combined, they can be used as solid-state transformers solutions components applied in DC power distribution systems.

Therefore, in this work, a novel topology called "AC-DC interleaved modular multilevel converter with a medium-frequency transformer" was proposed. It is particularly suitable for the connection of the medium-voltage utility grid (13.8 kV) to the low-voltage DC microgrids (380 V_{DC}). The interleaving and the use of a medium frequency transformer bring results in a modular integrated single-stage bidirectional structure, with medium-frequency isolated AC-DC conversion. Original feature of the converter includes the mathematical modeling of the IMMC, which allows the simultaneous generation of the low-frequency grid voltage and the medium-frequency transformer primary voltage. Also, the capacitor voltage balancing and the circulating currents minimization are combined together in a single algorithm.

Starting from the converter structure, a detailed modeling of the converter allowed to imagine an operating principle. The development of an original modulation technique and the design of an adapted control system were essential steps allowing us to demonstrate the stable operation of the converter. Before going towards the realization of a prototype, a dedicated study dealing with the modulation helped to choose the appropriate modulation techniques on each converter side.

Four analyses were developed in order to obtain the optimum number of submodules N_{opt}, the optimum transformer ratio k_{opt}, to evaluate the virtual voltage v_t behavior, concerning its RMS value and total harmonic distortion, and to understand the converter losses under full-load and no-load conditions. Also, the AC-DC IMMC design is described and tested through simulation for a 100 kVA three-phase converter applied as an AC-DC stage of a DC power distribution system. The steady-state and the dynamic operations. are simulated. The proposed converter achieved the requirements standardized by IEEE STD 519-2014 for the connection of a medium-voltage AC grid to a low-voltage DC grid.

Another step was concluded with the design and construction of a small-scale single-phase prototype, at GeePs laboratory in France in partnership with Brazil. Even though some constraints, such as material availability, delay of fabrication, technical skills of the technicians, and budget were faced to elaborate the parameters and specifications of the converter, the proper behavior of the converter was experimentally validated for steady-state and dynamic operations.

Several issues were addressed due to the noises in the measurements and the high leakage inductances of the interphase transformer and medium-frequency transformer and the difficulty of the power flow inversion test. The medium-frequency transformer operation didn't occur as expected, mainly because it wasn't easy do build and design.

The converter has some drawbacks, such as a complex structure and a large number of switches and passive elements (capacitors and inductors). Depending on its implementation, issues can be faced such as high switching losses, complex control and modulation technique. To make this converter more competitive, one would need to decrease the losses and, as one possible solution is developing a modulation technique that could provide a soft-switching operation.

In conclusion, the study demonstrates the feasibility of using solutions that require solid-state transformers, such as an AC-DC stage, for the connection between AC utility grids and DC microgrids. The proposed converter had the characteristics necessary for this type of application and complied with the recommendations of Brazilian and international standards.

In future works, the study of the proposed converter in a back-to-back configuration could be carried out. Such topology could be interesting for AC-AC solid-state transformers. In an attempt to further reduce the footprint of the converter, one could consider using a three-phase MFT instead of one MFT per phase. The design and realization of medium-frequency transformers proved difficult, and therefore such topology would probably require a detailed study of the MFT alone.

5.1 Scientific production

The scientific or technical papers were published in the last five years spent on PhD studies are presented as follows.

5.1.1 Proceedings papers

- JOCA, D. R.; BARRETO, L. H. S. C.; OLIVEIRA, D. S.; PRAÇA, P. P. **A single-phase isolated AC-DC converter using an interleaved MMC**. IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC), p. 1-6, Fortaleza, 2015.
- JOCA, D. R.; BARRETO, L. H. S. C.; OLIVEIRA, D. S.; PACHECO, J. O. **Three-phase AC-DC solid-state transformer for low-voltage DC power distribution applications**, 12th IEEE International Conference on Industry Applications (INDUSCON), p. 1-8, Curitiba, Brazil, Nov 2016.
- PACHECO, J. O.; BRITO, F. J. B.; JOCA, D. R.; OLIVEIRA, J. L. W.; PRAÇA, P. P.; OLIVEIRA JR, D. S. **Bidirectional modular multilevel PFC rectifier based on cascading full-bridge and interleaving technique suitable for SST applications**. 12th IEEE International Conference on Industry Applications (INDUSCON), p. 1-6, Nov 2016.
- JOCA, D. R.; BARRETO, L. H. S. C.; OLIVEIRA JR, D. S.; QUEVAL, L.; DZONLAGA, B.; VANNIER, J.-C. **AC-DC Interleaved Modular Multilevel Converter with Medium-Frequency Isolation Transformer for DC Micro-grids**. International Conference on Components and Systems for DC grids, Grenoble, France, Feb 2017.
- DZONLAGA, B.; JOCA, D. R. **Amélioration du Contrôle d'un Convertisseur AC-DC Modulaire Multiniveaux Entrelacé**. Jeunes Chercheurs en Génie Electrique - JCGE 2017, Arras, France, 2017.
- DZONLAGA, B.; JOCA, D. R.; QUEVAL, L.; VANNIER, J.-C. **Transient analysis of a modular multilevel converter with coupled arm inductors**. 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), p. 1662, San Antonio, USA, 2018.

5.1.2 Journal papers

- JOCA, DAVI R.; BARRETO, L. H. S. C.; OLIVEIRA JR, D. S. QUEVAL, L.; VANNIER, J.-C.; DZONLAGA, B. Estudo e Validação Experimental de um Conversor Multinível Modular Entrelaçado CA-CC Monofásico para Aplicações de Transformadores de Estado Sólido. **Revista Eletrônica de Potência**, p. 1-10, Oct 2018.

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BAHRANI, B.; RUFER, A.; KENZELMANN S.; LOPES, L. A. C. Vector Control of Single-Phase Voltage-Source Converters Based on Fictive-Axis Emulation. **IEEE Transactions on Industry Applications**, v. 47, n. 2, p. 831-840, March-April 2011.

BARBI, I. **Eletrônica de Potência**: projetos de fontes chaveadas. 2. ed. Florianópolis: Edição do Autor, 2007.

BARRETO, L. H. S. C.; HONÓRIO, D. de A.; OLIVEIRA, D. de S.; PRAÇA, P. P. An Interleaved-Stage AC-DC Modular Cascaded Multilevel Converter as a Solution for MV Railway Applications. **IEEE Transactions on Industrial Electronics**, v. 65, n. 4, p. 3008–3016, April 2018.

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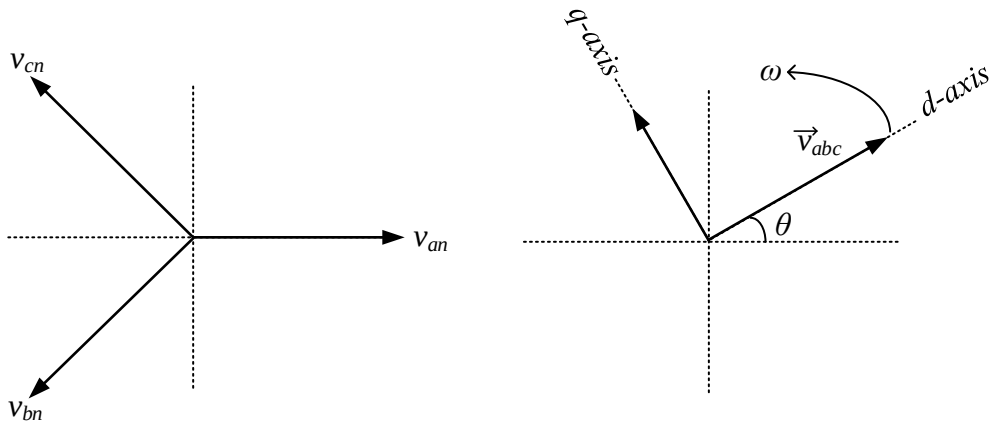
APPENDIX A – HVS PLANT IN ROTATING REFERENCE FRAME

In Figure A.1a is described the phasor diagrams of the abc-frame and dq-frame to obtain the HVS plant.

Figure A.1 – Phasor diagram: (a) abc-frame and (b) dq-frame.



(a) (b)

Source: author's right.

The grid voltages v_{an}, v_{bn}, v_{cn} are given as:

$$v_a(t) = \sqrt{2}\, V_g \sin(\omega t) \tag{A.1}$$

$$v_b(t) = \sqrt{2}\, V_g \sin\left(\omega t - \frac{2\pi}{3}\right) \tag{A.2}$$

$$v_c(t) = \sqrt{2}\, V_g \sin\left(\omega t - \frac{4\pi}{3}\right) \tag{A.3}$$

From (2.18), it is possible to obtain the equivalent model at the low-frequency side in each phase

$$v_{an}(t) = L_e \frac{di_a(t)}{dt} + v_{e,a}(t) \tag{A.4}$$

$$v_{bn}(t) = L_e \frac{di_b(t)}{dt} + v_{e,b}(t) \tag{A.5}$$

$$v_{cn}(t) = L_e \frac{di_c(t)}{dt} + v_{e,c}(t) \tag{A.6}$$

where, $v_{e,a}$, $v_{e,b}$, $v_{e,c}$ are the virtual voltages in each phase and i_a, i_b, i_c are the input currents in each phase.

The three-phase equation is calculated by

$$v_{abc}(t) = \frac{2}{3}\left(v_{an}(t) + v_{bn}(t)\, e^{-j\frac{2\pi}{3}} + v_{cn}(t)\, e^{-j\frac{4\pi}{3}}\right) \tag{A.7}$$

where, j is the imaginary unit and ω is the angular frequency in dq-frame

$$\omega = \frac{d\theta}{dt} \tag{A.8}$$

As described in Figure A.1b, placing the three-phase voltage v_{abc} in same direction of the direct axis phasor v_d and making the quadrature axis phasor v_q equal to zero, *i.e.*,

$$\begin{cases} v_d = |\vec{v}_{abc}| \\ v_q = 0 \end{cases} \tag{A.9}$$

From that, calculating the three-phase voltage phasor $\vec{v}_{abc}$

$$\vec{v}_{abc}(t) = L_e \frac{d\vec{\imath}_{abc}(t)}{dt} + j\,\omega\, L_e\, \vec{\imath}_{abc}(t) \tag{A.10}$$

where, $\vec{\imath}_{abc}$ is the three-phase current phasor.

Thus, calculating the grid voltage direct axis v_d and grid voltage quadrature axis v_q

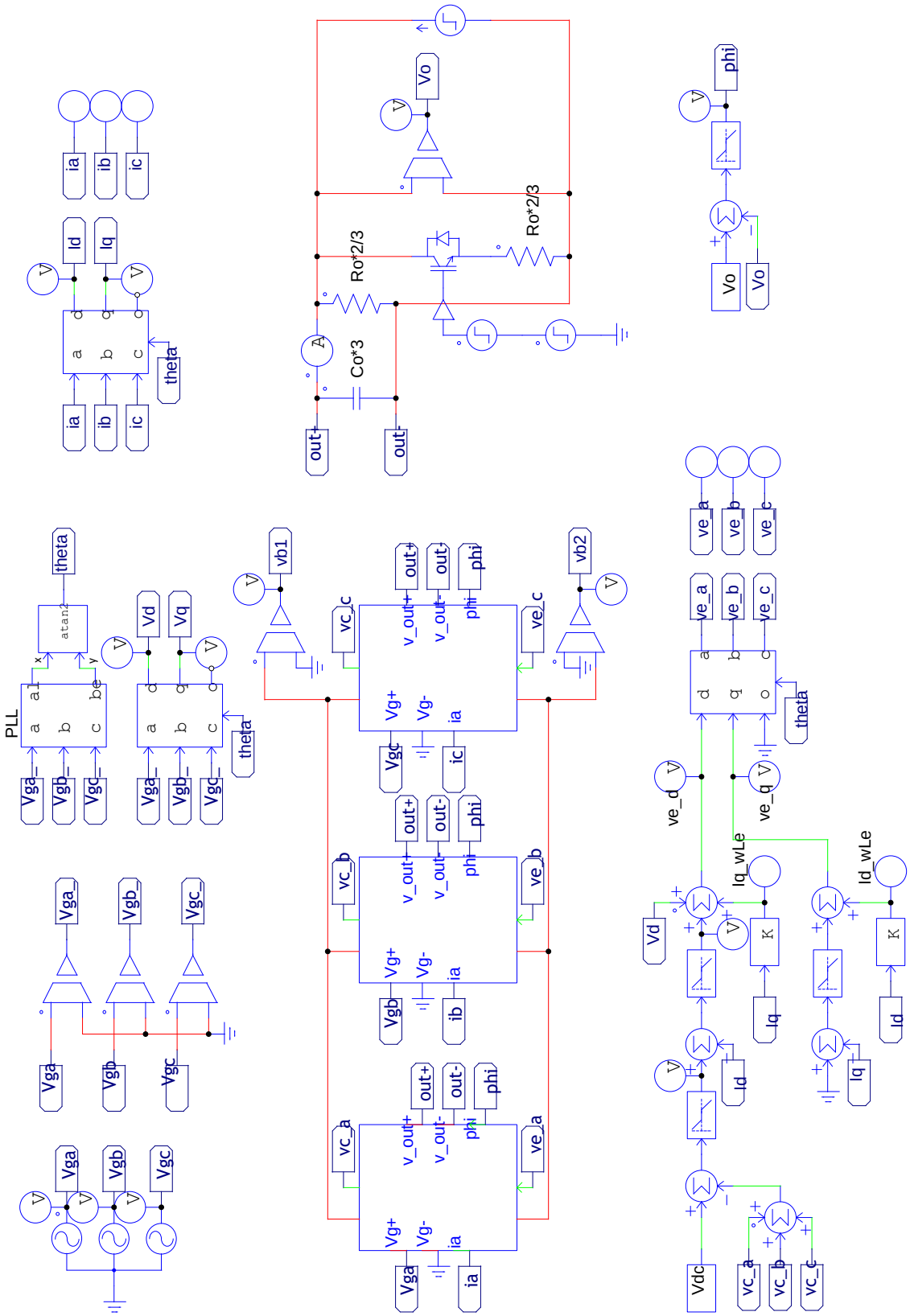
$$v_d(t) = L_e \frac{di_d(t)}{dt} - \omega\, L_e\, i_q(t) + v_{e,d} \tag{A.11}$$

$$v_q(t) = L_e \frac{di_q(t)}{dt} + \omega\, L_e\, i_d(t) + v_{e,q} \tag{A.12}$$

where $v_{e,d}$ and $v_{e,q}$ are, respectively, the direct axis and the quadrature axis of the virtual voltage v_e, i_d and i_q are, respectively, the direct axis and the quadrature axis of the input current.

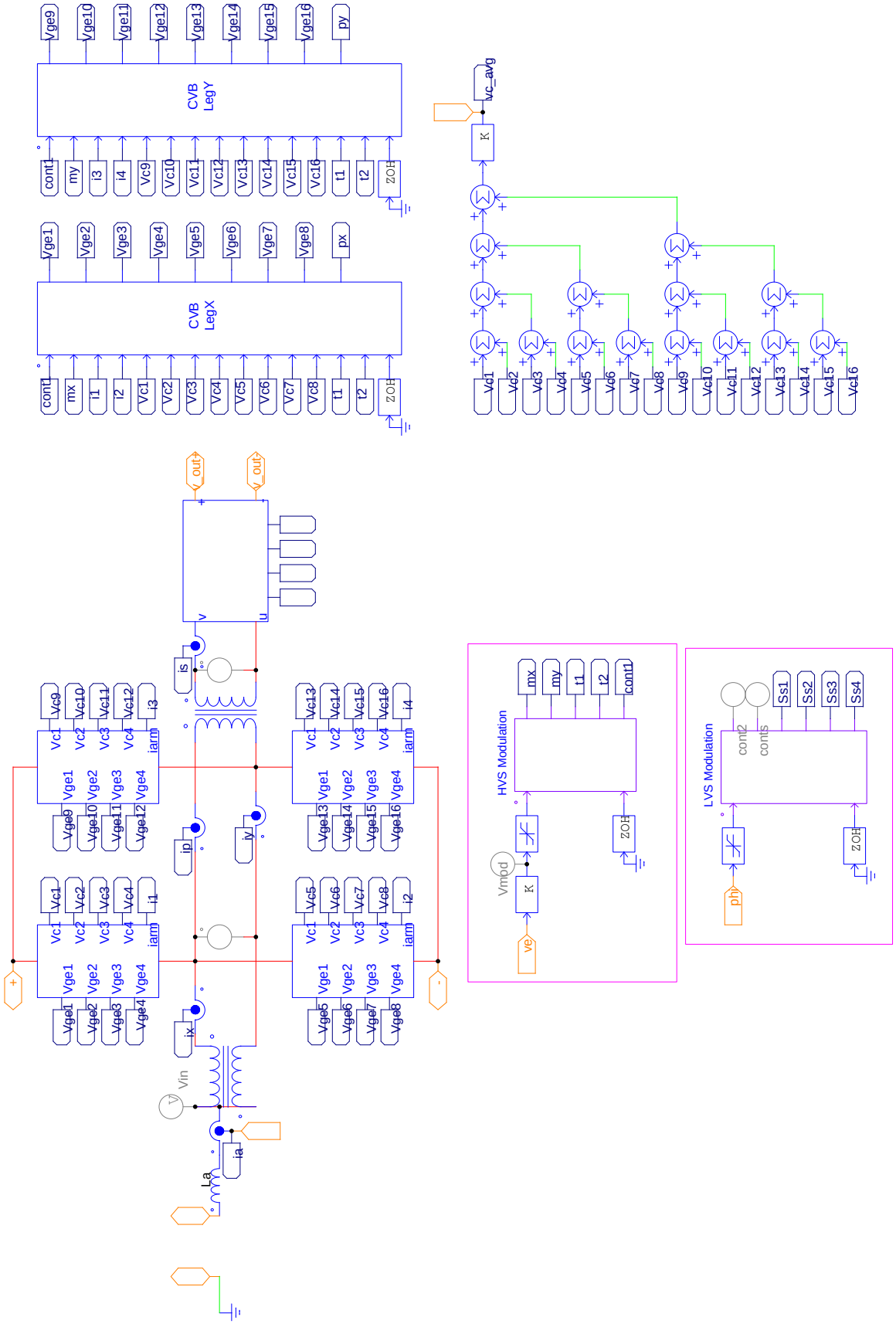
APPENDIX B – SIMULATION SCHEMATICS AND PARAMETERS

Figure B.1 – Three-phase AC-DC IMMC schematic circuit (simulation).



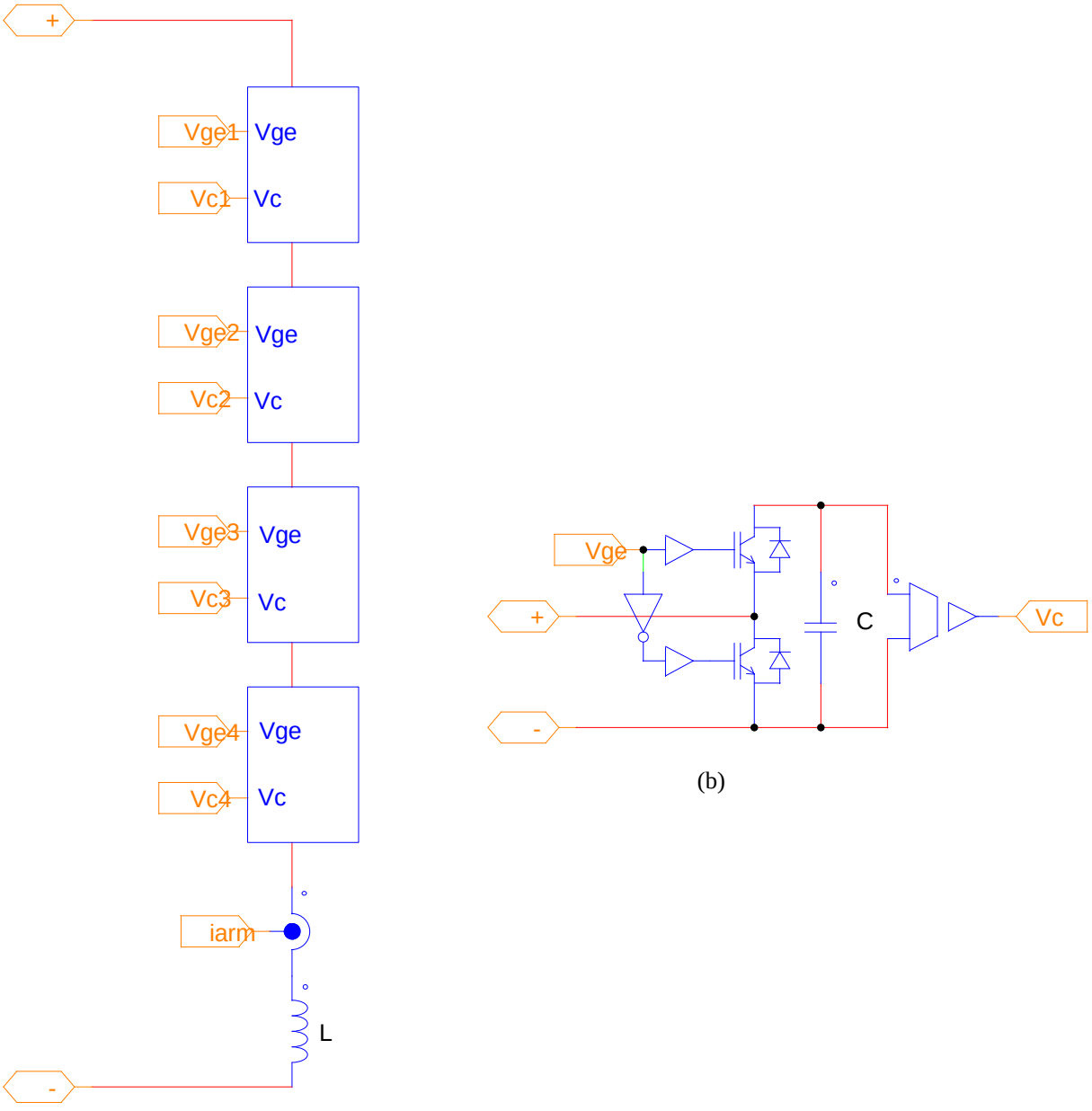
Source: author's right.

Figure B.2 – One phase schematic circuit of the AC-DC IMMC (simulation).



Source: author's right.

Figure B.3 – Schematic circuits: (a) one arm and (b) one submodule (simulation).



Source: author's right.

The simulation parameters are given as follows:

timestep=100n
fg = 60
me = 0.625
Po = 33.33k
pi = 3.1415
w=2*pi*fg

```
//Voltages
Vg = 7967
Vg_peak= 11268
Vg3 = 13.8k
Vbus =46k
Vdc = Vbus/4
Vc_in = Vdc
Vo = 380

//Currents
Io = Po/Vo

//Capacitors
Csm = 5.42u
Cbus=10.84u
Co = 1.15m

//Inductors
La = 8.38m
Li = 2.19m
Mi = 2.14m
L = 53.9m
Le = La+(Li-Mi)/2+L/4

//Submodules per arm
N = 4
Ron = 10m
Rd = 1m

// Load
Rg = 1904
Rt = 5281
```

```
Ro = 4.332

//Medium-frequency transformer
k=44.78
Np=k
Ns=1

//Input current control
iref = 5.9
Kp1 = 1375
Ti1 = 373u
Fp1 = 37321

//Capacitors voltage control
Kp2 = 19.66m
Ti2 = 298m
Fp2 = 46.6

//Output voltage control
Kp3 = 9
Ti3 = 2.94m
Fp3 = 4587
```