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DALTON DE ARAÚJO HONÓRIO

AN INTERLEAVED-STAGE AC-DC CONVERTER FEASIBLE FOR SST-BASED RAILWAY TRACTION SYSTEMS

FORTALEZA

2018

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Tese apresentada ao Programa de Pós-graduação em Engenharia Elétrica da Universidade Federal do Ceará, como requisito parcial à obtenção do título de Doutor em Engenharia Elétrica. Área de concentração: Sistema de Energia Elétrica.

Orientador: Prof. Dr. Luiz Henrique Silva Colado Barreto.
Coorientador: Prof. Dr. Demercil de Souza Oliveira Júnior.

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DALTON DE ARAÚJO HONÓRIO

AN INTERLEAVED-STAGE AC-DC CONVERTER FEASIBLE FOR SST-BASED RAILWAY TRACTION SYSTEMS

Thesis presented to the Doctoral Course in Electrical Engineering of the Electrical Engineering Department of Federal University of Ceará as part of the requirements for obtaining the title of Doctor of Philosophy (Ph.D.) in Electrical Engineering. Concentration Area: Electric Power Systems.

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EXAMINATION BOARD

_____

Prof. Dr. Luiz Henrique Silva Colado Barreto (Advisor)
Universidade Federal do Ceará (UFC)

_____

Prof. Dr. Demercil de Souza Oliveira Júnior (Co-advisor)
Universidade Federal do Ceará (UFC)

_____

Prof. Dr. Yales Rômulo de Novaes
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_____

Prof. Dr. Paulo Peixoto Praça
Universidade Federal do Ceará (UFC)

RESUMO

Esse trabalho propõe um conversor de potência com estágio intercalado CA-CC com características bidirecionais factível para aplicações de sistemas de ferrovia em média tensão. Ele é baseado em um arranjo que conecta os terminais de entrada em série e de os de saída em paralelo com módulos de potência idênticos. Existem dois tipos de módulos: o Tipo A consiste em dois braços intercalados empregando enrolamento acoplados de tal forma que seja possível a conexão de um transformador operando em média frequência, aliado a um célula dobradora de tensão, enquanto Tipo B também utiliza braços intercalados, contudo com um braço adicional operando na frequência da rede, substituindo a célula dobradora. A concepção da topologia é apresentada, seguida pela estratégia de controle adotada, bem como da modulação empregada. Uma estimação das perdas nos semicondutores é também discutida através de uma análise comparativa utilizando resultados de simulação, validando o desempenho superior da topologia proposta frente a soluções similares. Os resultados da topologia são obtidos através de testes experimentais em dois protótipos da topologia proposta considerando módulos do Tipo A. A estrutura de um único módulo demonstra as funcionalidades de comportamentos do conversor sobre as condições de regime permanente e transitórios, enquanto o protótipo com dois módulos demonstra as mesmas características em uma estrutura com múltiplos módulos. Com isso, é possível atestar o bom comportamento em termos de eficiência, mesmo o conversor proposto apresentando um número maior de componente magnéticos se comparado com soluções similares. Assim, a solução proposta é adequada para aplicações de alto níveis de potência em sistemas de acionamentos de máquinas de estágio CA-CC.

Palavras-chave: Transformador de estado sólido. Conversor modular bidirecional. Correção do fator de potência. Modulação vetorial.

ABSTRACT

This work proposes an interleaved-stage ac-dc bidirectional power converter topology feasible to medium-voltage (MV) railway systems. It is based on an arrangement that uses Input-Series-Output-Parallel (ISOP) configuration with identical power modules. There are two types of modules: Type A consists of two interleaved legs employing coupled-windings so that it is possible to connect a medium-frequency transformer (MFT), together with a voltage doubler cell, while Type B also uses the two interleaved legs, however with an additional one operating in the grid frequency in order to replace the voltage doubler cell. The topology conception is presented, followed by the adopted control and modulation technique. An estimation of semiconductor losses is also discussed through a comparative analysis by means of simulation results, validating the improved performance of the introduced approach if compared with similar solutions. The topology results are obtained through experimental test performed in two prototypes of the proposed topology, considering module type A. The single-module demonstrates the converter functionalities and performance under both steady-state and dynamic conditions, while the two-module structure demonstrates the same aspects for multi-module configurations. It is then possible to state that good performance in terms of efficiency even though the proposed power converter presents higher magnetic component count if compared with similar topology, thus making it suitable to high-power AC-DC machine drive applications.

Keywords: Solid state transformer. Modular directional converter. Power factor correction. Space vector modulation.

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1 INTRODUCTION

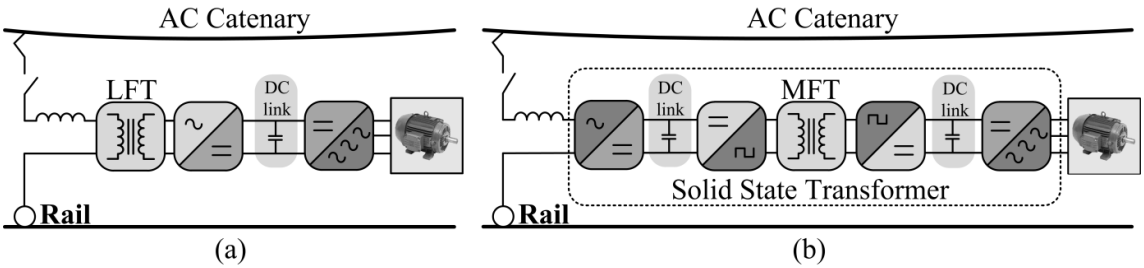
1.1 Thesis contextualization and motivation

Since its initial conception, the transformer has been used in the most diverse applications where insulation and adaptation of voltage levels are demanded. In fact, this device is widely employed either directly or indirectly in all electrical engineering fields due its simple design for distinct power and voltage conversion levels. In order to evidence how near this technology is from us, the reader, very likely, is using an electronic device with transformer in some part of its circuits to access this document, or it was used an electronic printer, which, also, applies transformer in some part of its inner electronics circuits, to obtain the paper based version of this document.

Transformers are the simplest magnetics circuits which can provide coupling with one or more electric circuits and their designs suffer minor changes as both power and voltage levels are varied. They are used in plenty kind of electric systems providing, impedance matching between the source and the load, filtering the dc current component on an ac power supply, and the aforementioned characteristics: galvanic insulation and voltage levels adaptation (1).

More specifically, the power transformer ensures such characteristics in power systems applications, such as: ac power energy transmission and distribution, as well as, medium-voltage machine drives. However, these applications are typically based on a bulky low-frequency device called Line Frequency Transformer (LFT) (2), as presented in Figure 1.1a.

Figure 1.1 – Power electronic converters used in traction applications: (a) Classical approach with LFT, (b) SST-based approach with MFT



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The size, weight and volume of these devices are closely related to the respective operating frequency, whose decrease causes the very augmentation of the magnetic (3). Moreover, if it is necessary to deal with power quality issues, such as voltages sags, flicker, harmonics and others, the inclusion of external devices are necessary to provide proper

protection, increasing the global volume of the transformer even further. Besides, many applications normally use oil inside the transformer for cooling and insulation purposes, what has direct impact on weight and volume and implies serious environmental issues (4). It is worth to mentioned, though, that in traction application normally the LFT are dry or oil less. On the other hand, the efficiency of the LFTs in this applications is low, since they are typically designed with high current densities (as less amount of copper is required) and efficiency range about (90-95)% (5). As a result, the use of the classical power transformer can become a limiter or even unfeasible in some applications such as traction and naval transportations (6).

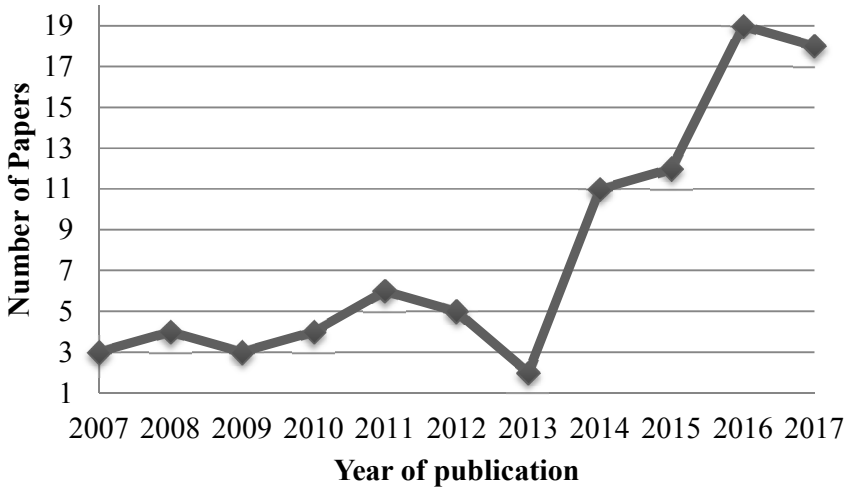
In order to address a lighter transformer for such applications, the first concept involving this matter is to replace the conventional bulky transformer operating at the line (catenary) frequency, which is usually lower than 100 Hz (7), by a solution using a transformer designed for an operating frequency around thousands of hertz. Such reduction is a must in medium-voltage machine drives, more particularly in electric railway application, since a more compact propulsion system is a requirement, resulting in the improvement of the transformer design and reduction of the requested power with the same cargo capability. This advantage is specially desired in Electric Multiple Units (EMU) where the propulsion system is distributed among the locomotive's cars (8).

Nowadays, with the power electronics development, trend applications accomplish such transformer replacement by applying power converter topologies with medium-frequency transformers (MFTs), these solutions are denominated as Solid State Transformer (SST), as presented in Figure 1.1b. Then, the classical LFT is no longer the only answer, when high-voltage, high-power capabilities are required in traction systems (9).

In fact, since the past decade both academic and the industry communities are spending research efforts in SST in the most diverse power electronic areas. Such interest can be note by looking the Figure 1.1, where it shown the SST-based railway systems publication statistic for the last decade. The focus of these studies are spread in several branches of railway traction applications, providing key concepts, new SST topologies, MFT analysis and design improvements, viability analysis of real scenarios and related subjects (10).

Hence, all the presented information and the recently attention around the SST applications (more specifically in traction systems) drive and motivate this PhD research and consequently this thesis.

Graph 1.1 – Number of scientific papers published by IEEE, related to SST-based railway traction application, in the last decade



SOURCE: Author's right.

1.2 Background of SST applied in traction systems

In order to allow for a better understanding about SSTs in railway traction systems and verify their potential in this application, it is necessary to know their basic concepts, aspects, requirements and compare them with the classical LTF approaches. Moreover, each SST solution can be sorted into a pre-established category, which helps either their historical presentation, as to note the evolution in the research lines of them. Hence, this chapter presents the SST technology focused in the aforementioned branches, as well as, its state-of-the-art in railway traction systems.

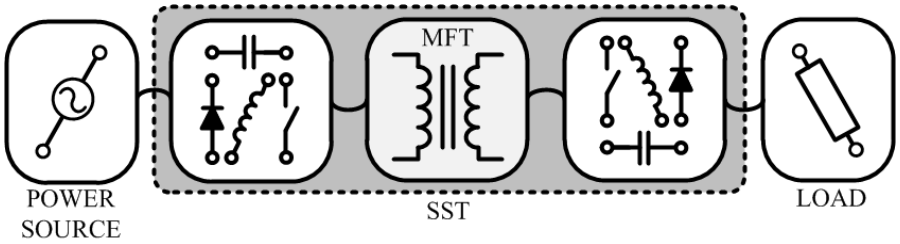
1.2.1 SSTs concepts and classification

As mentioned before, one possible solution to replace the LFT in power systems is to apply MFT together with power electronics structures. The general goal of the SST is to adapt the high-voltage level, in the targeted power application, for medium- or low-voltage levels, increasing dramatically its compatibility. Figure 1.2 presents a generic configuration of the SST concept.

It is possible to note from Figure 1.2 that the voltage level in the power source is used by the first power converter in order to modulate a voltage with medium frequency spectrum in the terminals of the MFT. Next, such modulated voltage is stepped-down by the

MFT's turns ratio, and then it is used by the second power converter to be adapted for a more feasible one, depending on the targeted application.

Figure 1.2 – Generic SST configuration



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The SST features can be summarized as follow.

- The transformer operates at a medium frequency, from hundreds Hertz to kilohertz;
- It is necessary application of power electronics converters, to provide medium frequency operation;
- High-voltage power devices are used in the input terminals due the grid (catenary) characteristics.
- The voltage in the MFT nominally is not sinusoidal, due the power switching structures.

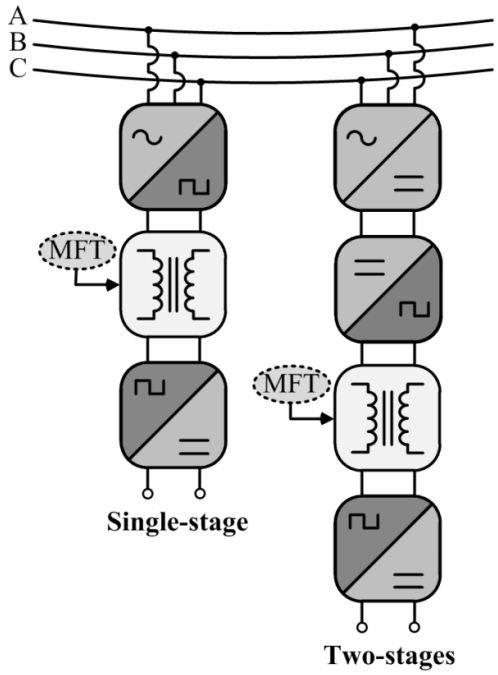
The SST application creates a large number of possibilities to be explored, since a large number of power converters can be adapted or even conceived for this matter. Then, some SST classifications are demanded to sort the solutions which already exist and those which will be considered in future.

In (11), it is presented a classification in terms of power conversion stages in the SST topologies, focusing on power distribution systems. In the studies elaborated by (12) and (13), it is presented a similar classification together with other one in terms of the MFT windings configuration. Kolar and Ortiz (14) show three different forms to categorize SSTs. The first one sees the SSTs in terms of how the structure provides the power flow, while the second one is concerned in the configuration used by the SST to link three-phase systems, which is similar with the one presented by (11). At last, the third classification is focused on how the SST is supposed to connect the high-voltage grid terminals, being comparable with the one presented in (12).

In this thesis, the SST solutions will be presented considering the power conversion stages category and assuming that they must provide a dc link voltage to the machine drive

systems. Therefore, it is possible to briefly classify the main characteristics of the SST topologies in two different categories, as presented in Figure 1.3.

Figure 1.3 – SSTs power stage categorization



SOURCE: Author's right.

The definitions of the conversion stages considered in this thesis is presented as follow.

- **single-stage approaches (ac-dc):** This solution usually uses bidirectional switches to create a high-voltage connection capability at its input terminals with an isolated medium frequency link without a dc link in the primary side of the MFT. It provides a dc voltage to the locomotive's drive machine systems in the secondary side of the MFT.

To aggregate such high-voltage connection capability without the presence of a medium-voltage dc link, some works propose cycloconverters combined with a voltage-source active rectifier (15) or with bidirectional converters structures (16). A general cycloconverter consisting of individual modules is proposed in (17) to decrease the power levels associated to MFTs. However, there is appreciable reactive content through the transformer due to the low-frequency envelop of the voltage waveform across the primary side of the transformer.

- **two-stages approaches (ac-dc/dc-dc)**: Such topologies also allow high-voltage input connection, but the additional conversion stage brings more flexibility to the whole structure. The isolated medium-frequency is commonly placed at the

dc-dc stage, since the isolated dc-dc stage is a well-known power electronic structures.

The work presented in (18) uses a cascaded high-voltage rectifier whose input voltage is rated at 7.2 kV, as well as a dual active bridge converter responsible for isolation and voltage step down from 3.8 kV to 400 V. Thus, the ac-dc converter is able to perform power factor correction, while the dc-dc stage is decoupled from the dc link (in the control aspect) and the design of the DAB converter can be optimized for a wide soft switching range. A similar topology is used in (19), but a different arrangement is proposed for the MFT, allowing multiport connections and consequently, flexibility for both EMU trains and locomotives machine drivers. The multiport connection in (20) is also used, but for power management purposes, since ports with different characteristics i.e. distributions systems, low-voltage dc storage plants, medium-voltage ac machine driver, among others are connected to provide a versatile and flexible power system.

Besides these categories, it is possible to find SST solutions which integrate two conversion stages. They use dc links to modulate the voltage across the primary side of the MFT without using an isolated dc-dc stage. In other words, the same semiconductor structure provides the dc link and the ac voltage across the MFT, instead of employing an H-bridge used as an ac-dc stage and another dc-ac one. Although such topologies could be considered as a middle term between the aforementioned categories, this work is supposed to treat them as a single-stage approach. An example for this kind of structure is the modular multilevel converter called M^2LC presented in (21), which uses cascaded full bridge converters in an H-bridge arrangement i.e. a set of cascaded converters form the upper and the lower arms of the structures' legs. Hence, medium-frequency isolation can be achieved without using an additional dc-dc isolated stage and high efficiency is achieved with high power density.

1.2.2 Requirements and aspects of a railway traction system

The evolution of railway traction systems is instigated by market requirements, which can be summarized by seven topics: 1) smart cargo capability use, 2) low floor accessing, 3) reliability, 4) operating life time, 5) minimized preventive maintenance, 6) motor technology improvement and 7) cost reduction on active components (22). In other words, the traction system should be attractive as much as individual transportation (cars, motorcycles, bicycles and etc.) over short distances and aircraft over long distances. To accomplish that, the on board power consumption of the trains shall increase, since air conditioning, automatic access, lights,

personal electronics devices and electronics charging stations, are becoming common in this applications (23).

Although traction systems are supposed to increase the passenger comfort, the real improvement should come from technology breakthrough in the components, more specifically in active power components (24) in the main electric power system. Then, to address the aforementioned requirements, the railway traction system should have the following aspects.

High efficiency: increment of the auxiliary power (on board consumption) with a slight addition of the total demanded power.

High power density: low weight in an elevated power level structure.

Reliability and reduced maintenance: constant improvement of the mean time before failure (MTBF) index.

High-voltage singe-phase capabilities: since the typically single-phase railway AC lines are 15 kV at 16⅔ Hz and 25 kV at 50 Hz (5), the SST solution should deal with these magnitudes.

1.2.3 Comparison between SST-based and classical LFT-based solutions

With the information presented so far about LFT-based and SST-based railway traction systems, it is possible to provide a comparison analysis between both approaches.

Besides the volume, weight and material cost reductions of the transformer in SST-based applications due the medium frequency operation, it is possible to highlight some other advantages, like the possibility to improve the transformer's efficiency, reducing its winding and core losses, which is very hard to be accomplished in the LFTs due the innate high voltage and low frequency operational levels.

Other characteristic of the MFTs is the possibility to provide functionalities that are impossible to obtain with classical LFTs, without the inclusion of external devices. The conversion of the power-stage by power converters allows the improvement of power quality, through the power factor control, harmonics mitigations and satisfactory response under transients. Moreover, if current and voltage are controlled separately, it is possible to provide power flow control and voltage disturbance compensation (sags/flickers/swell), as additional functionalities.

On the other hand, LFT-based applications uses medium- or low-voltage power devices, as the LFT steps down the catenary voltage. Similar behavior does not occur in the SST applications since active front-end converters interface the catenary and the MFT, requiring expensive and high-voltages power devices. Moreover, the MFT designs usually use

advanced cores materials in order to achieve high efficiency levels in medium frequencies applications, increasing the cost even further. However, the cost can be compensated by the additional functionalities and improvement of either the power quality and system efficiency.

Reliability of SST-based applications should also be considered, since it tends to decrease if directly compared with LFT-based ones. In fact, the larger number of power semiconductor devices required to deal with high-voltages levels together with the complexity of the power converter structures explain such behavior. Although the SST reliability can be improved by applying redundant designs, they also increase the cost, resulting in complex design criteria. Thus, the SST-based systems are more complicated and difficult to be conceived, mostly due the number of control variables and the degree of freedom used to obtain the proper structure controllability being well greater if compared with LFT-based systems.

Table 1.1 shows the summarization of the aspects compared in SST-based application over the ones in LFT-based systems, by categorizing them as pros and cons.

Table 1.1 – Comparison between SST-based and LFT-based applications

PROS	CONS
Greatly reduced transformer volume and weight	High input voltage for front end converter
Higher transformer and system efficiency	Higher system cost
Better power quality	Reduced reliability
Additional functionalities	Difficult to design and manufacture

SOURCE: Adapted from (25).

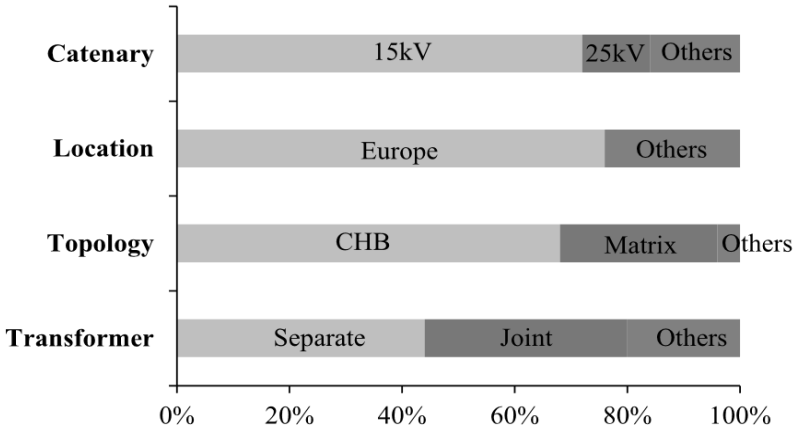
1.2.4 State-of-the-art of SST-based railway traction solutions

There are several works which present review studies and discussion in general aspects around SST, potential applications, topologies, power devices requirements, among others. Examples of such studies can be found in (13), (26), (27), (28) and (29). However, since each application of SST brings different particularities to the project, it is better to concentrate the attention in review studies focusing on railway traction systems, like the ones presented by (30) and (31). The study in (30) presents soft switching techniques applied in SST to improve the systems efficiency, while (31) presents the evolution of the individual parts of the railway traction systems, such as: power devices, transformers, drive motor systems. In (23), a deep discussion is elaborated about the MFT and six selected SST types are analyzed in the study presented by (5).

The analysis presented in (25) focus their reviews in the SST-solutions presented by both academic and industry communities. They start in the earliest concepts till the newest ones presented at the time, elaborating a series of statistic results with all the collected information.

For instance, Figure 1.4 gives the idea of how the interest in this field is mainly concentrated. It is possible to note that SST topologies for 15 kV input voltage level with cascaded structures to obtain the active front-end converter and separated MFTs processing a portion of the whole power are preferred.

Figure 1.4 – Publication statistic of SST-based railway traction application



SOURCE: Adapted from (25).

By analyzing proposed solutions in the scientific community, it is possible to find studies lying in transformerless topologies, which are independent on transformer and based on a medium-voltage rectifier stage (32). This possibility always is limited by the semiconductor blocking-voltage capability. However, Modular Multilevel Converters (MMC) (33) has recently raised the interest in such solution due its high blocking voltage, modularity, and very high power quality. Two structures based on MMCs for transformerless traction applications are presented in (34) using either dc links or single-stage approaches. The work in (35) employs energy storage systems integrated to a MMC to recovery the kinetic energy during the braking operation using the bidirectional converter characteristic. The bidirectionality has become handy in traction applications in order to increase the efficiency of the whole vehicle electrical system.

Galvanic isolation is welcome in traction application, since increases the systems reliability. In fact, it is a strong tendency, as the majority of the newest studies are based on it. Differing of transformeless approaches, these solutions must provide power converter structures with isolated medium frequency. The study presented in (36), where an interphase

transformer is used to achieve a three-phase interleaved MMC structure, is an example of these power converters. Following the same idea, the study in (37) applies the same interleaving technique to a single-phase, single-leg MMC structure, obtaining a low output voltage. The study in (9), also, applies the same interleaving technique, but in a cascaded modular multilevel converter.

In (38), the author focused in a resonant power converter structure in active front-end half-bridge rectifier in the primary side of the MFT, while the secondary side has a naturally commutated rectifier. The converter topology is conceived for dual 3.3 kV and 600 V dc fed tram-train transportation systems with a 120 kW 64 Kg nanocrystalline cored toroidal transformer, 95% of efficiency operational rating, 1.84 to 2.7 kHz.

The study presented in (39) presents input-series-output-parallel (ISOP) power converter with separated flyback transformers. The front end converter charges its respective flyback inductor, while the secondary is not active. Next, the secondary actives in a proper sequence to allow the stored energy dumped into the output capacitor, at the secondary side. There is some aspect that should be carefully handled in this approach. For example, the current in the flyback should always be in the same direction, to guarantee that, the authors use switches with unidirectional current behavior (IGBT in series with diode). Besides, the flyback transformer design should be identical, otherwise unequal voltage sharing will occur among the converter modules.

The study presented by (40) is related to classical multilevel power converter in modular structures. Each module is built with diode-clamped three-level structure for the ac-dc and isolated dc-dc stages. (41), also, presents a traction solution with diode-clamped three-level structure, but in a four quadrant structure, improving the flexibility of the system.

Other classical multilevel structure used in railway traction application is the cascaded H-bridge (CHB) converter. An isolated front end ac-dc SST in presented by (42), the proposed converter is built with SiC-based devices, resulting in maximum efficiency of 97.5% at 1.5 kW. The study presented in (43) shows a 7-level hybrid CHB with asymmetrical configuration obtaining high power quality with reduced number of modules.

It is possible to note that cascaded-based structures designs reach higher voltage and power levels than others solutions, assuming a same power switches capabilities, besides their more mature stage in traction application (44). Such fact, explain the preference pointed out by Figure 1.4.

1.3 Objectives and expected contributions

The interest of applying the solid state transformer in traction systems was introduced in the last sections. It is possible to note that this new technology can be treated as a game change in this field, since there are plenty of possibilities to provide solutions customized with the final goal of the application. Once the primary goal (reduce the use of raw material like copper) is guaranteed, the engineer can focus in others requirements of the application. For instance, high-voltage terminals capability is welcome in traction systems.

In fact, the designer can conceive his solution paying attention in a large number of characteristics, such as: MFT structure (one transformer or several ones), the number of power conversion stages used in the SST, the power converter topology applied in each stage, the requested semiconductor characteristics, among others.

The principal purpose of this thesis is to present, design and implement a SST topology feasible for traction systems, employing a new power converter topology with interleaved, modular, bidirectional and multilevel characteristics. The theoretical analysis of the proposed topology is carried out, as well as a simulation model, in order to obtain a better understanding of the topology's aspects, requirements and behaviors on operation. The applied control techniques and the modulation adopted will also be investigated. To set up the prototype, a down-scale model was built and the design of its parts will be addressed (capacitors, magnetics, semiconductors, printed circuit boards, etc.).

In the targeted application, some particularity is required. Hence, the proposed topology is expected to provide the possibility to deal with high-voltage and high-power levels, medium-frequency insulation and good efficiency. Although, such requirements turn the idea a big challenge, the proposed SST is expected to address them using the same power converter module. Then, it is possible, just calculating the number of modules requested by the application, to conceive the entire SST structure. The insulation and magnetics weight/volume reduction are delivered by the use of MFTs in each power module, as well as, the efficiency is improved by an interleaving technique, reducing the current effort in the semiconductors.

1.4 Thesis outline

The contents of this thesis are organized as follows:

- In the first chapter, the background of solid state transformer for railway traction applications is presented: requirements, aspects, basics concepts, classifications, as well as a comparison with low frequency transformer. It is,

also, presented an overview of the state-of-the-art of the application, besides the thesis motivation, objectives, contextualization and expected results.

- Chapter 2 gives the qualitative and quantitative analysis of the proposed converter. In the qualitative analysis are presented the converter structure with its possible arrangements, the modulations techniques and the control strategies applied, as well as, its theoretical functionalities. In the quantitative study is presented the modeling of the converter, addressing the magnetics values as well as a comparative losses analysis in a real scenario parameters for railway traction systems.
- Chapter 3 shows the design methodology and procedures of the controller applied in the control loop of the proposed converter.
- Chapter 4 presents the simulation and experimental of the proposed converter, considering a single- and multi-module arrangement. It is presented behavior of the control loop for both steady-state and dynamics test.
- Chapter 5 provides the conclusion of the thesis. The possible future analyzes of the doctoral study are presented, followed by the scientific production achieved during the PhD period.

2 PROPOSED TOPOLOGY

Once the SST role in the railway traction systems was demonstrated in the last chapter, it is possible to present properly the proposed converter. In this chapter, the qualitative and quantitative analysis of the proposed converter is presented as follows.

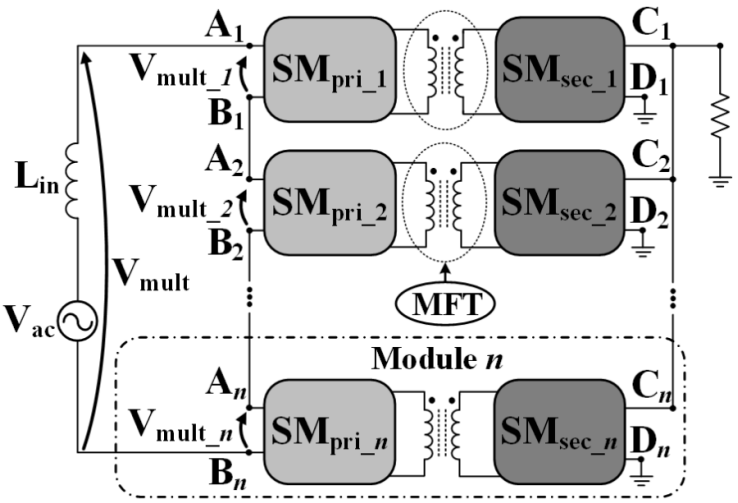
2.1 Qualitative analysis

The following sections are concerned about the conception, operation and technique applied in the proposed converter structure, for both modulation and control proposes.

2.1.1 Conception

The proposed power structure is a single-stage ac-dc modular cascaded multilevel (MCM) bidirectional converter. As presented in the last sections, cascaded structures fit quite well for high-voltage requirement. Therefore, a modular characteristic brings more versatility for the whole structure. In fact, it is possible to scale-up or -down the converter withstands voltage level by a convenient arrangement of its identically power module structures. Then, the generalized structure for a generic number of modules *n* is presented in Figure 2.1.

Figure 2.1 – Generalized structure of the proposed topology



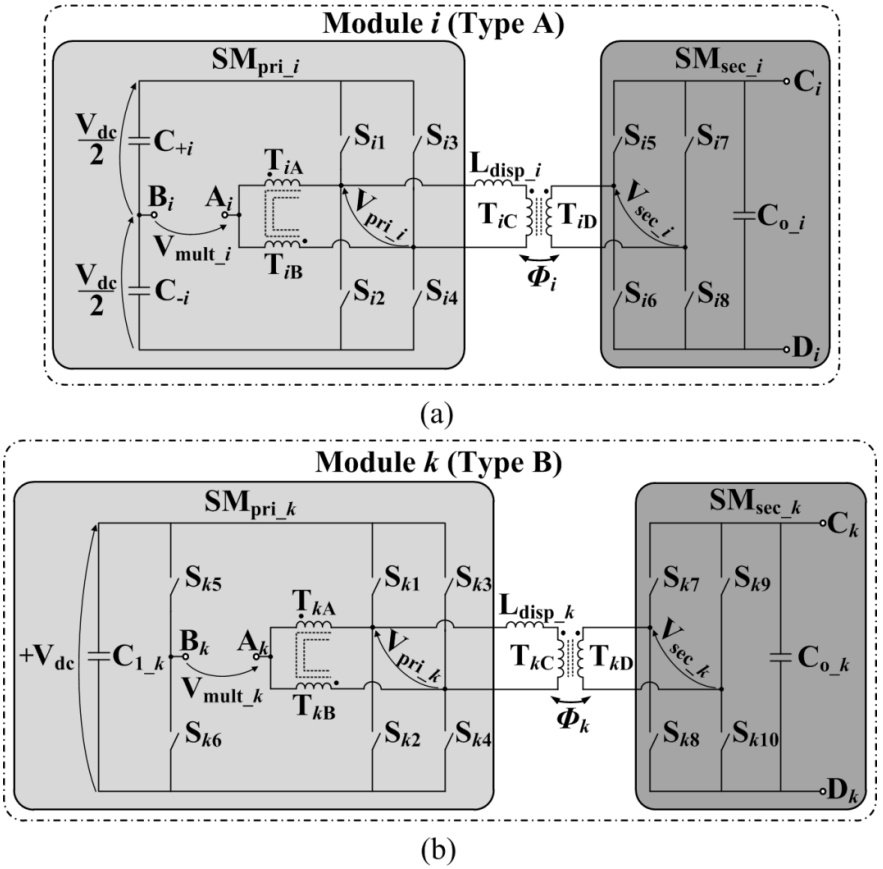
SOURCE: Author's right.

The proposed converter uses the concepts of cascaded multilevel structures in an input-series-output-parallel (ISOP) configuration. The ISOP arrangement allows the converter to deal with high-voltages levels in the input terminals, as well as, decrease the harmonic content of the multilevel voltage minimizing the input filter, L_{in}.

Moreover, the medium frequency isolation is accomplished by the MFT placed in each power module of the structure, where its primary and secondary voltages are phase-shifted by Φ_i. Therefore, the single-stage ac-dc is responsible for modulating a multilevel voltage to the input filter, while it provides a three-voltage level to the MFT in each module, as well.

The inner circuit of the power modules is presented in Figure 2.2. The proposed topology can be built separately with two different modules structures: Type A or Type B.

Figure 2.2 – The inner configuration of the module: (a) power module type A, (b) power module type B



SOURCE: Author's right.

Both power modules share, basically, the same configuration. They use two submodules arrangements, one in the primary side of the MFT ($SM_{pri\_i(k)}$) and other ($SM_{sec\_i(k)}$) in the secondary side. The generic submodule $SM_{sec\_i(k)}$ is the same for both module and its terminals $C_{i(k)}$ and $D_{i(k)}$ are connected in parallel. The MFT interfaces the submodules connecting the h-bridge structures conceived by the switches (S_{i1}, S_{i2}, S_{i3}, S_{i4}) and (S_{i5}, Si_6, S_{i7}, S_{i8}) for type A and (S_{k1}, S_{k2}, S_{k3}, S_{k4}) and (S_{k7}, S_{k8}, S_{k9}, S_{k10}) for type B. The modulation strategies requirements for this semiconductors will be addressed in section 2.1.3.

The submodule ($SM_{pri\_i(k)}$) applies interleaved coupled windings (i.e. an autotransformer configuration) to share the input current equally in both windings ($T_{i(k)}$A and $T_{i(k)}$B), providing good distribution of losses among the semiconductors and minimization of the harmonic content for current waveforms. Interleaving using an autotransformer was introduced in (45), whose benefits have been deeply analyzed in (46), where a reduction in the total magnetics volume has been proved.

The main difference between the modules remains in the $SM_{pri\_i(k)}$, where in type A (Figure 2.2a), its respective configuration can be seen as the combination of interleaved coupled windings (45) and the dual active bridge (DAB) topology (47) added to a dc link with a central point (capacitors C_{+i} and C_{-i}), while in type B, the dc link with central point is replaced by a low-frequency switched arm, (S_{k5}, S_{k6}) and a regular dc link, as can be seen in Figure 2.2b.

The minimum number of modules requested for the proposed converter using submoludes type A, $n_{min(A)}$, is described by:

$$n_{min(A)} \geq \left\lceil \frac{2 \times V_{peak}}{V_{dc\_min\_A}} \right\rceil, \tag{2.1}$$

where $V_{dc\_min\_A}$ is the minimum value of the average voltage sum across capacitors C_{+i} and C_{-i} and V_{peak} is the peak value of the ac input voltage.

And, using submoludes type B, $n_{min(B)}$, is described by:

$$n_{min(B)} \geq \left\lceil \frac{V_{peak}}{V_{dc\_min\_B}} \right\rceil, \tag{2.2}$$

where $V_{dc\_min\_B}$ is the minimum average voltage across capacitors C_{1_k} and V_{peak} is still the maximum input voltage.

Thus, the number of modules requested by the applications parameters are obtained by (2.1) and (2.2), making the specifications of the proposed converter done easily compared with other structure applied in the same conditions.

2.1.2 Operation

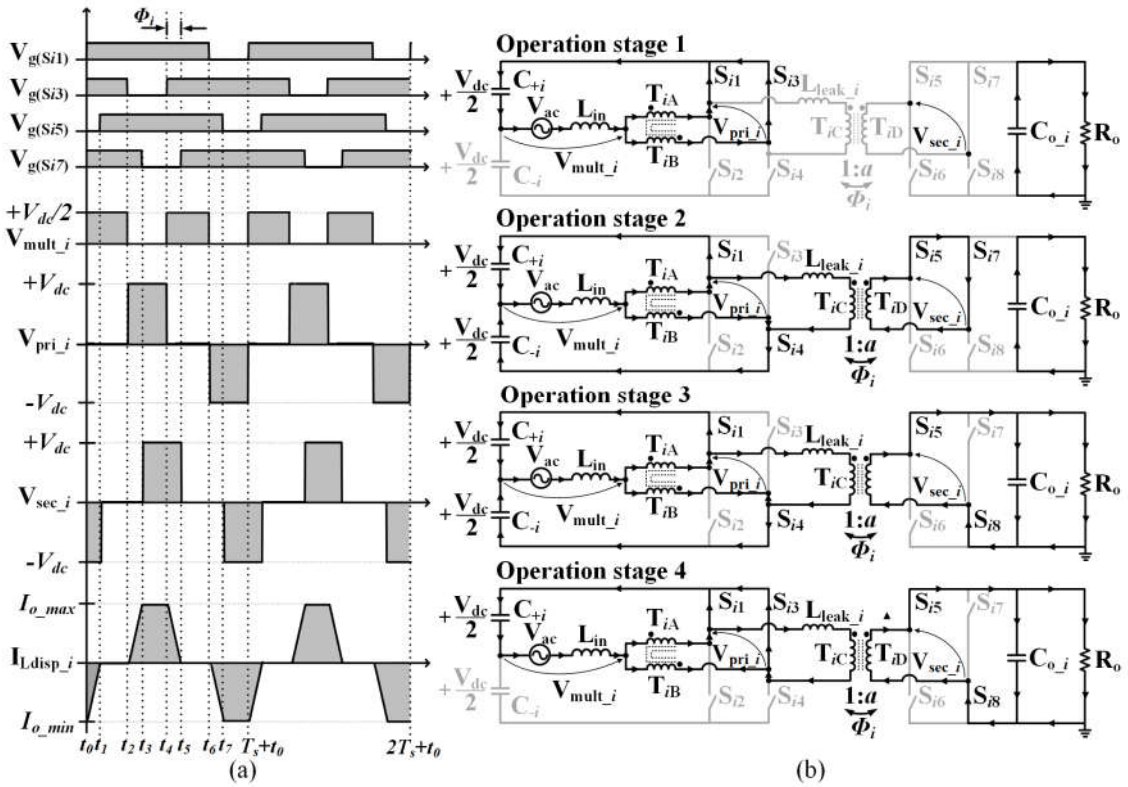
The operating principle of the basic modules is presented in this subsection in order to exemplify the whole converter behavior. Therefore, the equivalent circuits can be divided into eight intervals for one switching cycle for each module type. Figure 2.2a presents the main theoretical waveforms used to exemplify the operation in the type A, while the ones regarding the type B are presented in Figure 2.4a.

The graph representations of some key intervals are presented in Figure 2.3b for type A and Figure 2.4b for type B. Others intervals graph representation can be seen in (48), only considering the primary side switching cases in type A and B, respectively.

2.1.2.1 Type A

It is worth to mention that capacitor C_{o_i} is considered as charged in the previous switching cycle with the same voltage level of the dc link at the primary side of the MFT and L_{in} is much greater than L_{leak_i}. Besides, the pairs of switches (S_{i1}, S_{i2}), (S_{i3}, S_{i4}), (S_{i5}, S_{i6}) and (S_{i7}, S_{i8}) operate complementarily. $V_{g(Si1)}$, $V_{g(Si3)}$, $V_{g(Si5)}$, and $V_{g(Si7)}$ are not defined in the Figure 2.2a, so they are defined here as the gating signals applied to switches S_{i1}, S_{i3}, S_{i5} and S_{i7}, respectively; V_{mult_i} is the input voltage; V_{pri_i} is the primary voltage across the MFT; V_{sec_i} is the secondary voltage in the MFT; I_{leak_i} is the current through the leakage inductance, L_{leak_i}; Φ_i is the phase-shift angle between V_{pri_i} and V_{sec_i}. All parameters are valid for a generic module i.

Figure 2.3 – Type A operational aspects: (a) main theoretical waveforms during a switching period, (b) Operation stages



SOURCE: Author's right.

The variables behaviors during the intervals represented by Figure 2.3b are described as follow:

Operation 1 [t_1, t_2]: Initially, S_{i1} and S_{i3} are turned on, causing V_{mult_i} to equal V_{C+i}, i.e. $+V_{dc}/2$ V; V_{pri_i}=0, since the interleaved coupled windings are short-circuited. In the secondary side, S_{i5} and S_{i7} are on, but with no current circulation and, V_{sec_i}=0, since the winding T_{iD} is, also, short-circuited. The leakage inductance voltage and current are null.

Operation 2 [t_2, t_3]: It begins when switch S_{i4} is turned on and S_{i3} is turned off, implying V_{mult_i} =0, since the voltages across T_{iA} and T_{iB} windings have opposite polarity; V_{pri_i} equals $+V_{dc}$, because it is directly connecting to capacitor C_{+i} and capacitor C_{-i}; In the secondary side, the conditions are the same as those for operation 1 since the secondary switching states are maintained. Current I_{leak_i} starts increasing since its respective voltage is $+V_{dc}$.

Operation 3 [t_3, t_4]: Since the primary switching condition is the same as those for operation 2, the behavior of V_{mult_i}, V_{pri_i}, remains the same. When S_{i5} is turned on and S_{i7} is turned off, $V_{sec\_i} = +V_{Co\_i}$ i.e. $V_{sec\_i} = +V_{dc}$, while I_{leak_i} remains constant at its peak value.

Operation 4 [t_4, t_5]: During this case, switches S_{i1} and S_{i3} are turned on, resulting in a similar operation analysis like 1, i.e. V_{mult_i}=$+V_{dc}/2$, and V_{pri_i}=0. In the secondary side, switches S_{i5} and S_{i8} are on, as V_{sec_i}= $+V_{dc}$ and current I_{leak_i} decreases.

Due to the inherent symmetry of the circuit, only the operation regarding the positive half-cycle of the input current is described, although the behavior of V_{mult_i} is analogous, assuming negative values when switches S_{i1} and S_{i3} are off simultaneously. Besides, the interval [t_5, T_s+t_0+t_1] has, also, symmetric behavior of the interval [t_1, t_5].

2.1.2.2 Type B

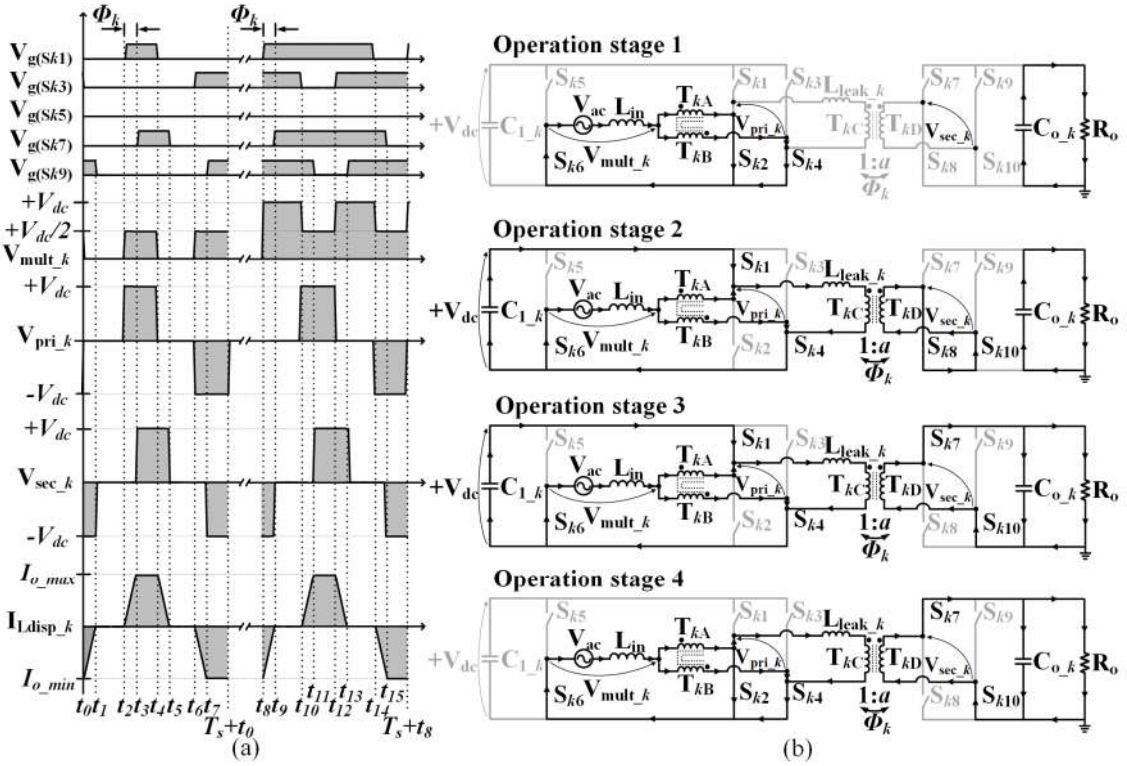
Assuming the same characteristics of the type A, it is possible to define the parameters for the analysis of type B. Similarly, $V_{g(Sk1)}$, $V_{g(Sk3)}$, $V_{g(Sk5)}$, $V_{g(Sk7)}$ and $V_{g(Sk9)}$ are the gating signals applied to switches S_{k1}, S_{k3}, S_{k5}, S_{k7} and S_{k9} and Φ_k is the phase-shift angle between V_{pri_k} and V_{sec_k}, respectively.

The switch pairs (S_{k1}, S_{k2}), (S_{k3}, S_{k4}), (S_{k7}, S_{k8}) and (S_{k9}, S_{k10}) have high-frequency operation, while the switch pair (S_{k5}, S_{k6}) has low-frequency one, as mentioned in section 2.1. All the switch pairs are supposed to operate complementarily.

Figure 2.4a presents two different regions of operation, region I [t_0, T_s+t_0] and region II, [t_8, T_s+t_8], while the graph representations of some key intervals are shown in Figure 2.4b. Hence, the variables behaviors during the intervals are described as follow, for region I firstly:

Operation 1 [t_1, t_2]: This stage begins when S_{k1}, S_{k3} and S_{k5} are turned off, causing V_{mult_k}=0 V, since the voltages across T_{kA} and T_{kB} windings have opposite polarity; V_{pri_k}=0, because the interleaved coupled windings are short-circuited. In the secondary side, S_{k7} and S_{k9} are on, but with no current circulation and, V_{sec_k}=0, since the winding T_{kD} is, also, short-circuited. The leakage inductance voltage and current are null.

Figure 2.4 – Type B operational aspects: (a) main theoretical waveforms during a switching period, (b) Operation stages



SOURCE: Author's right.

Operation 2 [t_2, t_3]: In such stage, the switch S_{k1} is turned on, while S_{k3} and S_{k5} are turned off, implying V_{mult_k} to equal $+V_{dc}$/2 V, since the voltage across capacitor C_{1_k} is shared by V_{mult_k} and the interleaved coupled winding; V_{pri_k}=$+V_{dc}$, because it is directly connecting to capacitor C_{1_k}; In the secondary side, the conditions are the same as those for operation 1 since the secondary switching states are maintained. Current I_{leak_k} starts increasing since its respective voltage is $+V_{dc}$.

Operation 3 [t_3, t_4]: The primary switching condition is the same as those for operation 2, then the behavior of V_{mult_k}, V_{pri_k}, remains the same. On the other hand, S_{k7} is turned on and S_{k9} is turned off, at the secondary side, implying V_{sec_k} = $+V_{Co\_k}$, i.e. V_{sec_k} = $+V_o$. The leakage inductance voltage is null and the current remains constant at its peak value.

Operation 4 [t_4, t_5]: Finally, when switches S_{k1}, S_{k3} and S_{k5} are turned off, once again, resulting in a similar analysis as operation stage 1 i.e. V_{mult_k}=0, and V_{pri_k}=0. The switching conditions for the secondary side remain the same as the previous stage. Then, V_{sec_k}= $+V_{dc}$ and the current in L_{leak_k} decreases, as the leakage inductance voltage is $-V_{dc}$.

For the same reasons pointed out in the last subsection, it is possible to omit the behavior of the converter considering the negative half-cycle of the input current and the symmetric intervals [t_5, T_s+t_0]∪[t_0, t_1] and [t_1, t_5].

The behavior of region II can be understood from the stages described above and from Figure 2.4a, more particularly, the interval [t_8, T_s+t_8]. It is possible to note that the voltages and currents of the MFT remains the same regardless the operating region, however the multilevel voltage V_{mult_k} presents different value according with the respective region.

In fact, when V_{mult_k} is null in region I, the leakage current is always null at end of its interval. To obtain the same behavior in region II, it is possible to use a redundant operational stage which results in V_{mult_k} equals to $+V_{dc}$, considering the positive input current half-cycle. Moreover, when value different from zero are necessary for V_{pri_k}, it is possible to use others redundant operational stages which results in V_{pri_k} equals to $+V_{dc}/2$ or $-V_{dc}/2$.

Then, the behavior of the variables in the MFT are preserved as those in region I, while a V_{mult_k} has an addition of $|V_{dc}/2|$ in magnitude. The implication of such behavior in the V_{mult_k} will be addressed in the next subsection.

2.1.3 Modulation technique

It was possible to note in last subsection, that the type A module presented operation stages which provide three-level voltage in the V_{mult_i}, while type B can be operated modulating until five-levels (Region I + Region II). The voltages across the MFT, for both modules types, present three levels in a frequency higher than the fundamental component of V_{mult_i}, as they should operate in medium frequency.

Then, the modulator, regardless its kind, is supposed to provide the multilevel voltage characteristics for the input terminals at the modules and their MFTs, as well. Besides, it allows the correct switching stages for configurations which use more than one power module, resulting V_{mult}, as presented in Figure 2.1.

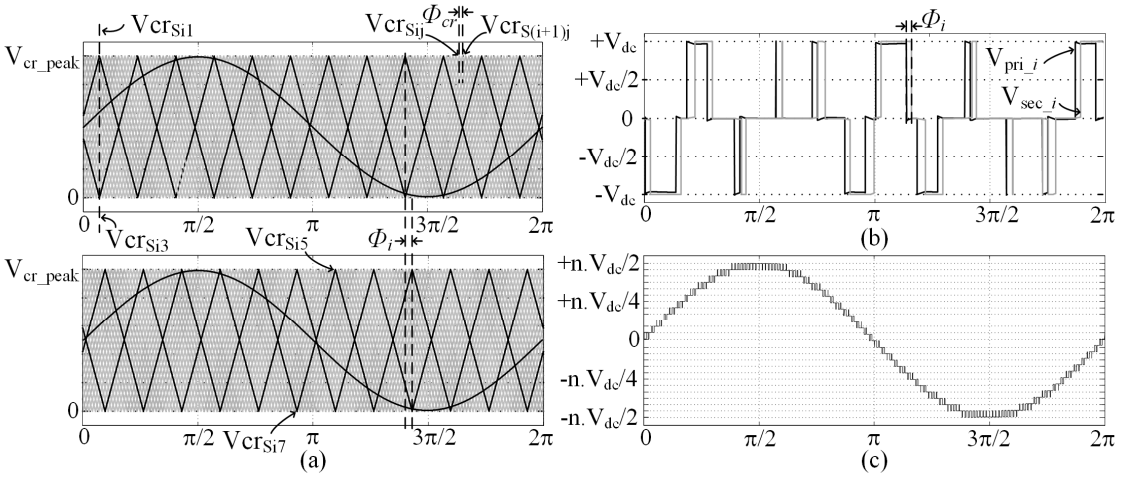
2.1.3.1 Carrier-Based Modulation

In order to obtain medium frequency operation in the MFT of each module, the adopted modulation technique must use the same switching frequency for each semiconductor

element, but with the possibility of using different duty cycles. Hence, by employing a single modulating signal, the carriers must provide such characteristics, which could be accomplished by using carriers grouped in a proper form.

The technique named Level-Shifted Multicarrier Modulation (LSMM) (49) provides the desirable different duty cycles although it imposes different switching frequencies to the semiconductors. On the other hand, the use of Phase-Shifted Multicarrier Modulation (PSMM) results in the required characteristics (50), as it should be adopted to compose the modulator block of the proposed topology.

Figure 2.5 – Carrier-based adopted modulation for type A module: (a) carriers dispositions for twelve-module converter configuration, (b) voltage waveforms in V_{pri_i} and V_{sec_i} with the phase shift of Φ_i, (c) voltage levels in V_{mult} using the modulation technique and $n_{min(A)}$=12



SOURCE: Author's right.

Figure 2.5 presents the adopted arrangements using PSMM, considering 12 type A modules. It can be seen in Figure 2.5a that the respective leg carriers (V_{crSi1}, V_{crSi3}) and (V_{crSi5}, V_{crSi7}) are 180º phase-shifted in each module, while the primary and the secondary sides (V_{crSi1}, V_{crSi5}) and (V_{crSi3}, V_{crSi7}) are phase-shifted by Φ_i. Such angular difference can be seen in Figure 2.5b where the voltages through the primary (V_{pri_i}) and secondary (V_{sec_i}) sides of the MFT in one module of the converter structure are presented.

Besides, a phase shift corresponding to Φ_{cr} must be provided between the adjacent carriers (V_{crSij}, $V_{crS(i+1)j}$), in order to generate different voltage levels in the multilevel voltage, V_{mult}. For instance, Figure 2.5c presents the twenty-five-level voltage waveform for 12 power modules structure.

The phase-shift between any two adjacent modules is described by:

$$\Phi_{cr} = \frac{360}{2 \times n} \tag{2.3}$$

The relationship between the number of modules and the voltage levels in V_{mult}, considering the module type A, is given by:

$$n_{Levels(A)} = 2n_{min(A)} + 1 \tag{2.4}$$

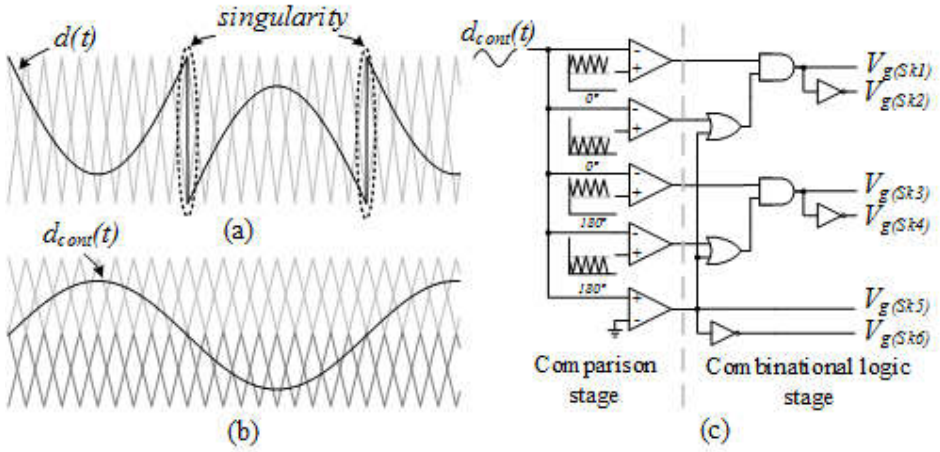
Similar technique can be applied in the converter using modules type B, however it is necessary to provide the command signal for the switches operating at low-frequency. The work presented by (51) demonstrates that the low-frequency command causes a singularity in the duty cycle function of the modulation signal of type B module, described by:

$$d(t) = V_{g(Sk5)} - M \sin(\omega_g t + \phi), \tag{2.5}$$

where, $V_{g(Sk5)}$ is the state of the switch S_{k5}, M is the modulation index, ω_g is grid angular frequency and ϕ is the phase delay.

The singularity is graphically presented in Figure 2.6a, where is possible to note that it will cause perturbations on the controlled variables, since the classical controllers with fixed gain would not be able to track the *d(t)* signal.

Figure 2.6 – Carrier-based adopted modulation for type B module: (a) singular modulating waveform produced by (2.5), (b) modulating waveform produced by new modulation arrangement, (c) proposed comparison and combinational stages of the new modulation arrangement



SOURCE: Adapted from (51).

The solution for this situation is also presented in (51). It is possible to conceive, without changing the control strategy, a new modulation arrangement which is supposed to generate the same switching states of the converter, but without the singularity in the *d(t)* function.

The disposition of the carriers and the new continuous modulation signal, $d_{cont}(t)$, is presented in Figure 2.6b. It is necessary to generates two different logic stages for the new modulator: comparison stage and combinational logic stage. Figure 2.6c presents the schematic of the new modulator, where the waveforms presented in Figure 2.6b are compared using LSMM technique and the combinational logic stage uses the result of the comparison stage to generate the gate signals of the switches in the SM_{pri_k} through a combinational circuits.

The secondary side switches, (S_{k7}, S_{k8}) and (S_{k9}, S_{k10}), are commanded equally as in the modulator for type A modules, by phase-shifting them by Φ_k.

Since the V_{mult_k} can be modulated in five different levels, the relationship between the number of modules and the voltage levels in V_{mult} is given by:

$$n_{Levels(B)} = 4n_{min(B)} + 1 \tag{2.6}$$

2.1.3.2 Space Vector Modulation

As mentioned in the last chapter, SST solutions for railway traction applications normally result in topologies with a large number of semiconductor and passive elements, implying in many variables to control. Moreover, the degree of freedom of these structures are limited in relation of the amount of variables to be regulated.

Therefore, the use of modulation techniques that allow controlling some parameters or even a power quality index, i.e the multilevel voltage THD, becomes necessary. The well-known space vector modulation (SVM), which was introduced in the 1980s (52), creates the desired flexibility. Thus, this section is dedicated to present the space vector modulation created for the proposed converter for both modules types, in order to increase their degrees of freedom.

The proposed SVM technique can be implemented following some procedures. Firstly, it is necessary to specify the possible states for the semiconductors in the single-module topology and their implication in some topology variables. In this stage, only the primary side switches are considered, since it is assumed that the secondary-side gating signals are delayed by a phase angle from the primary-side ones.

The next step consists in the determination of the total switching state vector space (SSVS) of the proposed converter using a pre-established number of modules. After that, it is possible to present some assumptions based on specific feature such as reduction of the multilevel voltage THD or improvement of MFT waveform, for instance. These assumptions allow the minimization of the SSVS, as proper sequence and an algorithm can be created from the new subspace.

The aforementioned sequence will be presented considering the proposed converter with modules type B, as the ones with type A were addressed in (53) and (54), considering the same methodology.

The proposed SVM has as main goal to impose a three-level voltage across the MFT terminals and a five-level voltage across the input terminals of each module. Besides that, the converters should operate with a phase shift between any two adjacent modules, Φ_{mod} (it is given by (2.3), $\Phi_{mod} = \Phi_{cr}$), providing medium frequency in all MFTs and maximizing the number of levels of the resulting multilevel voltage across the input terminals of the whole structure, V_{mult}.

The relationship among the voltages levels and the switching vectors, V^p, for the converter topology considering a single-module structure is shown in Table 2.1.

Table 2.1– Switching states for a single-module structure

S_{k1}	S_{k3}	S_{k5}	V_{mult_k}	V_{pri_k}	V^p
On	On	On	0	0	V^7
On	On	Off	$+V_{dc}$	0	V^6
On	Off	On	$-V_{dc}/2$	$+V_{dc}$	V^5
On	Off	Off	$+V_{dc}/2$	$+V_{dc}$	V^4
Off	On	On	$-V_{dc}/2$	$-V_{dc}$	V^3
Off	On	Off	$+V_{dc}/2$	$-V_{dc}$	V^2
Off	Off	On	$-V_{dc}$	0	V^1
Off	Off	Off	0	0	V^0

SOURCE: Author's right.

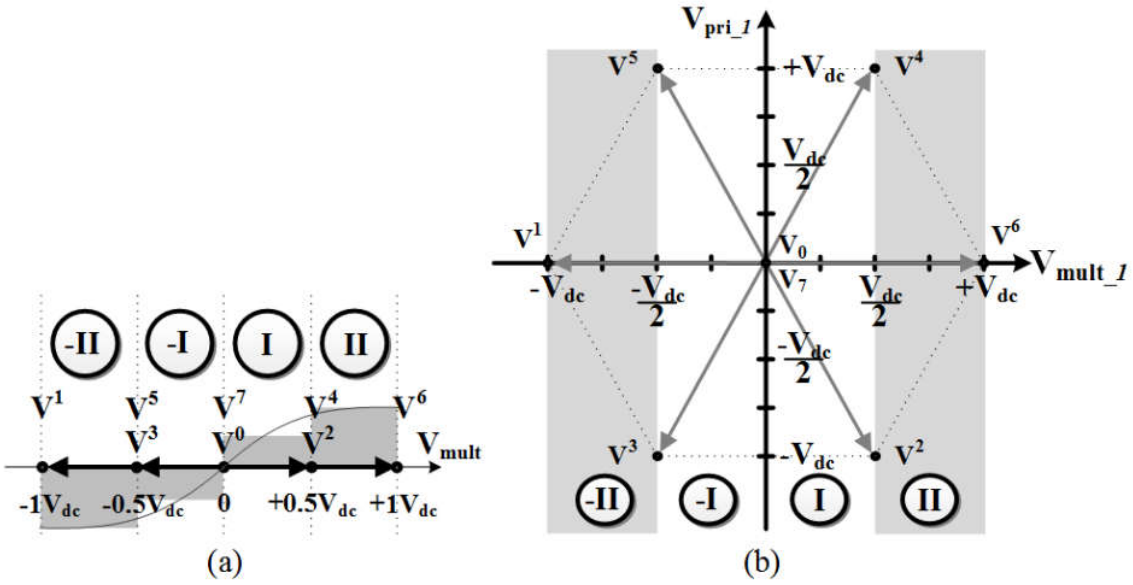
Since the pairs of switches (S_{k1}, S_{k2}), (S_{k3}, S_{k4}) and (S_{k5}, S_{k6}) operate complementarily, there are eight different arrangements for the primary-side bridge converter and, which impact on the input voltage and MFT voltage.

In order to obtain the total SSVS of the proposed structure for a generic number of modules, $n_{min(B)}$, it is considered that each module can contribute with eight different switching vectors. Consequently, for a given number of modules n, it is possible to obtain $2^{(3 \cdot n)}$ different switching vectors, with $n>0$.

In order to illustrate such relationship, an example where n=1 is presented in Figure 2.7a, where the resulting switching vectors are placed with their respective operational sectors.

Since the number of voltage levels obtained with single-module configuration is five (from (2.6)), it is expected four operational sectors, being defined as: -II, -I, I, and II.

Figure 2.7 – Figure of merit of the proposed SVM: (a) space diagram of the multilevel voltage across the converter; (b) space diagram of the multilevel voltage versus the MFT primary voltage



SOURCE: Author's right.

The operational sector is a region where switching vectors are used to obtain the proper level for V_{mult}. Therefore, the redundant switching vectors are placed at the border of each sector, favoring the determination of the switching vector sequence in each operational sector. Thus, the operational sector is responsible for the low-frequency component presented in the multilevel voltage, therefore using the switching vectors in medium frequency.

The MFT voltage is supposed to be provided by the space vector modulator as well, then Figure 2.7b presents the relationship among the switching vectors and both MFT primary and input multilevel voltages. It is worth to mention that such diagram represents the possible behavior of such voltages during a switching period.

The next step is to present assumptions to rule the choice of the switching vectors in a desired sequence. In fact, they decrease the number of available vectors in the switching state vector space, by eliminating the redundant vectors, and guiding the sequence selection in a new switching vector subspace. The following assumptions are made to obtain the sequence for the proposed SVM algorithm:

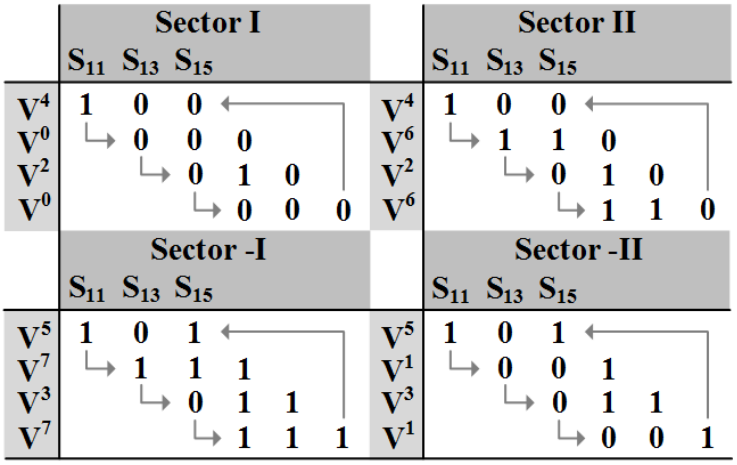
- Once the required sector is specified, the sequence must occur with the vectors of the required sector and the previous one;

- The transition of a switching state to the next one must occur at a single leg of submodules, avoiding unnecessary switching in the semiconductors;
- Any sequence is not allowed to occur with redundant vectors, which results in opposite behavior for the V_{mult}.

For instance, if the required sector is +II, the sequence must be determined by the vectors in the +II and the +I sectors from Figure 2.7. Then, it is verified if the selected vectors (V^6, V^4 and V^2) can built a sequence that only use one converter's leg commutation by transition. Next, it is verified if the sequence provides the desired behavior for the V_{mult} and V_{pri} considering the switching period, i.e. two voltage levels for V_{mult} ($+V_{dc}$ and $+0.5V_{dc}$) as Figure 2.7a and three voltage levels for V_{pri} ($+V_{dc}$, 0, $-V_{dc}$) as Figure 2.7b. Finally, it cannot use the redundant vectors V^3 and V^5 since they result in opposite value for V_{mult}.

After applying the aforementioned assumptions in the space vectors diagram, it is possible to extract the switching sequence presented in Figure 2.8.

Figure 2.8 – Proposed switching sequence for the single-module topology with type B module



SOURCE: Author's right.

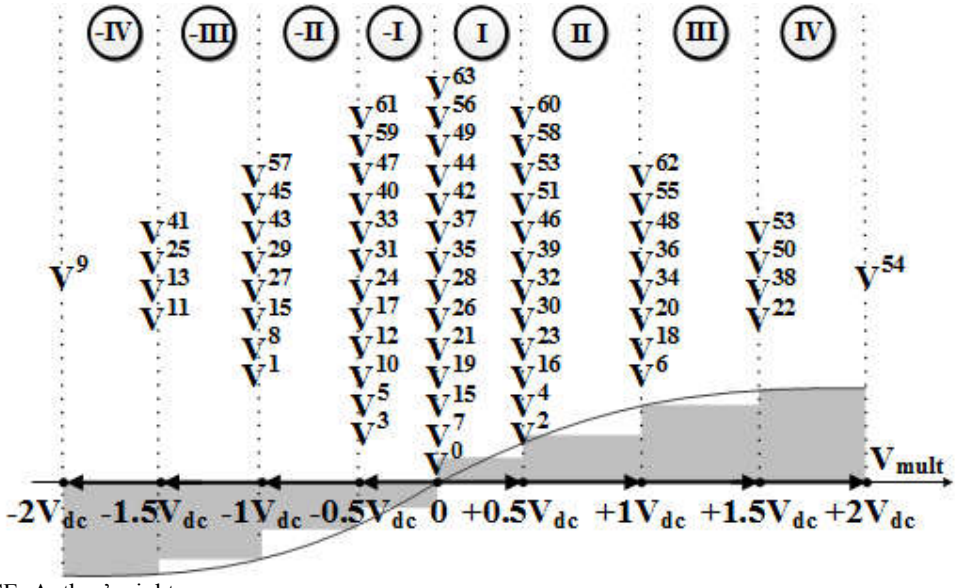
This sequence respects the initial assumptions and provides the expected behavior for the voltages in the input terminals of the module and the MFT.

Once the switching vector sequence is created for the single-module structure, it is possible to extrapolate the sequence for multi-modules structures by phase shifting the sequence in any two adjacent modules by Φ_{cr}, from (2.3). This delay can be accomplished in a practical way by some forms, such as: changing the switching vectors position in the look up table for each module, creating phase-shifted modulating signals for each module, alternating the look up table index respectively with the operational sector for the V_{mult}, among others. This study uses the last option.

There is other methodology that considers the total number of modules to obtain the SSVS and then applying the initial assumption to obtain the proper sequence.

Figure 2.9 presents the SSVS considering the two-module configuration of the proposed converter, using modules type B, which results in 64 switching vector divided in 8 operational sectors and the possibility to provide a nine-level voltage for V_{mult}.

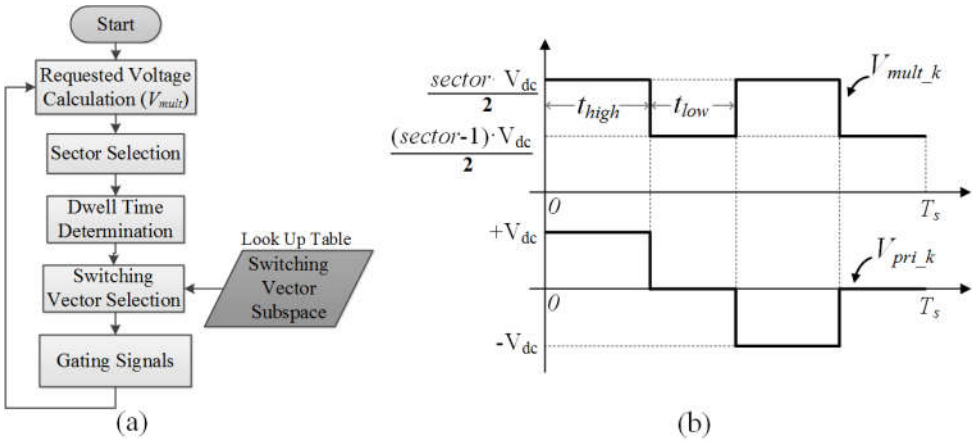
Figure 2.9 – SSVS considering the two-module configuration of the proposed converter, using modules type B



SOURCE: Author's right.

Finally, with the sequence properly obtained, it is possible to conceive the space vector algorithm. In Figure 2.10a is presented a flow chart with the logic steps elaborated for the proposed space vector modulation algorithm.

Figure 2.10 – Figure of merit of the proposed SVM: (a) low chart for the proposed space vector modulation algorithm; (b) determination of the dwell time in the proposed algorithm



SOURCE: Author's right.

As can be seen, there are five logic steps to follow.

A. Requested voltage calculation: this information is obtained from the control unit and space vector modulator is the actuator.

B. Sector selection: the control signal is compared with the number of modules, resulting in the proper voltage level interval.

C. Dwell Time Determination: Figure 2.10b illustrates the assumed dwell times in the switching period. The values of t_{high} and t_{low} are obtained using (2.7) and (2.8), respectively, where T_s is switching period, $n_{min(B)}$ is the number of modules, *Sector* is the selected sector from step *B* and $D(\omega_{PLL} \cdot t)$ is the output control signal.

$$t_{high} = \frac{T_s}{2.n_{\min(B)}}\left[1 - |Sector| + 2 \cdot D(\omega_{PLL} \cdot \mathrm{t})\right] \tag{2.7}$$

$$t_{low} = \frac{T_s}{2.n_{\min(B)}}\left[|Sector| - 2 \cdot D(\omega_{PLL} \cdot \mathrm{t})\right] \tag{2.8}$$

D. Switching Vector Selection: the information of the selected sector is used to index the (*sector*, *sector+1*) Lookup Up Table (LUT) which contains the subspace highlighted in Figure 2.8.

E. Trigger Signals Configurations: this stage applies all the information obtained in the previous steps. The algorithm uses them in a function that translates the information from the LUT to digital outputs, which are connected with switch's driver circuits.

As could be seen, the proposed algorithm considers the number of modules and the value of Φ_{mod} to elaborate the switching sequence for all the switches pairs in the converter. The control signal from the control loops is used as input signal in the modulation algorithm. Thus, the next section will explain how this signal is generated.

2.1.4 Control system

The control strategy applied to the proposed converter is presented is this section. Since the proposed converter has at least two different ways to be built, it is shown the control block diagram for both forms.

The following goals must be achieved by the control system for the accurate operation of the proposed converter:

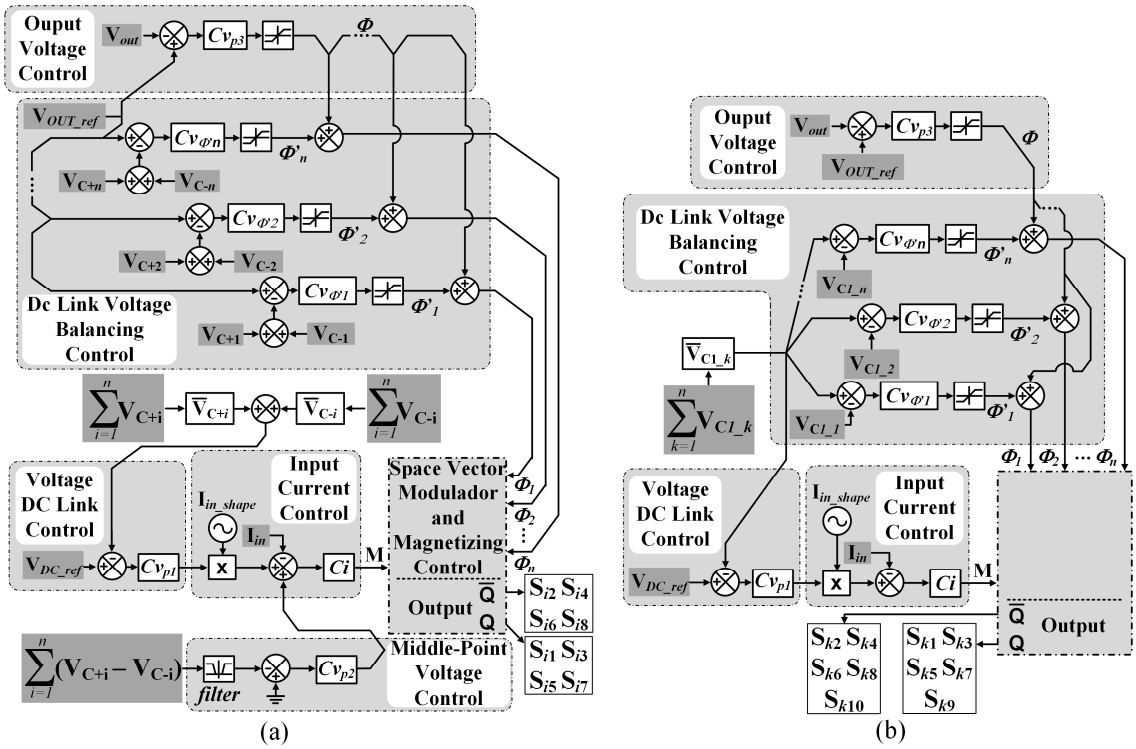
- The input current must be sinusoidal and in phase with the input voltage.

- The sum of the average voltages across capacitors C_{+i} and C_{-i} must be constant considering type A module, like the average voltage across capacitor C_{1_k} also must be constant considering type B module.
- The average voltages across capacitors C_{+i} and C_{-i} must be the same.
- The output voltage must be regulated.
- The average magnetizing current through each MFT must be negligible.

Figure 2.11a shows the control strategies applied to the converter, considering type A modules, in order to obtain the aforementioned requirements. Firstly, the dc link voltage control loop regulates the average voltage across the dc links ($V_{C+i} + V_{C-i}$). Its output signal is multiplied by a sinusoidal waveform and used as the reference for the input current control loop, performing the power factor correction in the power bridges in the primary side of the MFT.

Then, the individual dc link voltage regulation is made by a control loop denominated dc link voltage balancing control, which aims to maintain the regulation of the voltages across the dc link voltages in each module.

Figure 2.11 – Control block diagram applied to the proposed topology: (a) considering type A modules; (b) considering type B modules



SOURCE: Author's right.

In order to meet the third requirement, the middle-point voltage control loop is designed to balance the voltages across capacitors C_{+i} and C_{-i} through the sum of an offset to ac input current reference. This requirement is not necessary in the topology using modules type B, consequently there is no middle-point voltage control loop for that topology.

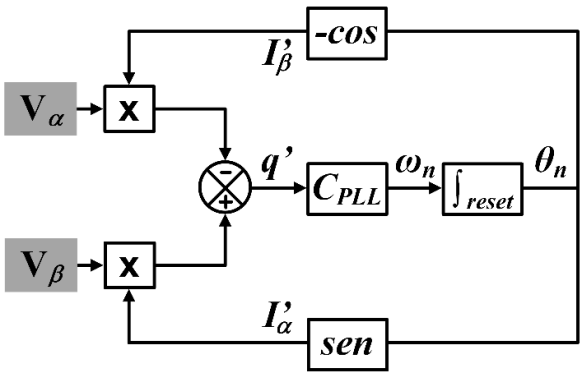
The output voltage control loop uses the phase shift angle between the primary and secondary sides of the MFT to regulate the power flow of the converter maintaining the output voltage regulated in the reference value with a same phase angle in all modules. Therefore, the responsibility of the dc link voltage balancing control is to allow each module to operate with a slight different phase-shift angle, what allow the balance of the voltages among the dc link capacitors at the primary side in the MFTs.

Thus, with different phase angles, the modules could process slightly different values of power, regulating their dc link voltages individually. It is worth to mention that the dc link voltage control only is responsible for the regulation of the average value of all dc links in the whole converter, which combined with the balancing dc link voltage control guarantee the same average value of the dc link voltages in the modules, despite the power flow conditions imposed by the output control loop.

The synchronism circuit considered for the study is the phase locked loop (PLL), more specifically the q-PLL presented in (55) and in Figure 2.12. With the tracking of the ac voltage phase, it is possible to create variables with sinusoidal variation in the microcontroller code, obtaining the shape for the ac current used in the reference signal of the input current loop.

However, the structure presented in (55) is applied to three-phase systems, then it is necessary to adapt it for single-phase systems, as presented in (56).

Figure 2.12 – q-PLL structure applied in the control methodology



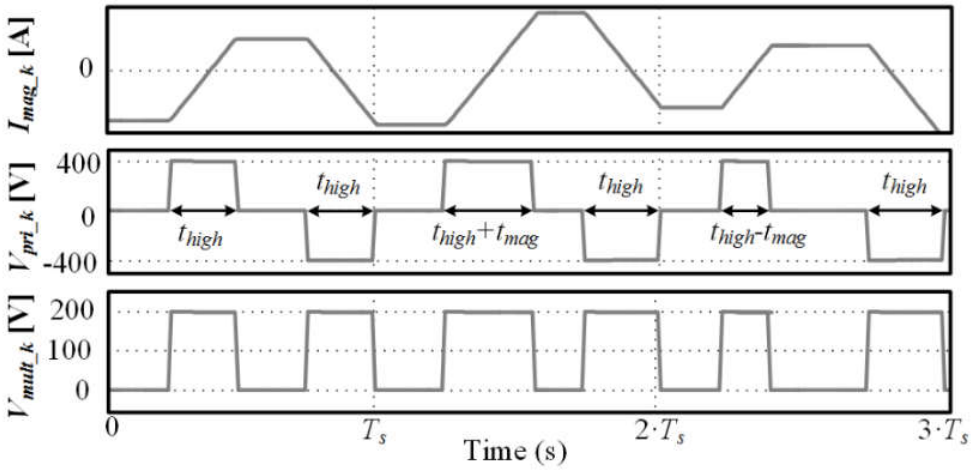
SOURCE: Adapted from (55).

The adaptation consists in obtaining the ac voltage from a single-phase system and from generating other voltage signal phase shifted by 90º degrees. Then, both voltages are applied in the q-PLL circuit, since they can be treated as V_α and V_β from Clarke transform (57).

Finally, the magnetizing current is controlled by an algorithm implemented in the modulator block, a magnetizing current control loop is used to generate the requested time to compensate the average value of the current. This interval is inserted in the converter operation by the space vector modulation algorithm.

When is necessary to increase the instantaneous magnetizing current and consequently its average value, the time from the magnetizing current control loop, t_{mag}, is added to the t_{high} calculated by the SVM algorithm, creating larger time for the MFT to magnetize. Same logic it is used when is necessary a smaller magnetizing time, by subtracting t_{mag} from t_{high}. These behaviors are presented in Figure 2.13 in three different switching periods for t_{mag}=0, t_{high}+t_{mag}, and t_{high}-t_{mag}, respectively.

Figure 2.13 – Magnetizing current behavior with the magnetizing control loop



SOURCE: Author's right.

The proper design of all control loops shall be seen in the next chapter, followed by their respective simulation and experimental results for both steady and dynamic behaviors.

2.2 Quantitative analysis

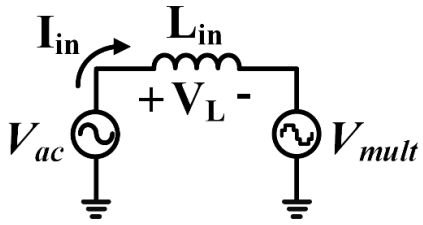
This section will deal with the qualitative analysis of the proposed converter. The input inductive filter as the equivalent inductance of the MFT in a fundamental model will be presented in terms of the converter parameters. The losses analysis is presented as well, followed by a comparative losses study with others topologies.

The quantitative analysis considering the proposed converter with modules type A is presented by (54).

2.2.1 Input Inductance determination

The input filter inductance can be obtained through the input current ripple. Figure 2.14 presents the model adopted to obtain the input inductance filter.

Figure 2.14 – Model adopted to the input inductance filter analysis



SOURCE: Author's right.

The voltage across the inductance L_{in} can be described by (2.9).

$$V_L = V_p.sen\left(\omega_{grid}.t\right) - V_{mult} = \frac{\Delta i_L}{\Delta t}.L_{in} \tag{2.9}$$

The inductive input filter has its charging period when the V_{mult} is in its lower level. Then, replacing the lower level in V_{mult} (Figure 2.10b) and Δt by t_{low} from (2.8), the input current ripple can be obtained as follow:

$$\Delta i_L = \frac{1}{L_{in}}\left[V_p.sen\left(\omega_{grid}.t\right) - \frac{V_{dc}}{2}\left(Sector - 1\right)\right].\left[\frac{T_s}{2.n}\left(Sector - 2\cdot M(\omega_{PLL}\cdot \mathrm{t})\right)\right] \tag{2.10}$$

The maximum point of ripple from (2.10) is investigated, seeking its relationship with the input inductance, which is given by:

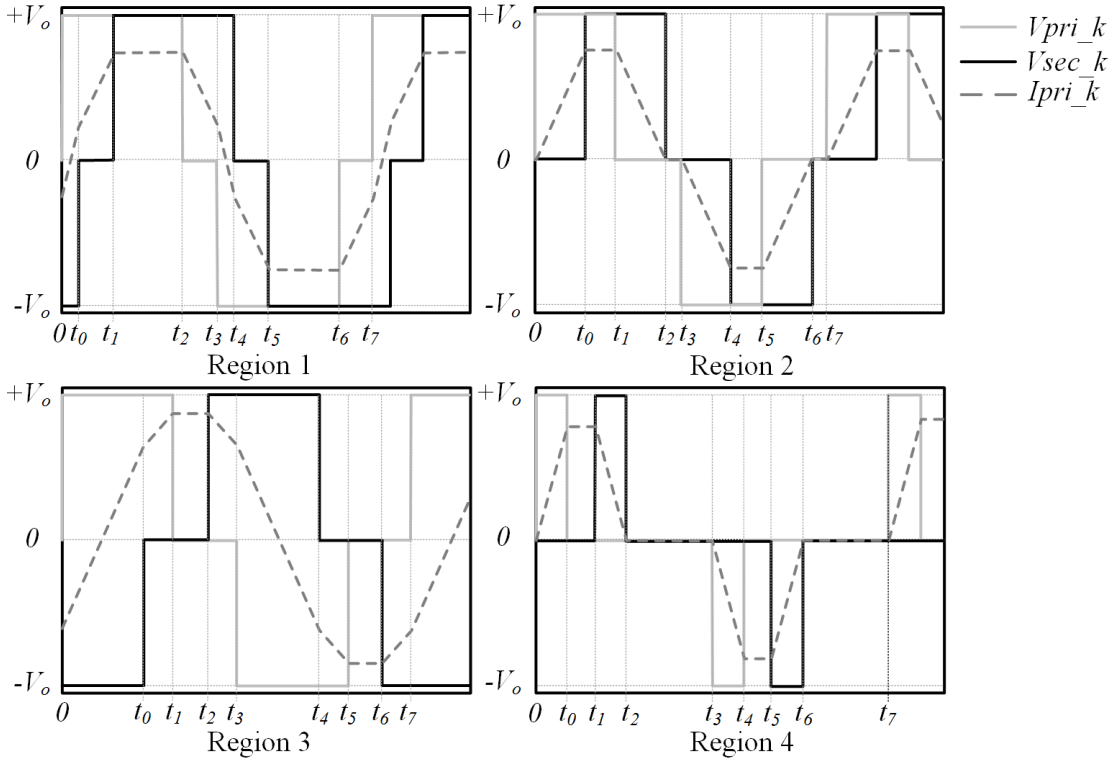
$$L_{in} = \frac{T_s \cdot V_{dc}}{16 \cdot n \cdot \Delta i_{Lin\_max}} \tag{2.11}$$

2.2.2 Complete model

In (58) the ac/dc DAB converter is analyzed in twelve distinct operation regions, which are classified as: four with positive power flow, four with negative power flow and four considering different duty cycles between the bridges of the converter.

This study uses similar methodology to address the operation region of the proposed converter with type B modules. Since the proposed converter operates with fixed duty cycles and the turn ratio of the MFT is unitary, it is possible to summarize its operation regions in four conditions as presented in Figure 2.15. Each region is divided in seven instants, which are presented in Table 2.2.

Figure 2.15 – Operation regions of the proposed converter considering type B modules



SOURCE: Author's right.

Table 2.2– Instants considered in each operating region

Instant	***Region 1***	***Region 2***	***Region 3***	***Region 4***
t_0	$\frac{\Phi_k}{2.\pi.f_s}+D.T_s-\frac{T_s}{2}$	$\frac{\Phi_k}{2.\pi.f_s}$	$\frac{\Phi_k}{2.\pi.f_s}-\frac{T_s}{2}+D.T_s$	$D.T_s$
t_1	$\frac{\Phi_k}{2.\pi.f_s}$	$D.T_s$	$D.T_s$	$\frac{\Phi_k}{2.\pi.f_s}$
t_2	$D.T_s$	$\frac{\Phi_k}{2.\pi.f_s}+D.T_s$	$\frac{\Phi_k}{2.\pi.f_s}$	$\frac{\Phi_k}{2.\pi.f_s}-D.T_s$
t_3	$\frac{T_s}{2}$	$\frac{T_s}{2}$	$\frac{T_s}{2}$	$\frac{T_s}{2}$
t_4	$\frac{\Phi_k}{2.\pi.f_s}+D.T_s$	$\frac{\Phi_k}{2.\pi.f_s}+\frac{T_s}{2}$	$\frac{\Phi_k}{2.\pi.f_s}+D.T_s$	$\frac{T_s}{2}+D.T_s$
t_5	$\frac{\Phi_k}{2.\pi.f_s}+\frac{T_s}{2}$	$D.T_s+\frac{T_s}{2}$	$\frac{T_s}{2}+D.T_s$	$\frac{\Phi_k}{2.\pi.f_s}+\frac{T_s}{2}$
t_6	$D.T_s+\frac{T_s}{2}$	$\frac{\Phi_k}{2.\pi.f_s}+\frac{T_s}{2}+D.T_s$	$\frac{\Phi_k}{2.\pi.f_s}+\frac{T_s}{2}$	$\frac{\Phi_k}{2.\pi.f_s}+\frac{T_s}{2}+D.T_s$
t_7	T_s	T_s	T_s	T_s

SOURCE: Author's right.

In Table 2.3, it is possible to see the MFT primary voltage, V_{pri_k}, for each region.

Table 2.3– MFT primary voltage by Region

Interval	*Region 1*	*Region 2*	*Region 3*	*Region 4*
$[0, t_0]$	V_o	V_o	V_o	V_o
$]t_0, t_1]$	V_o	V_o	V_o	0
$]t_1, t_2]$	V_o	0	0	0
$]t_2, t_3]$	0	0	0	0
$]t_3, t_4]$	$-V_o$	$-V_o$	$-V_o$	$-V_o$
$]t_4, t_5]$	$-V_o$	$-V_o$	$-V_o$	0
$]t_5, t_6]$	$-V_o$	0	0	0
$]t_6, t_7]$	0	0	0	0

SOURCE: Author's right.

Then, similarly, it is possible to obtain the analytic expression of the current through the series inductance, L_{disp_k}, for each interval and the considered operating region.

Table 2.4– Currents expression for Region 1 and 2

Interval	*Region 1*	*Region 2*
$[0, t_0]$	$\left(2.V_o.t - V_o.t_0\right).L_{disp\_k}^{-1}$	$V_o.L_{disp\_k}^{-1}.t$
$]t_0, t_1]$	$\frac{V_o.(t-t_0)}{L_{disp\_k}} + \frac{V_o}{L_{disp\_k}}t_0$	$\frac{V_o.\Phi_k}{2.\pi.f_s L_{disp\_k}}$
$]t_1, t_2]$	$\frac{V_o.\Phi_k}{2.\pi.f_s L_{disp\_k}}$	$\frac{V_o.\Phi_k}{2.\pi.f_s L_{disp\_k}} - \frac{V_o.(t-t_1)}{L_{disp\_k}}$
$]t_2, t_3]$	$-\frac{V_o.(t-t_2)}{L_{disp\_k}} + \frac{V_o.\Phi_k}{2.\pi.f_s L_{disp\_k}}$	0
$]t_3, t_4]$	$\left(-2.V_o.(t-t_3) + V_o.t_0\right).L_{disp\_k}^{-1}$	$-V_o.(t-t_3).L_{disp\_k}^{-1}$
$]t_4, t_5]$	$-\frac{V_o.(t-t_4)}{L_{disp\_k}} - \frac{V_o}{L_{disp\_k}}t_0$	$-\frac{V_o.\Phi_k}{2.\pi.f_s L_{disp\_k}}$
$]t_5, t_6]$	$-\frac{V_o.\Phi_k}{2.\pi.f_s L_{disp\_k}}$	$-\frac{V_o.\Phi_k}{2.\pi.f_s L_{disp\_k}} + \frac{V_o.(t-t_5)}{L_{disp\_k}}$
$]t_6, t_7]$	$\frac{V_o.(t-t_6)}{L_{disp\_k}} - \frac{V_o.\Phi_k}{2.\pi.f_s L_{disp\_k}}$	0

SOURCE: Author's right.

Table 2.4 and Table 2.5 present these expressions to regions 1 and 2 and regions 3 and 4, respectively.

Table 2.5– Currents expression for Region 3 and 4

Interval	*Region 3*	*Region 4*
$[0, t_0]$	$\left(2.V_o.t - V_o.t_0\right).L_{disp\_k}^{-1}$	$V_o.L_{disp\_k}^{-1}.t$
$]t_0, t_1]$	$\left(V_o.\left(t-t_0\right)+V_o.t_0\right).L_{disp\_k}^{-1}$	$T_s.V_o.L_{disp\_k}^{-1}.\Phi_k$
$]t_1, t_2]$	$V_o.D.T_s.L_{disp\_k}^{-1}$	$\left(V_o.D.T_s - V_o.\left(t-t_1\right)\right).L_{disp\_k}^{-1}$
$]t_2, t_3]$	$\left(-V_o.\left(t-t_2\right)+V_o.D.T_s\right).L_{disp\_k}^{-1}$	0
$]t_3, t_4]$	$\left(-2.V_o.\left(t-t_3\right)+V_o.t_0\right).L_{disp\_k}^{-1}$	$-V_o.\left(t-t_3\right).L_{disp\_k}^{-1}$
$]t_4, t_5]$	$\left(-V_o.\left(t-t_4\right)-V_o.t_0\right).L_{disp\_k}^{-1}$	$-V_o.D.T_s.L_{disp\_k}^{-1}$
$]t_5, t_6]$	$-V_o.D.T_s.L_{disp\_k}^{-1}$	$\left(-V_o.D.T+V_o.\left(t-t_5\right)\right).L_{disp\_k}^{-1}$
$]t_6, t_7]$	$\left(V_o.\left(t-t_6\right)-V_o.D.T_s\right).L_{disp\_k}^{-1}$	0

SOURCE: Author's right.

Once the voltages and current analytic expressions of the MFT primary side are determined, it is possible to obtain the instantaneous power equations through the multiplication of the tables terms by the proper interval and region, resulting in the equations presented in Table 2.6.

Table 2.6– Instantaneous power expression by Region

Interval	*Region 1*	*Region 2*	*Region 3*	*Region 4*
$[0, t_0]$	$\frac{2.V_o^2}{L_{disp\_k}}t - \frac{V_o^2}{L_{disp\_k}}t_0$	$\frac{V_o^2}{L_{disp\_k}}t$	$\frac{2.V_o^2}{L_{disp\_k}}t - \frac{V_o^2}{L_{disp\_k}}t_0$	$\frac{V_o^2}{L_{disp\_k}}t$
$]t_0, t_1]$	$\frac{V_o^2.\left(t-t_0\right)}{L_{disp\_k}} + \frac{V_o^2}{L_{disp\_}}$	$\frac{V_o^2.\Phi_k}{2.\pi.f_s L_{disp\_k}}$	$\frac{V_o^2.\left(t-t_0\right)}{L_{disp\_k}} + \frac{V_o^2}{L_{disp\_k}}$	0
$]t_1, t_2]$	$\frac{V_o^2.\Phi_k}{2.\pi.f_s L_{disp\_k}}$	0	0	0
$]t_2, t_3]$	0	0	0	0

SOURCE: Author's right.

Due the symmetry of the voltage behavior for the $]t_2, t_7]$ interval, the resulting expressions are equal with the ones presented in Table 2.6, which demonstrate that the power has the double of the current frequency.

With these time functions, it is possible to calculate the quasi-instantaneous power expressions for each region by meaning of an integration considering the switching period, T_s. It is worth to mention that, in this operation, T_s is considered significantly smaller than the grid

period, therefore D is considered constant between two adjacent switching periods. The result of these derivations is presented in Table 2.7.

Table 2.7– Quasi-instantaneous Power by Region

Region	***Quasi-instantaneous Power***
1	$\frac{V_o^2.\left(-4.\pi^2.D^2+4.\pi^2.D-2.\Phi_k^2+2.\pi.\Phi_k^2-\pi^2\right)}{4.\pi^2.L_{disp\_k}.f_s}$
2	$\frac{V_o^2.\Phi_k^2.(4.\pi.D-\Phi_k^2)}{4.\pi^2.L_{disp\_k}.f_s}$
3	$-\frac{V_o^2.\left(\Phi_k^2-\pi\right).\left(\Phi_k^2-\pi+4.\pi.D\right)}{4.\pi^2.L_{disp\_k}.f_s}$
4	$\frac{V_o^2.D^2}{L_{disp\_k}.f_s}$

SOURCE: Author's right.

Finally, it is possible to obtain the total transferred active power in the MFT considering the variation of D during the grid period, T_{grid}. The duty cycle variation for the proposed topology with type B modules is defined by (2.12) and (2.13), where M is the modulation index and ω_{grid} is the angular frequency of the grid.

$$D_1(\omega_{grid}\cdot \mathrm{t}) = \frac{M}{2}\sin(\omega_{grid}\cdot \mathrm{t}) \tag{2.12}$$

$$D_2(\omega_{grid}\cdot \mathrm{t}) = 1-\frac{M}{2}\sin(\omega_{grid}\cdot \mathrm{t}) \tag{2.13}$$

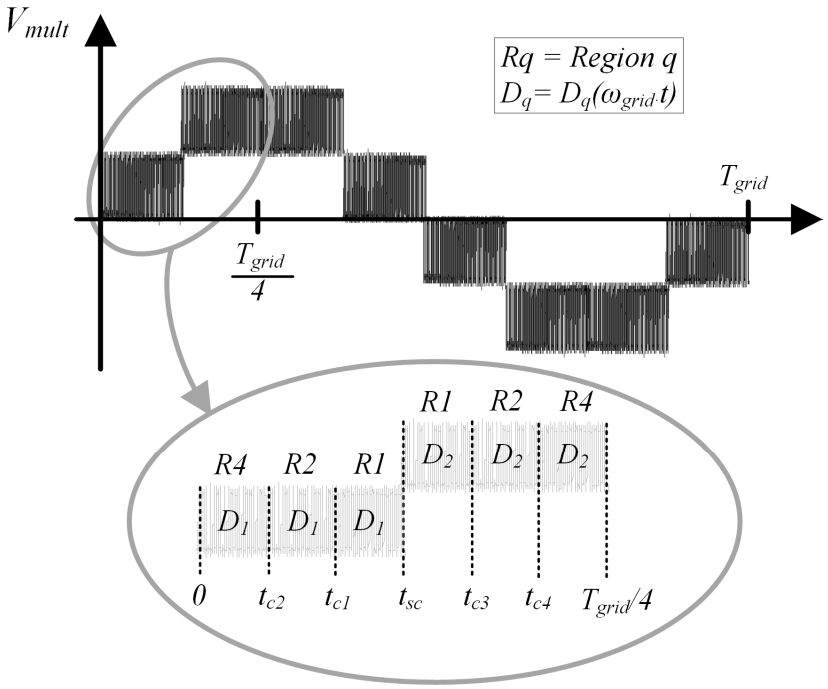
It is necessary to determinate the boundary conditions among the operating regions to determinate the limit of integrations. Besides, it is, also, necessary determinate the operating limits of (2.12) and (2.13), which is labelled as t_{sc} and it is expressed by (2.14).

$$t_{sc} = \frac{1}{\omega_{grid}}\arcsin\left(\frac{1}{M}\right) \tag{2.14}$$

Figure 2.16 presents, for a quarter of grid period, the behavior of both aspects: regions and duty cycle boundaries. It is shown every boundary instant, while t_{c1}, t_{c2}, t_{c3} and t_{c4} are defined in Table 2.8.

Table 2.8 presents the boundary instants considering the regions transitions and Φ_k less than 90º. It is possible to note from Figure 2.15 that $\Phi_k < 90^o$ implies no occurrence of Region 3, justifying its absence in Figure 2.16.

Figure 2.16 – Boundary conditions for region and duty cycle functions



SOURCE: Author's right.

Table 2.8– Boundary instants by its transition of regions

Transition	***IF***	***Instant***	***Value***
Region 2 to Region 1	$\Phi_k \leq \pi.(1-M)$ / $\Phi_k > \pi.(1-M)$	t_{c1}	$\frac{1}{\omega_{grid}}\arcsin\left(\frac{\pi-\Phi_k}{\pi.M}\right)$ / $\frac{T_{grid}}{4}$
Region 4 to Region 2	$\Phi_k \leq \pi.M$ / $\Phi_k > \pi.M$	t_{c2}	$\frac{1}{\omega_{grid}}\arcsin\left(\frac{\Phi_k}{\pi.M}\right)$ / $\frac{T_{grid}}{4}$
Region 1 to Region 2	$\Phi_k \leq \pi.(2-M)$ / $\Phi_k > \pi.(2-M)$	t_{c3}	$\frac{1}{\omega_r}arcsen\left(\frac{2\pi-\Phi_k}{\pi.M}\right)$ / $\frac{T_{grid}}{4}$
Region 2 to Region 4	$\Phi_k \geq \pi.(M-1)$ / $\Phi_k < \pi.(M-1)$	t_{c4}	$\frac{1}{\omega_r}arcsen\left(\frac{\pi+\Phi_k}{\pi.M}\right)$ / $\frac{T_{grid}}{4}$

SOURCE: Author's right.

A related point to consider is the boundary instants being dependent of the phase shift angles, as well as the duty cycle required to provide the proper voltage level. Thus, their determination is more easily obtained from a conditional requirement involving Φ_k and M, as presented in the second column (*IF*) of Table 2.8.

Thus, with the intervals and its time function, it is possible to obtain the expression for the active power considering the grid period, being described by (2.15) to (2.19).

$$\begin{aligned} P_{tc1}(\Phi,M) &= V_o^2.\left(4.\pi^2.\omega_{grid}.t_{c1} + 8.\pi^2.M.\cos\left(\omega_{grid}.t_{c1}\right)\right) + \\ &+ V_o^2.\left(-\pi^2.M^2.\sin\left(2.\omega_{grid}.t_{c1}\right) + 4.\Phi_k^2.\omega_{grid}.t_{c1} + 2.\pi^2.M^2.\omega_{grid}.t_{c1}\right) + \\ &+ V_o^2.\left(-8.\pi.\Phi_k.\omega_{grid}.t_{c1} - 8.\pi.\Phi_k.M.\cos\left(\omega_{grid}.t_{c1}\right)\right) \end{aligned} \tag{2.15}$$

$$\begin{aligned} P_{tc2}(\Phi,M) &= V_o^2.\left(-\pi^2.M^2.\sin\left(2.\omega_{grid}.t_{c2}\right) + 4.\Phi_k^2.\omega_{grid}.t_{c2}\right) + \\ &+ V_o^2.\left(2.\pi^2.M^2.\omega_{grid}.t_{c2} + 8.\pi.\Phi_k.M.\cos\left(\omega_{grid}.t_{c2}\right)\right) \end{aligned} \tag{2.16}$$

$$\begin{aligned} P_{tc3}(\Phi,M) &= V_o^2.\left(-4.\pi^2.\omega_{grid}.t_{c3} - 8.\pi^2.M.\cos\left(\omega_{grid}.t_{c3}\right)\right) + \\ &+ V_o^2.\left(\pi^2.M^2.\sin\left(2.\omega_{grid}.t_{c3}\right) - 4.\Phi_k^2.\omega_{grid}.t_{c3} - 2.\pi^2.M^2.\omega_{grid}.t_{c3}\right) + \\ &+ V_o^2.\left(-8.\pi.\Phi_k.\omega_{grid}.t_{c3} - 8.\pi.\Phi_k.M.\cos\left(\omega_{grid}.t_{c3}\right)\right) \end{aligned} \tag{2.17}$$

$$\begin{aligned} P_{tc4}(\Phi,M) &= V_o^2.\left(-16.\pi^2.\omega_{grid}.t_{c1} - 16.\pi^2.M.\cos\left(\omega_{grid}.t_{c4}\right)\right) + \\ &+ V_o^2.\left(\pi^2.M^2.\sin\left(2.\omega_{grid}.t_{c4}\right) - 4.\Phi_k^2.\omega_{grid}.t_{c4} - 2.\pi^2.M^2.\omega_{grid}.t_{c4}\right) + \\ &+ V_o^2.\left(16.\pi.\Phi_k.\omega_{grid}.t_{c4} + 8.\pi.\Phi_k.M.\cos\left(\omega_{grid}.t_{c4}\right)\right) \end{aligned} \tag{2.18}$$

$$P(\Phi,M) = \frac{\pi^3.M^2 + 8.\pi^3 + P_{tc1}(\Phi,M) + P_{tc2}(\Phi,M) + P_{tc3}(\Phi,M) + P_{tc4}(\Phi,M)}{8.\pi^3.L_{leak\_k}.f_s} \tag{2.19}$$

The inductance of the input filter can be determined by (2.20), considering a fixed $\Phi_{k\_desired}$ and $M_{desired}$ for a desired active power, $P_{desired}$.

$$\begin{aligned} L_{leak\_k} &= \frac{\pi^3.M_{desired}^{\ 2} + 8.\pi^3 + P_{tc1}\left(\Phi_{k\_desired}, M_{desired}\right)}{8.\pi^3.P_{desired}.f_s} + \\ &+ \frac{P_{tc2}\left(\Phi_{k\_desired}, M_{desired}\right) + P_{tc3}\left(\Phi_{k\_desired}, M_{desired}\right) + P_{tc4}\left(\Phi_{k\_desired}, M_{desired}\right)}{8.\pi^3.P_{desired}.f_s} \end{aligned} \tag{2.20}$$

2.2.3 Analysis of losses

This section will present the losses analysis of the converter considering the proposed converter with type B modules to address the devices losses and the theoretical

efficiency. It is, also, shown a comparative losses analysis, considering other well-known structures.

2.2.3.1 Conduction and switching losses calculation

In this section, the conduction and switching losses of the semiconductors are obtained. Therefore, the switch characteristics is required from the manufacturer, and these information are provided by curves. Then, it is necessary to use some interpolation technique in order to extract the losses amount. In (2.21) and (2.22), it can be seen the equations that represent the linearized curve for the instantaneous voltage as a function of the current through the transistor and the antiparallel diode, respectively.

$$V_{Tij}(t) = V_{CEsat} + R_s \cdot I_{Tij}(t) \tag{2.21}$$

$$V_{Dij}(t) = V_{Dcond} + R_D \cdot I_{Dij}(t), \tag{2.22}$$

where R_s is the switch resistance and R_D is the diode resistance, V_{CEsat} is the transistor saturation voltage and V_{Dcond} is the voltage drop across the forward-biased diode.

It is possible to obtain the instantaneous power in the switch, by multiplying (2.21) and (2.22) with the respective current device. Then, by applying average value, it is conceivable to calculate the conduction losses for the transistor and the diode, as presented in (2.23) and (2.24), respectively.

$$P_{Tij\_cond} = \frac{1}{T_{grid}} \cdot \int_0^{T_{grid}} \left(V_{CEsat} . I_{Tij}(t) + R_s \cdot {I_{Tij}}^2(t) \right) dt = V_{CEsat} . I_{Tij\_avg} + R_s \cdot {I_{Tij\_rms}}^2 \tag{2.23}$$

$$P_{Dij\_cond} = \frac{1}{T_{grid}} \cdot \int_0^{T_{grid}} \left(V_{Dcond} . I_{Dij}(t) + R_D \cdot {I_{Dij}}^2(t) \right) dt = V_{Dcond} . I_{Dij\_avg} + R_D \cdot {I_{Dij\_rms}}^2 \tag{2.24}$$

where I_{Tij_avg} and I_{Dij_avg} are the average current through every transistor and diode, while I_{Tij_rms} and I_{Dij_rms} are the rms current.

The switching losses calculation requires the energy loss curve from the device datasheet. Then, with a polynomial regression, it is possible to obtain the energy losses during the turn on and turn off of the switch. These energy expression can be seen in (2.25) and (2.26), considering a second order polynomial regression.

$$W_{Tij\_ON}(t) = k_{0\_ON} + k_{1\_ON} \cdot I_{Tij}(t) + k_{2\_ON} \cdot \left[I_{Tij}(t) \right]^2 \tag{2.25}$$

$$W_{Tij\_OFF}(t) = k_{0\_OFF} + k_{1\_OFF} \cdot I_{Tij}(t) + k_{2\_OFF} \cdot \left[I_{Tij}(t) \right]^2 \tag{2.26}$$

where, k_{i_ON} and k_{i_OFF} are the regression coefficients. It is possible to note that the energy loss depends of the current flowing in the device.

In order to obtain power, it is necessary to multiply the energy expression by the switching frequency and extract the average value, resulting in the (2.27) and (2.28).

$$P_{Tij\_ON} = \frac{1}{T_r} \cdot \int_0^{T_r} f_s \cdot W_{Tij\_ON}(t) \cdot dt \tag{2.27}$$

$$P_{Tij\_OFF} = \frac{1}{T_r} \cdot \int_0^{T_r} f_s \cdot W_{Tij\_OFF}(t) \cdot dt \tag{2.28}$$

Finally, it is necessary to obtain the energy loss due the diode reverse recovery. According with Casanellas (59) such energy can be calculated as follow:

$$W_{Dij\_rr}(t) = V_{cc} \cdot \left(0{,}8 + \frac{0{,}2 \cdot I_{Dij}(t)}{I_n}\right) \cdot t_{rr} \cdot \left(0{,}35 \cdot t_{rr} + 0{,}15 \cdot \frac{I_{rr}}{I_n} \cdot I_{Dij}(t) + I_{Dij}(t)\right), \tag{2.29}$$

where, I_n is the switch rated current, t_{rr} reverse recovery time and I_{rr} is the reserve recovery current peak. Executing the same procedures presented for P_{Tij_ON} and P_{Tij_OFF}, it is possible to obtain the following expression for the power loss due the diode reverse recovery:

$$P_{Dij\_rr} = \frac{1}{T_r} \cdot \int_0^{T_r} f_s \cdot W_{Dij\_rr}(t) \cdot dt\,. \tag{2.30}$$

Then, the total power loss of the semiconductors can be expressed by the sum of the conduction, switching and reverse recovery powers, resulting in the following expression:

$$P_{switches} = \sum_{j=1}^{10} \left(P_{Tij\_cond} + P_{Dij\_cond} + P_{Tij\_ON+} P_{Tij\_OFF} + P_{Dij\_rr}\right) \tag{2.31}$$

The characteristics of the switches models selected for the losses analysis is presented in Table 2.9, as well as, the coefficients resulted from the polynomial regression.

Table 2.9– Electric characteristics of the switch used in the analyses

characteristic	***IIRGP50 B60PD***	***C3M006 5090J***	***characteristic***	***IIRGP50B6 0PD***	***C3M00650 90J***
Collector-to-Emitter voltage	600 V	900 V	R_D	20 mΩ	-
Continuous collector current	33 A	35 A	k_{0_ON}	489 nJ	25.94 µJ
Reverse recovery time	74 ns	12 ns	k_{1_ON}	15.22 µWb	756.3 nWb
V_{CEsat}	1.687 V	8.33 mV	k_{2_ON}	86.55 nH	15.62 nH
R_S	31 mΩ	85 mΩ	k_{0_OFF}	282 µJ	6.937 µJ
V_{CEsat_3Q}	-	1.67 mV	k_{1_OFF}	-7.94 µWb	256.3 nWb
R_{S_3Q}	-	82 mΩ	k_{2_OFF}	390 nH	20,62 nH
V_{Dcond}	1.479 V	-			

SOURCE: Author's right.

The first switch is the IGBT IRGP50B60PD and the second one is the silicon carbide MOSFET, C3M0065090J. It is worth to mention that the IGBT negative current will flow through the antiparallel diode, however in the MOSFET it is necessary to apply the regression for first and third operational quadrants. Thus, V_{CEsat_3Q} and R_{S_3Q} are the values obtained with the regression on the third quadrant.

The result from the losses analysis is presented in Table 2.10, where it is possible to note that the silicon carbide switch obtained the best result for the losses analysis.

Table 2.10– Switches losses

characteristic	***IRGP50B60PD***	***C3M0065090J***
Conduction on the first quadrant	14.04 W	4.60 W
Switching	46.60 W	5.42 W
Conduction on the third quadrant	10.12 W	2.28 W
Reverse recovery	11.97 W	-
Total	82.73 W	12.31 W

SOURCE: Author's right.

2.2.3.2 Transformer and inductance losses calculation

The proposed converter has four magnetics: the input inductance, the leakage inductance, the autotransformer and the MFT. The input inductance can be obtained by (2.11), once the maximum input current ripple is specified. The leakage inductance can be obtained by (2.20), once is specified the power, modulation index and phase shitted angle.

Applying the values from Table 2.11, it is possible to obtain 1.57 mH and 331.8 µH for the input inductance and the leakage one, respectively.

Table 2.11– Converter specifications

parameters	***Value***
Dc link voltage	V_{dc} = 400 V
Output voltage	V_o = 400 V
Rms input voltage	V_{ac} = 220 V
Switching frequency	f_s = 20 kHz
Output power	P_{out} = 1 kW
Turn ratio	$a = 1$

SOURCE: Author's right.

With these inductance values, it is possible to determinate the respective inductor. The inductors physical specifications are presented in Table 2.12. The current density and magnetic flux density are specified to keep the transformers and inductors in the proper operational range suggested by the manufacturer.

Table 2.12– Inductor characteristics

parameter	L_{in}	L_{disp}
Current density	450 A/cm^2	450 A/cm^2
Magnetic flux density	0.3 T	0.3 T
Number of turns	317	152
Copper wires	4 wires / 22 AWG	3 wires / 22 AWG
Wire length	26.02 m	9.42 m
Fill factor	0.27	0.32
Selected Core	MMT034 T7713	MTT002 T4416

SOURCE: Author's right.

The physical characteristics for the transformer and autotransformer are presented in Table 2.13.

Table 2.13– Transformers characteristics

parameter	*autotransformer*	*MFT*
Current density	450 A/cm^2	450 A/cm^2
Magnetic flux density	0.1 T	0.24 T
Number of turns	160/160	134/134
Copper wires	2 wires / 22 AWG	3 wires / 22 AWG
Wire length	14.45 m	12.12 m
Fill factor	0.23	0.29
Selected Core	MMT139T6325	MMT139T6325

SOURCE: Author's right.

The copper conduction losses calculation is obtained through the following expression:

$$P_{copper} = R_{wire}.I_{rms}^{\ 2}, \tag{2.32}$$

where, R_{wire} is the conductor resistance.

Moreover, there are core losses which should be considered in the analysis, as well. These losses are proportional with the switching frequency, the magnetic flux density and the core volume (3). The core manufacturer provides the values related with the core analysis. Table 2.14 presents the magnetics losses obtained from the analysis.

Table 2.14– Magnetics losses

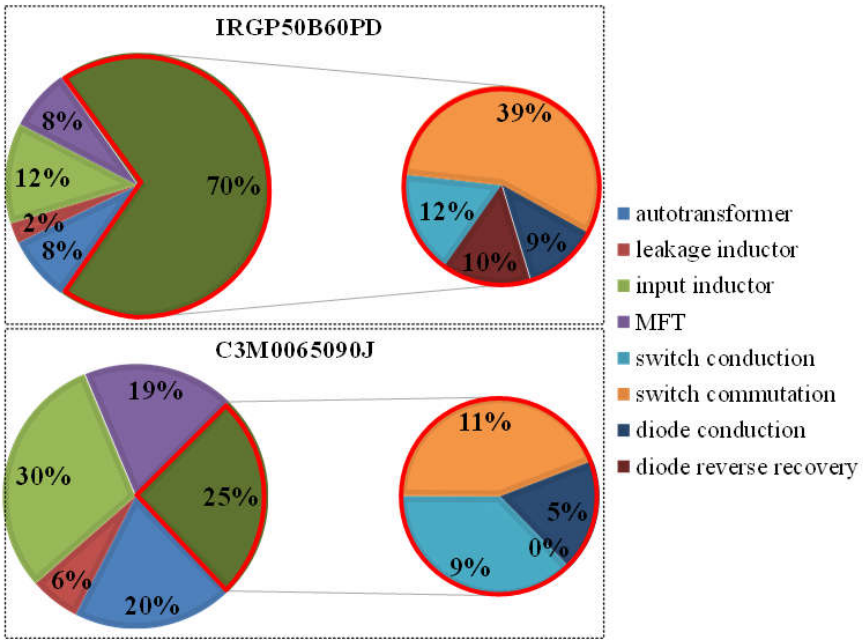
magnetic	*loss*
Leakage inductor	2.96 W
Input inductor	14.62 W
MFT	9.03 W
Autotransformer	9.57 W
Total	36.20 W

SOURCE: Author's right.

2.2.3.3 Converter efficiency

Once the determination of the semiconductor and magnetics losses are elaborated, it is possible to determinate the efficiency of the converter. Applying the IGBT IRGP50B60PD the obtained result is 89.37%, while with the silicon carbide MOSFET is 95.38%. The distribution of the presented result are shown in Figure 2.17.

Figure 2.17 – Proposed converter losses distribution



SOURCE: Author's right.

It can be noted that the IGBT used in the analysis presents 70 % of the total losses amount, while for the silicon carbide switch only 25 % is obtained. In the magnetics, it is possible to see that the input inductor is responsible for the largest amount of loss.

2.2.3.4 Comparative losses analysis

This section will present the losses analysis of the converter with both module type operating in a real railway traction system application. The study of losses consists in the analysis by using the modules presented in Figure 2.2.

In order to perform the comparative losses analysis, three additional structures have been selected for comparison purposes with the proposed one, considering the same specification and parameters stated in Table 2.15, for the same linear load condition. The adopted number of modules can be seen in Table 2.16.

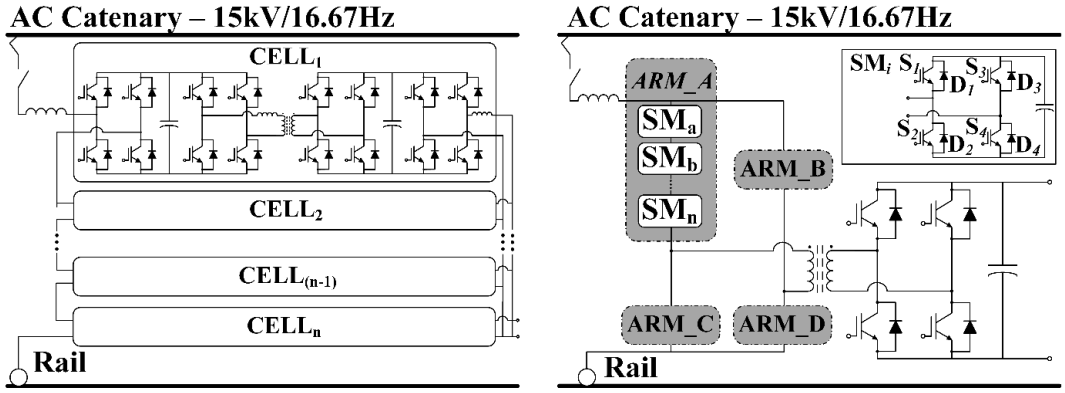
Table 2.15– Design parameters considered in the comparative losses analysis

Parameter	***Specification (Type A)***	***Specification (Type B)***
Capacitance	$C_{+i} = C_{-i} = C_{o\_i} = 2200\mu F$	$C_{1\_k} = C_{o\_k} = 2200\mu F$
MFT frequency	$f_{MFT} = 1$ kHz	$f_{MFT} = 1$ kHz
Dc link voltage	$V_{dc} = 4$ kV	$V_{dc} = 4$ kV
Number of modules	$n_{min(A)} = 12$	$n_{min(B)} = 6$
Input current ripple	$\Delta Iin = 10\%$	$\Delta Iin = 10\%$
Rated rms imput voltage	$V_{ac} = 15$ kV	$V_{ac} = 15$ kV
Output voltage	$V_o = 4$ kV	$V_o = 4$ kV
Rated outpur power	$P_o = 1.5$ MW	$P_o = 1.5$ MW
Input frequency	$f_{grid} = 16{,}67$ Hz	$f_{grid} = 16{,}67$ Hz
Switching frequency	$f_s = 1$ kHz	$f_s = 1$ kHz
Ripple voltage across the capacitors	$\Delta V_{C+i} = \Delta V_{C-i} = 10\%\ V_o$ and $\Delta V_{Co\_i} = 5\%\ V_o$	$\Delta V_{Co\_k} = \Delta V_{C1\_k} = 5\%\ V_o$

SOURCE: Author's right.

The first is a PET converter formed by cascaded multilevel active front end (AFE) circuits and parallel-output isolated dc-dc circuits, as presented in (60). The second one is known as modular multilevel line converter (M^2LC) (21), which consists in a single-stage converter formed by four identical cascaded multilevel converter arms in a full-bridge structure. Both topologies are presented in Figure 2.18. The third one is described in (61) together with the modulation functions for all aforementioned topologies.

Figure 2.18 – Generalized structure of ac-dc/dc-dc and ac-dc SSTs: (a) PET with AFE topology, (b) M^2LC Topology



SOURCE: Author's right.

The general waveforms adopted in the analysis using the proposed topology with type A is presented in (62). The switching function $\delta(\omega t)$ and its complementarity function for the primary winding current together with the sinusoidal input current I_{in} are used to obtained the current waveform of each semiconductor.

Table 2.16– Comparison result of the typical railway systems topologies

Parameter		*Proposed topology (Type A)*	*Proposed topology (Type B)*	*M²LC* (21)	*PET with AFE* (62)	*AC/DC MMC* (61)
Conduction losses [kW]		4.7	2.6	10	6.2	4.7
Switching losses [kW]		63.2	28.9	78.2	44.3	113.9
Losses per module [kW]		5.7	5.3	14.7	8.4	4.9
Total losses [kW]		67.9	31.5	88.2	50.5	118.6
Efficiency [%]		95.7	97.9	94.4	96.7	92.7
Input Inductance [mH]		1	1	10	8	0.75
Multilevel Voltage WTHD [%]		0.017	0.017	0.156	0.106	0.010
First harmonic order of the multilevel voltage		24×fs	24×fs	12×fs	12×fs	24×fs
Minimum number of modules		11	6	6	6	22
Adopted number of modules		12	6	6	6	24
Number of switches (blocking voltage)	Primary	48 (4kV)	36 (4kV)	96 (4kV)	48 (4kV)	96 (4kV)
	Secondary	48 (4kV)	24 (4kV)	4 (4kV)	24 (4kV)	96 (4kV)
Total number of inductor x designed power		12x 125 kW	6x 250 kW	1x 1.5 MW	6x 250 kW	24x 62.5 kW
Total number of auto-transformer x designed power		12x 62.5 kW	6x 250 kW	-	-	24x 31.25 kW
Total number of Transformer x designed power		12x 125 kW	6x 250 kW	1x 1.5 MW	6x 250 kW	24x 62.5 kW
Number of capacitors (max. voltage)	Primary	24 (4kV)	6 (4kV)	24 (4kV)	6 (4kV)	48 (2kV)
	Secondary	12 (4kV)	6 (4kV)	1 (4kV)	6 (4kV)	24 (4kV)

SOURCE: Author's right.

Therefore, it is possible to obtain the modulation functions by observing the behavior of the current through the switches.

In order to consider the same total silicon area for all topologies, conduction losses have been estimated as in (63) using (2.21).

$$P_{cond}(A,i) = U_{f,x} \cdot i + \frac{R_{onN} \cdot A_N}{A} \cdot i^2 \tag{2.33}$$

The commutation loss curve can be considered independent on the silicon area as stated in (63). In other words, the total number of switches in each topology is different, although they have the same silicon area.

The proposed topology considering modules type A requires at least eleven modules to modulate the input voltage due the converter contribution of $|V_{dc}/2|$ for V_{mult}. Twelve modules have been chosen to achieve a modulation index lower than 90% at the rated operating condition. The others topologies demand only six modules for the same modulation index, but the one proposed in (61), requires 24 modules.

Moreover, the proposed topology for both module types and the AC/DC MMC (61) present the best harmonic distribution for the multilevel voltage with the first amplitude seen in the 24^{th} order, thus allowing the reduction of the input filter volume, which can be evidenced by the seventh row of Table 2.16.

AC/DC MMC topology has the major disadvantage of dc input characteristics, being necessary the same number of modules to modulate the positive semicycle of the ac input voltage, which results in the double number of modules if compared with the proposed type A topology. This scenario gets even worse if compared with topology type B.

It is worth to mention that, although the proposed topologies present an autotransformer as an extra magnetic component if compared with other solutions, the WTHD of the multilevel voltage demonstrates that the input inductance value (1 mH) is way reduced compared with the others topologies (10 mH (21), 8 mH (62)), resulting in a smaller magnetic and, then, compensating the extra volume of the autotransformer.

The interleaving technique using an autotransformer allows good distribution of the current stress in the semiconductors according to the calculation of conduction losses, while the proposed converters presents the best results together with AC/DC MMC. In fact, the losses per module in this case are the second best for *Type B* topology and the third best one for *Type A* topology, since the number of modules of the AC/DC MMC is larger in relation with the ones for the proposed topologies.

The handled power of each magnetic was provided to give the idea of size magnitude in each element. The number of capacitors was also inserted in such table, together with their operating voltage conditions. Although the number of capacitors is different, the total capacitor volume requested by all topologies is the same due to low frequency component presented in single-phase systems.

Finally, it is worth to mention that the introduced converters present the best and the third best result in terms of efficiency, while the AC/DC MMC presents the lower one due the large number of switching devices. In this analysis the contribution of the magnetics for the losses is not considerate. So, the final efficiency result could vary from the presented

calculation, however the author believes that these fact would not jeopardize the proposed study and proposal.

3 DESING PROCEDURE

This chapter is dedicated to present the description and tuning of the controllers presented in the section 2.1.4, considering the proposed topology built with modules type B, as presented in Figure 2.11b. Besides, it presents the sensor configurations applied in the converter topology, as well as its signal conditioning schematics.

The specifications considered for the proposed converter design is presented in Table 3.1 as well as its design parameters.

Table 3.1– Design parameters and specifications

Parameter	***Value***	***Specification***	***Value***
Rated input voltage	220 V	Input inductance	1.57 mH
Input frequency	60 Hz	MFT series inductance	331.8 μH
Rated output power	1 kW	Magnetization inductance	27 mH
Dc link voltage (primary side)	400 V	Capacitance (primary side)	340 μH
Dc link voltage (secondary side)	400 V	Capacitance (secondary side)	470 μH
Switching frequency	20 kHz	Turns ratio	1

SOURCE: Author's right.

3.1 Sensors

To create the proper exchange of information between the power converter and the controllers, some sensors are necessary. They are responsible to generate the controlled variables feedback signal from the power converter structures. This study uses two type of sensors, voltage and current, which will be presented as follow.

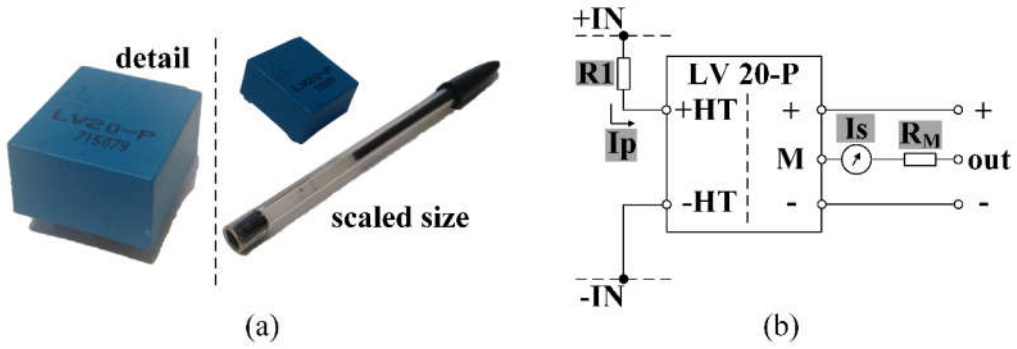
3.1.1 Voltage

To obtain the voltages measurements in the converter, isolated voltages sensors manufactured by LEM® are chosen. The selected model was the LP-20p (Figure 3.1a), due its capability to measure voltages until 500 V with galvanic isolation above 2 kV.

One sensor in each module is necessary to obtain the voltage of the dc link in the primary side of the MFT, but only one to measure the output voltage regardless the number of modules. Moreover, another one is used to obtain the ac voltage value for the synchronism circuit.

Two resistors are necessary to set the measured voltage range of this sensor, as presented in Figure 3.1b. One in series with the input terminal of the target-voltage side, R1, which should limit the terminals current around ±14 mA. The second one, R_M, is used together with the inner gain of the sensor to produce the proper output voltage level for the analogic-digital converter (ADC) in the microcontroller. The gain of the sensor is given by the ratio 2500:1000, while the input voltage A/D range is 0 to 3.3 V.

Figure 3.1 – Isolated voltage sensor: (a) physic aspect, (b) recommended circuit connections



SOURCE: Author's right.

In Table 3.2 is presented the parameterization settled for each voltage sensor used in the proposed converter.

Table 3.2– Parameterization of the applied voltages sensors

Parameter	***AC input voltage***	***DC link voltage (MFT primary side)***	***Output voltage***
Maximum input voltage (+IN and -IN)	311 V	400 V	400 V
R1	23.5 kΩ	68 kΩ	68 kΩ
Ip	13 mA	5.9 mA	5.9 mA
R_M	50 Ω	200 Ω	200 Ω
Is	33 mA	15 mA	15 mA
Calculated gain	4.8×10^{-3}	7.25×10^{-3}	7.25×10^{-3}

SOURCE: Author's right.

Since the output sensor voltage maximum values are ±1.5 V for AC voltages, it is necessary a signal conditioning circuit to offset its negative portion in 1.65 V, leaving it only with positive values. This circuit is inserted together with the filtering circuit in the used signal conditioning schematic. Such arrangement is not necessary for the other voltage sensors.

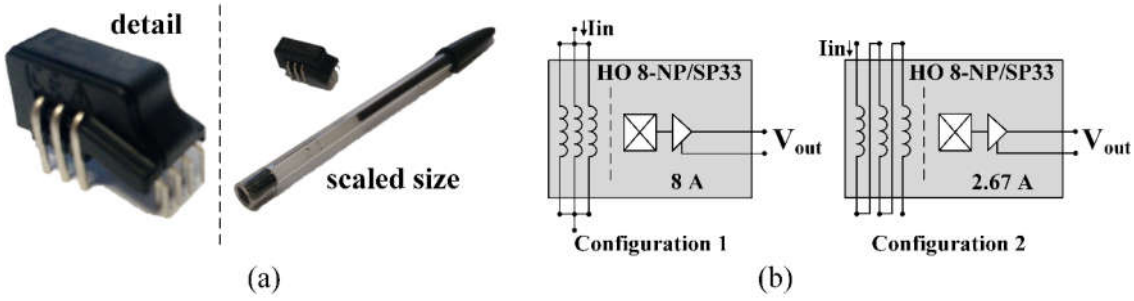
3.1.2 Current

For current measurements LEM® sensors are also used. The adopted family model is the H0-NP/SP33. The rms value of the ac current is obtained by (2.15), considering the parameters presented in Table 3.1.

$$I_{in} = \frac{P}{V_{ac}}\sqrt{2} = \frac{1000}{220} = 4.55A \tag{3.1}$$

Thus, the sensor used is the model HO 8-NP/SP33 (Figure 3.2a), which allows two different connections, as presented in Figure 3.2b. The first one, series associated coils, measures rms current until 2.67 A, while the second one, with paralleled coils, measures until 8 A.

Figure 3.2 – Isolated current sensor: (a) physic aspect, (b) recommended circuit connections



SOURCE: Author's right.

Configuration 1 is used to obtain the current in the inductances placed in parallel with the primary and secondary terminals of the MFT, respectively. Then the current waveform proportional with the magnetization current of the MFT is obtained. Besides, the configuration 2 is used to obtain the rms current in the input inductance filter. The inner gain of this sensor is 0.0575 V/A and its output voltage range is already set in 0 to 3.3 V, as default.

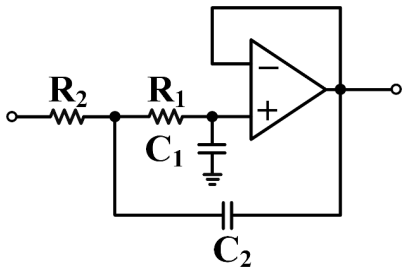
3.2 Anti-aliasing filter

A low-pass second order Butterworth filter is used to avoid aliasing in the feedback signals. Its circuits is presented Figure 3.3.

With the desired cutoff frequency specified, as well as considering a damping factor ζ=0.7 and knowing the value of C_2, it is possible to establish the capacitance of C_1 by (2.16).

$$C_1 = \frac{C_2}{\xi^2} \tag{3.2}$$

Figure 3.3 – Second order Butterworth filter circuit



SOURCE: Author's right.

It is considered that R_1 and R_2 are equal to simplify the design, allowing to express their resistance value by (2.17).

$$R = \frac{1}{\omega_c \sqrt{C_1 \cdot C_2}} \tag{3.3}$$

Table 3.3 presents the values calculated for each filter used in the prototype.

Table 3.3– Parameterization of the applied filters

Parameter		***DC link voltage (MFT primary side)***	***Output voltage***	***AC input current***	***Magnetizing current***
Cutoff frequency	designed	10 kHz	10 kHz	10 kHz	5 kHz
	obtained	10.55 kHz	10.55 kHz	10.55 kHz	4.94 kHz
R_1		2.2 kΩ	2.2 kΩ	2.2 kΩ	4.7 kΩ
R_2		2.2 kΩ	2.2 kΩ	2.2 kΩ	4.7 kΩ
C_1		10 nF	10 nF	10 nF	10 nF
C_2		4.7 nF	4.7 nF	4.7 nF	4.7 nF

SOURCE: Author's right.

3.3 Controllers designs

This section presents the description of the control loop designs applied in the proposed topology. The methodology adopted consists in the k factor control method (64) considering type II controller structures. The controllers are designed in the s-plane and then discretized to the z-plane by Tustin's approximation to be included in the microcontroller code.

3.3.1 Voltage DC link controller

The dc link voltage controller is built in a cascaded loop with the input current control loop. Then, it is necessary to obtain the transfer function related with dc link voltage and the ac input current, which is given by:

$$H_z(s) = \frac{R_o}{R_o \cdot C_{1\_k} \cdot s + 1}, \tag{3.4}$$

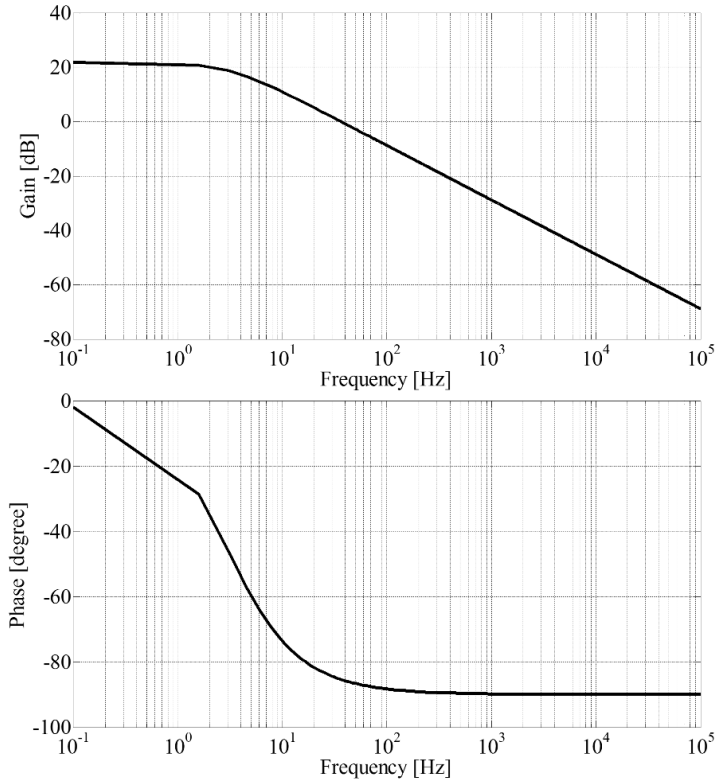
where R_o is the rated resistive load and C_{1_k} is the capacitor in the power module SM_{pri_k}.

Since the crossover frequency in this type of control loop is usually at low values, it is possible to use this transfer function as an approximation of the real model with satisfactory behavior. Moreover, the inner current loop is considered as a gain, since its crossover frequency is much larger than the voltage's one. Besides, the open loop transfer function should also considers the voltage sensor gain, being obtained by:

$$OLTF_v(s) = H_v(s).\frac{H_v}{H_i} \tag{3.5}$$

where, H_v is the voltage sensor gain and H_i is the considered the gain of the input current control loop. The bode diagram for both gain and phase of the $OLTF_v$ is presented in Figure 3.4.

Figure 3.4 – Bode diagram of $OLTF_v$



SOURCE: Author's right.

It is worth to mention that the ADC gain can be neglected, since this control loop provides the reference signal for the cascaded input current control loop, where such gain is

considered, as presented in Figure 2.11b. Moreover, crossover frequency of 10 Hz and a desired phase margin of 60 degrees is chosen.

The next step from the k factor control method is to calculate the required phase boost by:

$$Boost = M - P - 90, \tag{3.6}$$

where, M is de desired phase margin and P is the modulator phase shift, all values expressed in degrees. Since, all controllers in the proposed topology required a boost lower than 90º, (3.6) can be applied in all of their designs control loop.

The calculated boost is applied in (3.7) to obtain the k factor, which is used to obtain the frequency of the pole and the zero of the controller with the selected crossover frequency and desired phase margin. The zero and pole frequencies are obtained by (3.8) and (3.9), respectively.

$$k = tg\left(\frac{\alpha}{2} + 45°\right) \tag{3.7}$$

$$\omega_z = \frac{\omega_c}{k} \tag{3.8}$$

$$\omega_p = \omega_c . k \tag{3.9}$$

Now, it is necessary to calculate the required gain of the controller function to guarantee the desired characteristics. It is possible to calculate such gain using (3.10).

$$G_c = \frac{1}{\left|OLTF\left(\omega_c\right)\right|} \tag{3.10}$$

Once, all parameters of the controller function are determined, it is time to obtain its expression, which is given by (3.11).

$$C\left(s\right) = G_c . \omega_p \frac{s + \omega_z}{s + \omega_p} \tag{3.11}$$

Finally, with the controller defined, the next step is to use Tustin's approximation to obtain the z-plane expression of the controller. The Tustin's approximation is given by (3.12), where z is the frequency variable in the z-plane and T_a is the sample period of the discretization.

$$s = \frac{2}{T_a} . \frac{z - 1}{z + 1} \tag{3.12}$$

The z-plane controller expression is achieved applying (3.12) in (3.11), which results in (3.13).

$$\frac{U(z)}{E(z)} = C(z) = \frac{G_c.\omega_p.T_a}{\omega_z}.\frac{(\omega_z.T_a+2).z^2+2.\omega_z.T_a.z+(\omega_z.T_a-2)}{(4.+2.\omega_p.T_a).z^2-8.z+(4-2.\omega_p.T_a)} \tag{3.13}$$

Then, it is possible to relate the controller output with the error input by a difference equation expressed by (3.14), where its coefficients are represented by (3.15) to (3.19).

$$U(z) = a_1.U(z-1)+a_2.U(z-2)+b_0.E(z)+b_1.E(z-1)+b_2.E(z-2) \tag{3.14}$$

$$a_1 = \frac{4}{2+T_a.\omega_p} \tag{3.15}$$

$$a_2 = \frac{T_a.\omega_p-2}{2+T_a.\omega_p} \tag{3.16}$$

$$b_0 = \frac{G_c.\omega_p.T_a.(2+T_a.\omega_z)}{2.(2+T_a.\omega_p)} \tag{3.17}$$

$$b_1 = \frac{G_c.\omega_p.T_a^{\,2}.\omega_z}{2+T_a.\omega_p} \tag{3.18}$$

$$b_2 = \frac{G_c.\omega_p.T_a.(T_a.\omega_z-2)}{2.(2+T_a.\omega_p)} \tag{3.19}$$

With the aforementioned methodology, it is possible to determine the values of the voltage controller coefficients, which are summarized in Table 3.4.

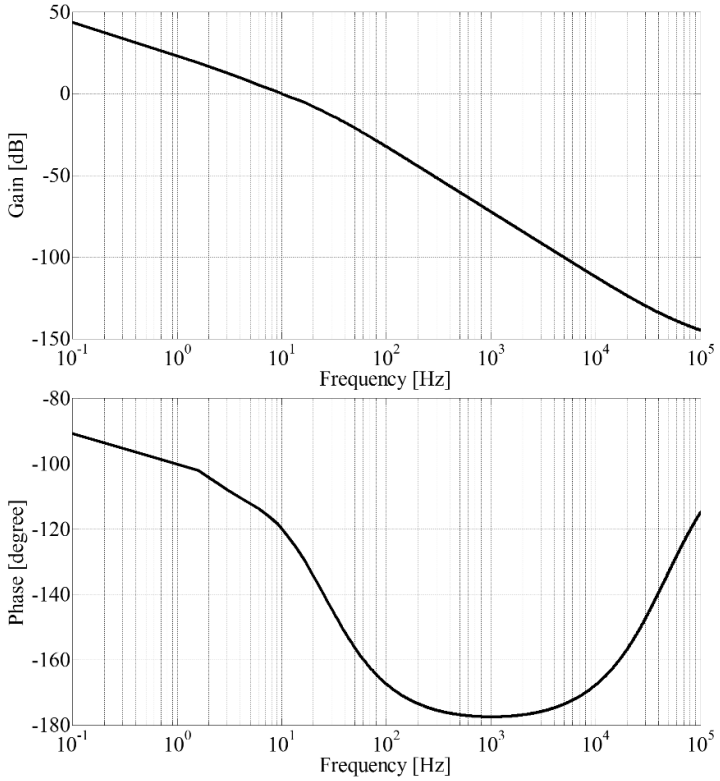
Table 3.4– Parameters of the dc link voltage controller

Parameter		***Value***
required phase boost	α_v	43.681°
k factor	k_v	2.338
zero frequency	ω_{zv}	26.877 rad/s
pole frequency	ω_{pv}	146.885 rad/s
controller required gain	G_{cv}	0.287
difference equation coefficients	a_{1v}	1.998
	a_{2v}	-0.998
	b_{0v}	3.507×10^{-4}
	b_{1v}	1.571×10^{-7}
	b_{2v}	-3.506×10^{-4}

SOURCE: Author's right.

In Figure 3.5 is presented the Bode diagram of the control loop tuned in the desired specification.

Figure 3.5 – Bode diagram of $OLTF_v$ compensated



SOURCE: Author's right.

3.3.2 Input current controller

To regulate the shape of the input current, the input current control loop uses, as its reference signal, the control signal from dc link voltage loop control together with the sinusoidal shape phase from PLL block. The transfer function for this loop is given by (3.20), where V_o is the dc link voltage and L_{in} is the input inductance filter given by (2.11).

$$G_i(s) = \frac{V_o}{L_{in}.s} \tag{3.20}$$

This controller regulates the modulation index of the proposed topology. In the controllers design, it is necessary to consider the gains of the current sensor and ADC, as well as, the one from the modulator. The gain of the current sensor is presented in section 3.1.2, while the gains from the ADC and the modulator are described by (3.21) and (3.22), where V_{Fad} is reference voltage of the ADC, V_{ppm} is the maximum value of the modulator input, and F_m is the modulator gain, respectively.

$$K_{ad} = \frac{2^{bits} - 1}{V_{Fad}} \tag{3.21}$$

$$F_m = \frac{1}{V_{ppm}} \tag{3.22}$$

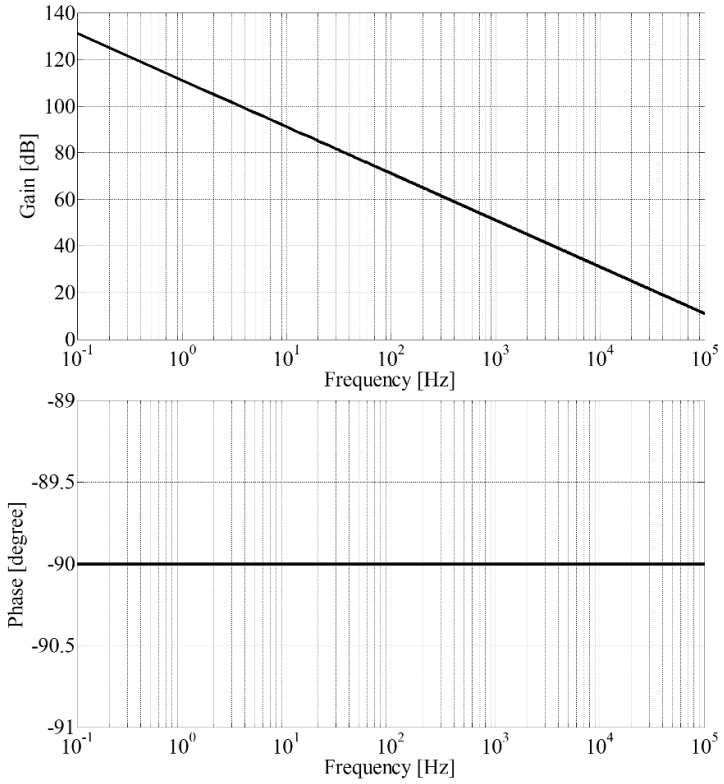
The modulator is conceived to operate in a range of -2 to 2, which implies in a V_{ppm} = 4.

The open loop transfer function of the current controller is expressed by (3.23), considering all mentioned gains.

$$OLTF_i(s) = G_i(s).H_i.K_{ad}.F_m \tag{3.23}$$

Figure 3.6 presents the Bode diagram of $OLTF_i$ for gain and phase behaviors, providing the initial assumption for the k factor control methodology, similarly as in the last section.

Figure 3.6 – Bode diagram of $OLTF_i$



SOURCE: Author's right.

It is possible to note the first-order behavior expressed by (3.20), since this expression is an approximated model for high frequency operation. Although the complete model didn't present pole at zero, the adopted model demonstrates good behavior in high frequencies operations.

The same steps made in the dc link voltage loop are taken here as well. Therefore, it is selected a crossover frequency of 1.3 kHz and 60º of desired phase margin. Table 3.5 presents the parameters resulted from the k factor control methodology with Tustin's approximation as discretization method.

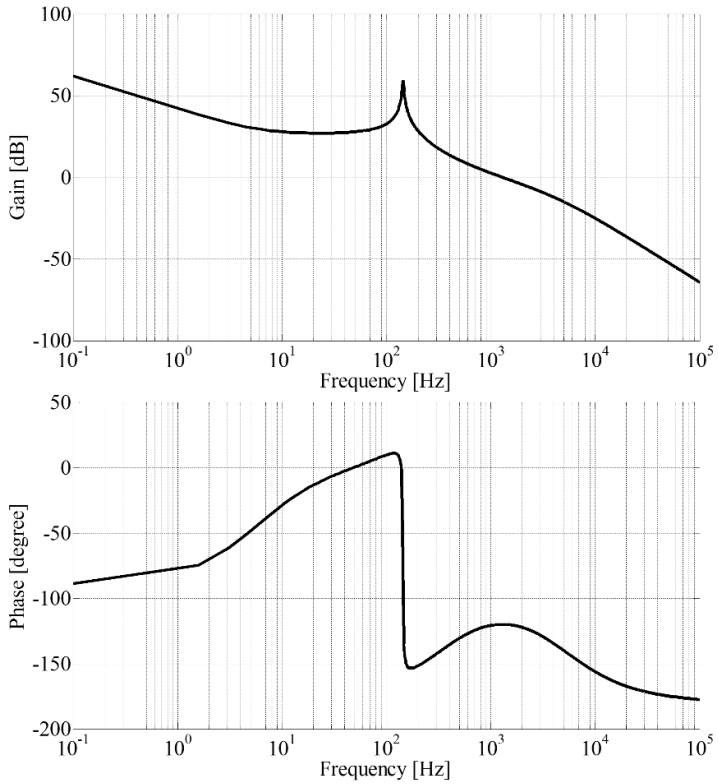
Table 3.5– Parameters of the input current controller

Parameter		***Value***
required phase boost	α_i	60.097º
k factor	k_i	3.745
zero frequency	ω_{zi}	2,181 rad/s
pole frequency	ω_{pi}	30,590 rad/s
controller required gain	G_{ci}	3.018×10^{-3}
difference equation coefficients	a_{1i}	1.594
	a_{2i}	-0.594
	b_{0i}	6.242×10^{-4}
	b_{1i}	2.229×10^{-5}
	b_{2i}	-6.019×10^{-4}

SOURCE: Author's right.

Figure 3.7 presents the gain and phase behavior for the compensated system. It is possible to note the desired behavior for the input current control loop.

Figure 3.7 – Bode diagram of $OLTF_i$ compensated



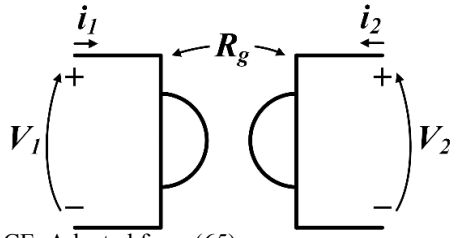
SOURCE: Author's right.

3.3.3 Output voltage controller

To specify the output control loop, it is necessary a transfer function that relates the output voltage with the phase shift angles between the primary and secondary side of the MFT. This function can be obtained applying gyrator theory (65).

Gyrator is considered the fifth linear networks element and it is composed by two ports interconnected by a constant denominated as gyration resistance, R_g, as presented in Figure 3.8.

Figure 3.8 – Proposed symbol for the ideal gyrator



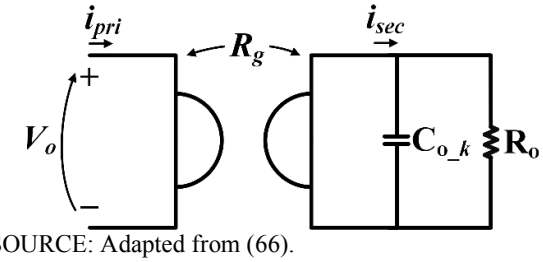
SOURCE: Adapted from (65).

The work presented is (66) uses the gyrator theory to represent the DAB converter, with R_g expressed by (3.24).

$$R_g = \frac{1}{2.\pi.f_s.L_{disp\_k}}.\Phi_k.\left(1-\frac{|\Phi_k|}{\pi}\right) \tag{3.24}$$

This model can be used to find the required transfer function for the tuning of the output voltage control loop. Figure 3.9 present the equivalent circuit used to extract such transfer function.

Figure 3.9 – Equivalent circuit of the load port



SOURCE: Adapted from (66).

Then, the transfer function which relates the secondary voltage with the phase shift angle in the MFT is expressed by (3.25).

$$V_{\text{sec}}(s) = \frac{V_o}{2.\pi.f_s.L_{disp\_k}}.\Phi_k.\left(1-\frac{|\Phi_k|}{\pi}\right).\frac{R_o}{R_o.C_{o\_k}.s+1} \tag{3.25}$$

Next, the transfer function used in the control methodology is archived by making a linearization in (3.25) with the adopted operational point, resulting in (3.26), where Φ_o is the phase shifted angle by the rated output power in the load port and L_{leak} is the series inductance of the proposed converter expressed by (2.20).

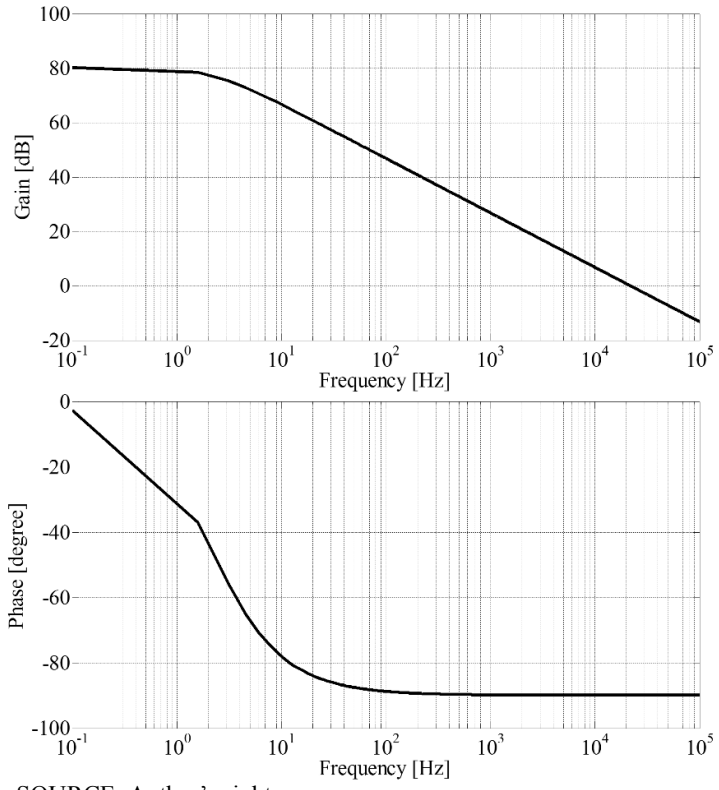
$$G_{vout}(s) = \frac{V_o}{2.\pi.f_s.L_{leak\_k}}.\left(1 - \frac{2.|\Phi_o|}{\pi}\right).\frac{R_o}{R_o.C_{o\_k}.s+1} \tag{3.26}$$

Finally, the transfer function is arranged with the gains of the voltage sensor and the ADC to obtain the open loop transfer function presented in (3.27).

$$OLTF_{vout}(s) = K_{ad}.H_v.G_{vout}(s) \tag{3.27}$$

The k factor control methodology is used considering crossover frequency of 500 Hz with a desired phase margin of 60º. The behaviors of gain and phase of the $OLTF_{vout}$ is presented in Figure 3.10.

Figure 3.10 – Bode diagram of $OLTF_{vout}$



SOURCE: Author's right.

Table 3.6 presents the parameters resulted from the k factor control methodology with Tustin's approximation as discretization method, while Figure 3.11 presents the gain and

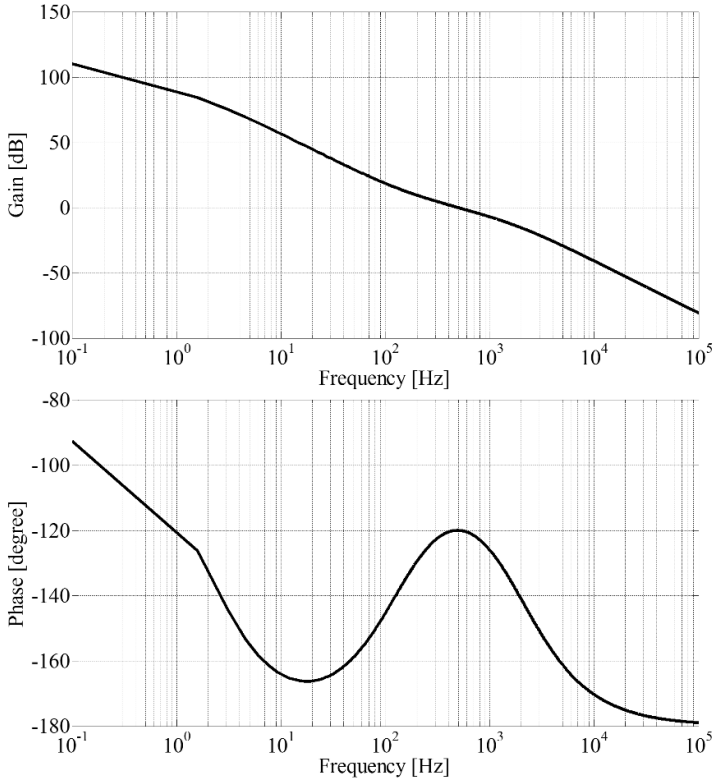
phase behavior for the compensated system. It is possible to note the desired behavior for the output voltage control loop.

Table 3.6– Parameters of the output voltage controller

Parameter		***Value***
required phase boost	α_{vout}	59.757º
k factor	k_{vout}	3.701
zero frequency	ω_{zvout}	848.918 rad/s
pole frequency	ω_{pvout}	11,630 rad/s
controller required gain	G_{cvout}	0.023
difference equation coefficients	a_{1vout}	1.823
	a_{2vout}	-0.823
	b_{0vout}	2.016×10^{-3}
	b_{1vout}	2.833×10^{-5}
	b_{2vout}	-1.988×10^{-3}

SOURCE: Author's right.

Figure 3.11 – Bode diagram of $FTLA_{vout}$ compensated



SOURCE: Author's right.

3.3.4 DC link voltage balancing controller

This control loop, as mentioned in section 2.1.4, is responsible for the balancing of the dc link voltage in each module of the proposed converter. In order to do that, the control

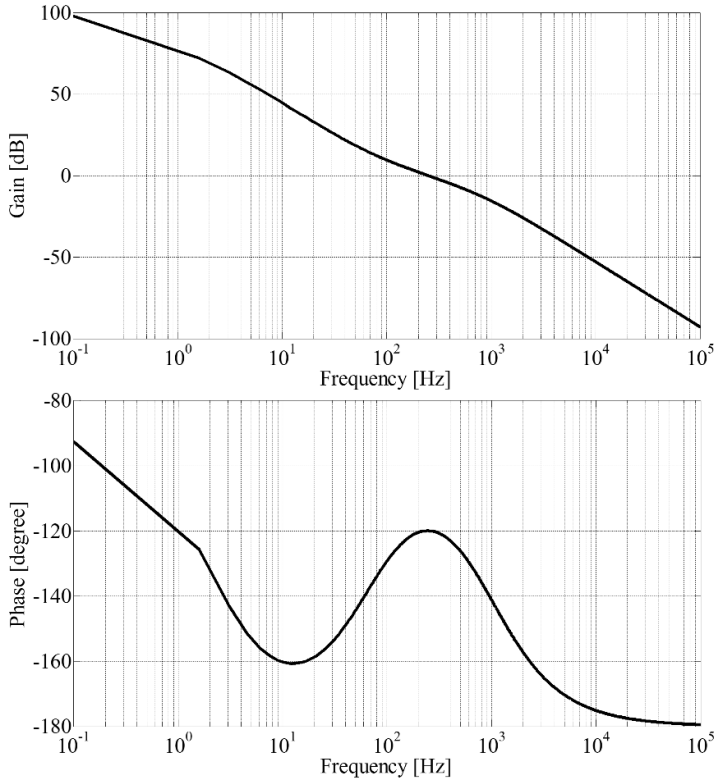
loop should works slower than the dc link voltage loop, resulting in the correct regulating of the dc link.

Then, the dc voltage link balancing control loop uses the similar control structure as the one presented in the output voltage control.

The difference is in the feedback signal where it uses the dc link voltage of each module in its respective control loop instead of the average value of all modules combined. However, this signal is used as reference in this control loop, as presented in Figure 2.11b.

Thus, the crossover frequency selected is 250 Hz with a desired margin of 60º. Figure 3.12 presents the gain and phase behavior for the compensated system. It is possible to note the desired behavior for the dc link balancing control loop.

Figure 3.12 – Bode diagram of $OLTF_{vdc\_banl}$ compensated



SOURCE: Author's right.

Table 3.7 presents the parameters resulted from the k factor control methodology with Tustin's approximation as discretization method.

Table 3.7– Parameters of the dc link balancing voltage controller

Parameter		***Value***
required phase boost	α_{vdc_banl}	59.515º
k factor	k_{vdc_banl}	3.67
zero frequency	ω_{zvdc_banl}	428.028 rad/s
pole frequency	ω_{pvdc_banl}	5,765 rad/s
controller required gain	G_{cvdc_banl}	0.011
difference equation coefficients	a_{1vdc_banl}	1.908
	a_{2vdc_banl}	-0.908
	b_{0vdc_banl}	5.214×10^{-4}
	b_{1vdc_banl}	3.706×10^{-6}
	b_{2vdc_banl}	-5.177×10^{-4}

SOURCE: Author's right.

4 EXPERIMENTAL SETUP AND RESULTS

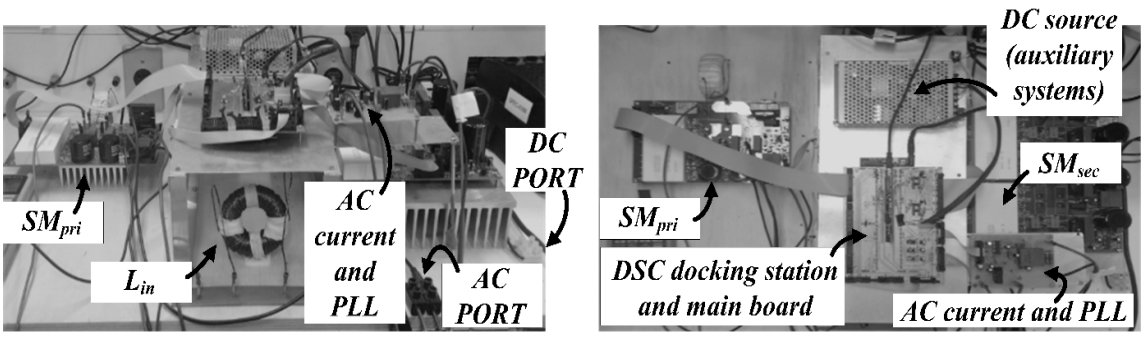
This chapter presents the experimental setup and its operational behavior, as well as, the results of the simulation models. The prototypes and simulation model specifications are shown in Table 3.1 in the controller design procedure. Firstly, the single-module converter with type B module is built and tested in the test rig. Then, the same it is done with the two-module configuration, in order to validate the multi-module structure of the proposed power converter. Both prototypes are addressed in the following sections.

4.1 Prototypes description

Figure 4.1 shows the prototype considering the single-module structure. The test rig consists in the submodules SM_{pri} and SM_{sec}. The PCB for each submolude is designed with the driver from SEMIKRON®, model SKHI 61(R). The voltages and current sensors are also placed in the PCBs with the configuration presented in the last chapter.

A dc power source to feed the auxiliary circuits, such as, buffers, drivers and filters, it is used as well. The model selected is the NET-75C by MEAN WELL®, since it provides all the dc voltages levels used in the test rig.

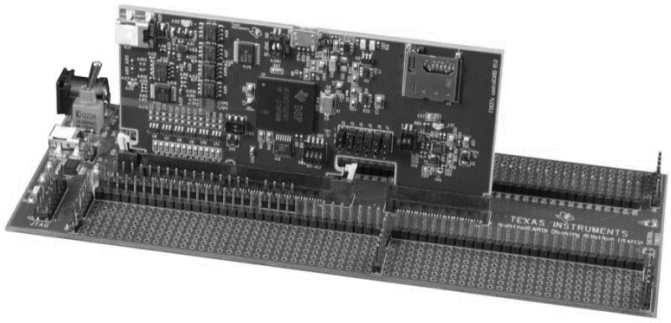
Figure 4.1 – Single-module structure prototype: (a) front view, (a) superior view



SOURCE: Author's right.

The microcontroller applied in the experimental setup is the TMS320F28377D from Texas Instruments®, as presented in Figure 4.2.

Figure 4.2 – TMDSDOCK28377D Experimenter's kit

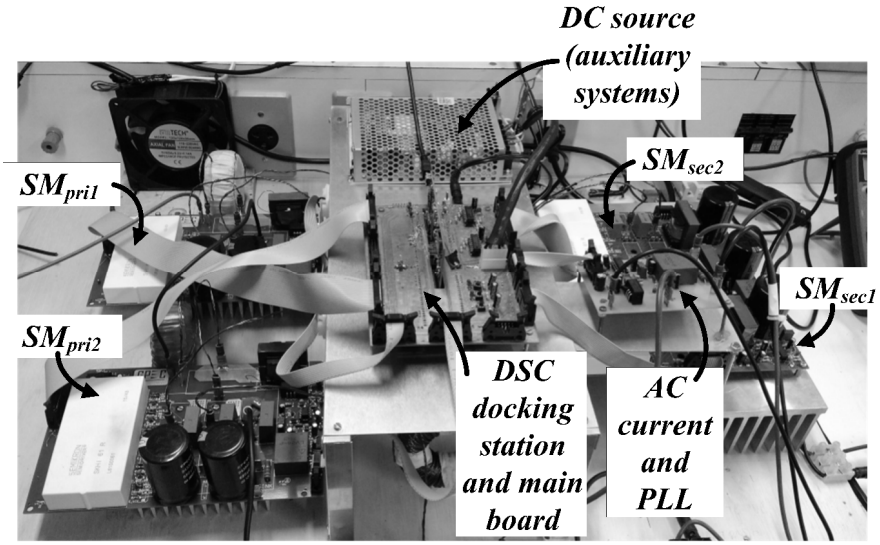


SOURCE: Adapted from (67).

This device, has a dual-core structure of 32-bit processor from Delfino family. The dual-core architecture is important due the space vector modulation algorithm implementation which occurs in one core, while the control routine runs in the other.

Figure 4.3 presents the prototype built with the two-module structure configuration. It is possible to note that the modularity of the proposed structure facilitates the constructions and specifications of the prototype.

Figure 4.3 – Two-module structure prototype



SOURCE: Author's right.

Table 4.1 presents the main devices used in the proposed topology. Due the modularity of the proposed converter, such list tends to remains with the same kind of components, although their numbers should increase as the number of module does.

Table 4.1 – Mainly devices applied in the experimental setup, considering the two-module configuration

Device	***Model***	***Qtd.***	***Specification***
Discrete IGBT (IR)	GP50B60PD1	24 und.	600 V/33 A
Driver (SEMIKRON)	SKHI 61(R)	4 und.	—
Dc link Capacitors (primary side) (C_{1_k}=340 µF/800 V)	B43304-H2687-M	4 und.	680 µF/450 V
	R75-MKP	6 und.	0.22 µF/1 kV
Dc link Capacitors (secondary side) (C_{o_k}=940 µF/450 V)	B43503-S5477-M91	2 und.	470 µF/450 V
	R75-MKP	2 und.	0.1 µF/1 kV
Current sensor (LEM)	HO 8-NP/SP33	5 und.	8 A
Voltage sensor (LEM)	LV 20-P	4 und.	10-500 V
Ferrite Toroid Cores (Magmattec)	MMT002T4416	2 und.	—
	MMT139T6325	4 und.	—
Iron dust Cores (Magmattec)	MMT034T7713	1 und.	—

SOURCE: Author's right

4.2 Simulation and experimental results

This section is dedicated to present the steady and dynamic behaviors of the proposed converters either in simulation and experimental tests, such as: steady-state and power flow inversion.

The prototypes are built considering the parameters from Table 3.1 and the controllers tuning presented in the last chapter. It is worth to mention that the same controllers tuning is used in both simulation and experimental tests.

The results concerned with the power converters using type A module are presented in (54), while the ones considering the single- and two-module configurations of the proposed converter, both with modules type B, are presented and discussed as follows.

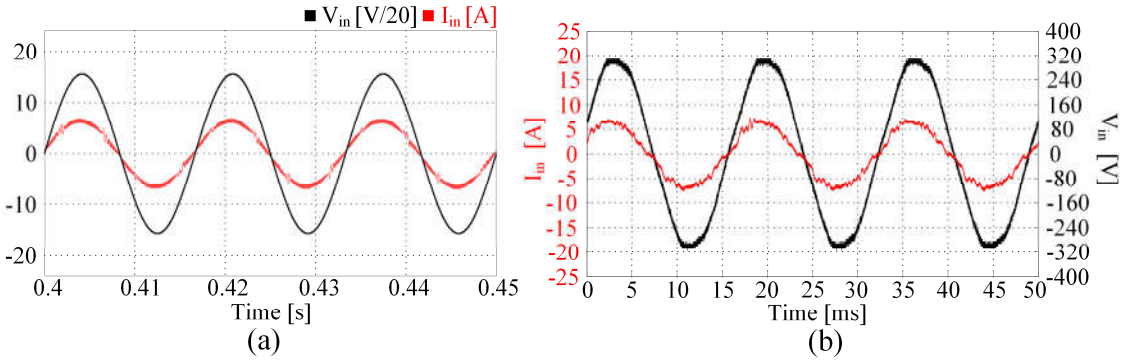
4.2.1 Steady-state behavior

This section focus in the presentation of the steady-states behaviors of the proposed topologies, considering the single- and two-module structures.

4.2.1.1 Single-module power converter structure

The rms sinusoidal input voltage is maintained at V_{ac}=220 V and 60 Hz thus resulting in 1 kW, while some results are presented through Figure 4.4 to Figure 4.7.

Figure 4.4 – Single-module structure steady-state behavior for the input voltage and current: (a) simulation results, (b) experimental results

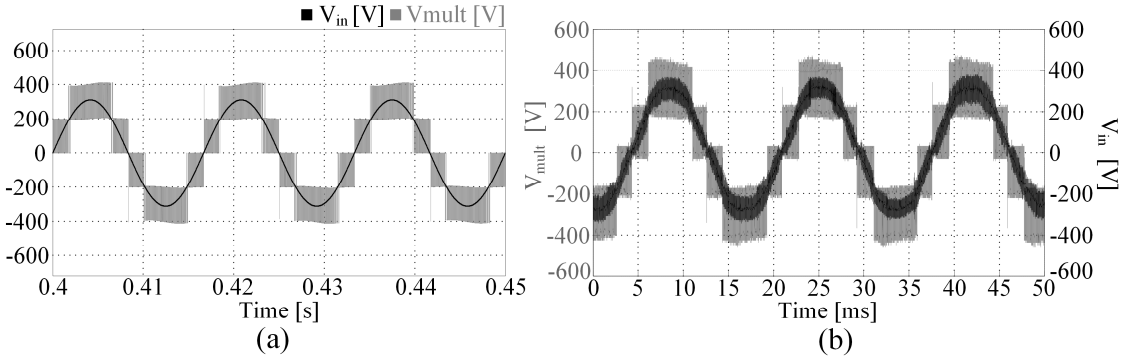


SOURCE: Author's right.

The waveforms regarding the input voltage and current is shown in Figure 4.4a for the simulations analysis. The current remains sinusoidal, whose rms value is 4.5 A with THD of 5.98%, while the power factor is 0.995. Figure 4.4b presents the experimental behavior of the same variables, where THD of 7.9% and power factor of 0.982, it were found.

Figure 4.5 shows the multilevel voltage across the input terminal of the single-module converter structure. It is possible to see the expected five voltage levels from (2.6).

Figure 4.5 – Single-module structure steady-state behavior for the multilevel voltage: (a) simulation results, (b) experimental results



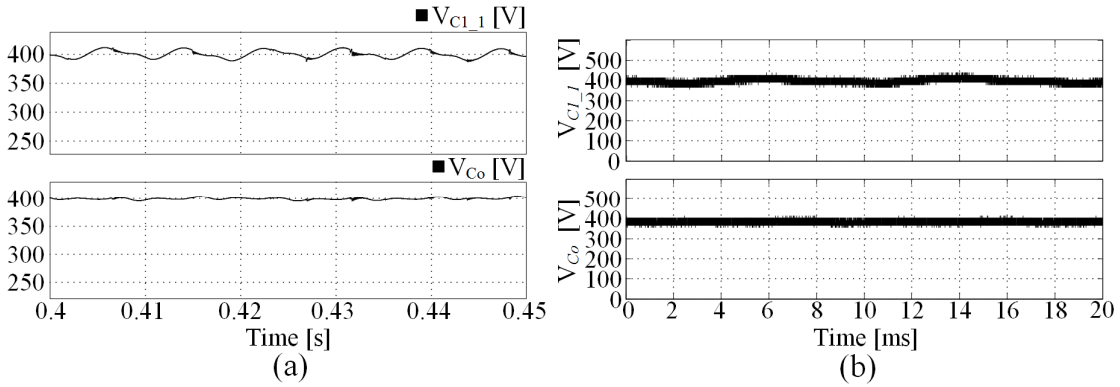
SOURCE: Author's right.

Figure 4.5a presents three grid cycles of the multilevel voltage for the simulation analysis. It possible to see that the expected five voltage levels are achieved. Similar behavior is note in Figure 4.5b for the experimental test, as well. Then, it is possible to conclude that the vector modulation algorithm was implemented correctly in both tests, in term of the modulated voltage.

Figure 4.6 presents the behavior of the voltages across capacitors C_{1_1} and C_o. It is possible to notice the satisfactory actuation of the dc link voltage control loop as V_{C_1}=400 V is

achieved in Figure 4.6a and Figure 4.6b with the results for simulation and experimental tests, respectively.

Figure 4.6 – Single-module structure steady-state behavior for the voltages across capacitor C_{1_1} and C_o: (a) simulation results, (b) experimental results

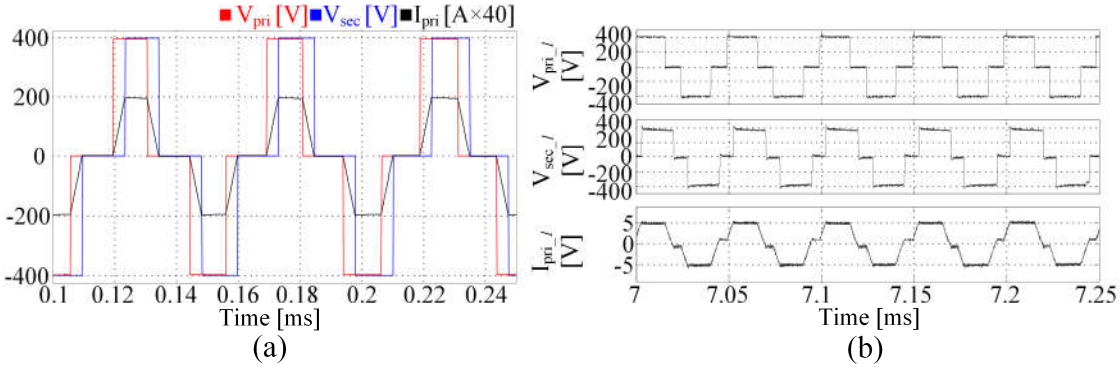


SOURCE: Author's right.

Still in the same figure, it is, also, possible to see the correct behavior of the output voltage, since the voltage across the capacitor C_o is regulated by the output control loop in V_{out} = 400 V.

In Figure 4.7, it is presented the steady-state behavior of the voltage across the MFT. Figure 4.7a presents the simulations behaviors, while the Figure 4.7b presents the experimental ones. It is possible to see the correct performance of the space vector modulator, since it is providing the multilevel capability to the input terminals of the converter as the medium frequency operation for the MFT is archived.

Figure 4.7 – Single-module structure steady-state behavior for the voltages across the MFT and the current, as well: (a) simulation results, (b) experimental results

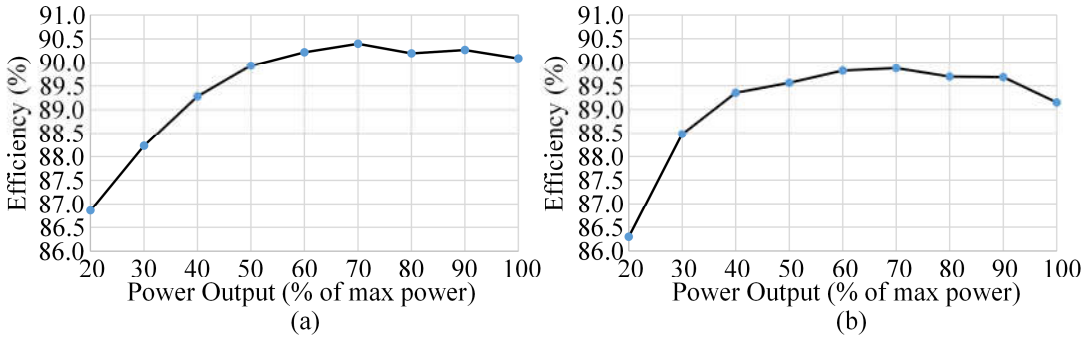


SOURCE: Author's right.

Three switching periods are considered to analysis the medium frequency behavior of the MFT variables in Figure 4.7. It is possible to note that V_{pri} and V_{sec} are phase shifted by Φ, to obtain the power flow in the terminal of the MFT. Finally, the current through the series inductor is also presented in Figure 4.7, where its correct correlation with the MFT voltages is noted.

The Graph 4.1 presents the efficiency curves of the single-module power converter structure, considering both the rectification and inversion modes.

Graph 4.1– Single-module experimental efficiency: (a) rectification mode (b) inversion mode



SOURCE: Author's right

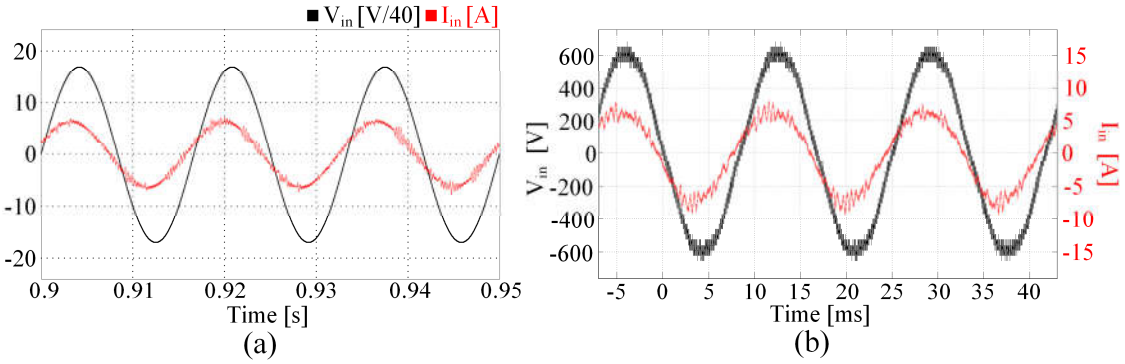
In Graph 4.1a it is possible to see the rectification mode behavior, which has the maximum efficiency point of 90.4%, while at the rated power relays in 90.1%. The results for reversion mode is presented in Graph 4.1b, where the maximum efficiency point is 89.87% and about 89% is noted in the rated power operation.

4.2.1.2 Two-module power converter structure

The steady-state results with two-module structure are presented considering the parameters presented in Table 3.1, however with V_{ac}=440 V and 60 Hz thus resulting in 2 kW (1 kW per module), while some results are presented through Figure 4.8 to Figure 4.13.

The first result regards the steady-state behavior of the ac current in the input filter. presents, such variable behavior for simulation and experimental steady-state condition. It is possible to see a sinusoidal waveform shape, resulting in rms value of 4.5 A with THD of 10.77%, while the power factor is 0.941, for simulations tests presented in Figure 4.8a. Figure 4.8b presents the experimental behavior of the same variable, where THD of 7.5% and power factor of 0.946, it were found.

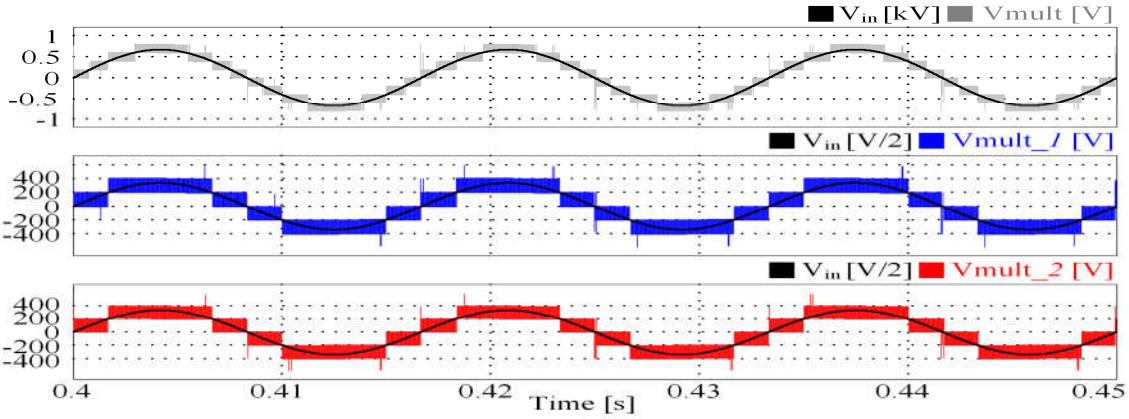
Figure 4.8 – Two-module structure steady-state behavior for the ac current in the inductive filter: (a) simulation results, (b) experimental results



SOURCE: Author's right.

The multilevel voltages of each module, as well as the resulting multilevel voltage, are presented in Figure 4.9. The first graph presents the resulting multilevel voltage, V_{mult}, which according with (2.6) shows the expected nine levels.

Figure 4.9 – Two-module structure steady-state behavior for the multilevel voltages in the simulation model

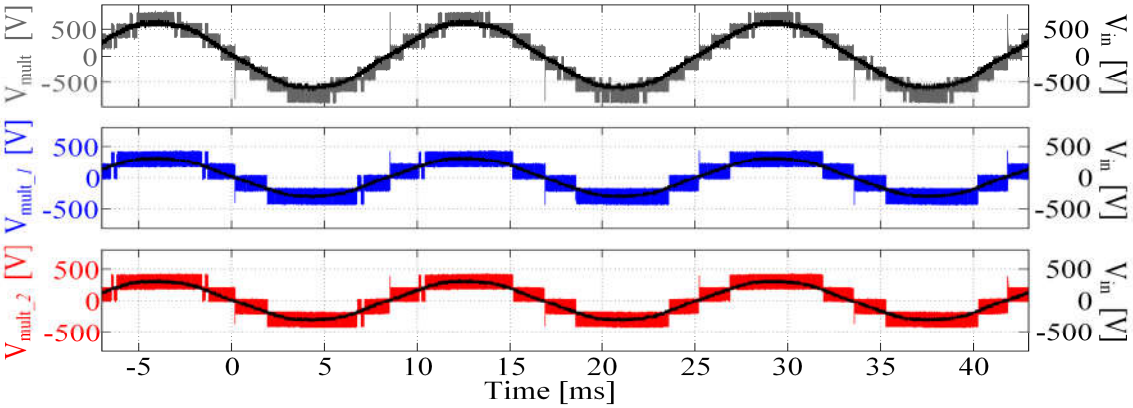


SOURCE: Author's right.

The second graph exhibits the five-level voltage in the input terminal of module 1 and the third one shows the five-level voltage in module 2. With these results it is possible to note the correct operation of the space vector modulator in the simulation model in terms of to provide multilevel voltages for each modules, while the resulting multilevel voltage is composed by four more voltage levels.

Figure 4.10 presents the behavior of the same variables aforementioned, however with experimental results. It is possible to see very similar behaviors compared with the ones in Figure 4.9, as the first graph presents the expected nine levels multilevel voltage, while five-level voltage can be noted in each modules.

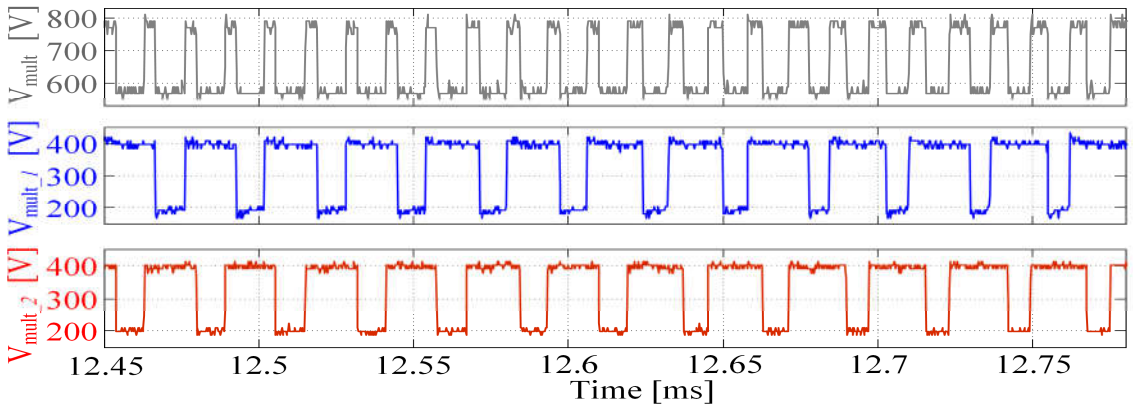
Figure 4.10 – Two-module structure steady-state behavior for the multilevel voltages in the experimental test



SOURCE: Author's right.

In Figure 4.11, it is presented the detail of the phase deposition between the multilevel voltages in each module of the power converter structure. It is possible to see the phase shift of 90º, expected from (2.3), between such voltages, as well as, the doubled frequency operation of the resulting multilevel voltage, V_{mult}.

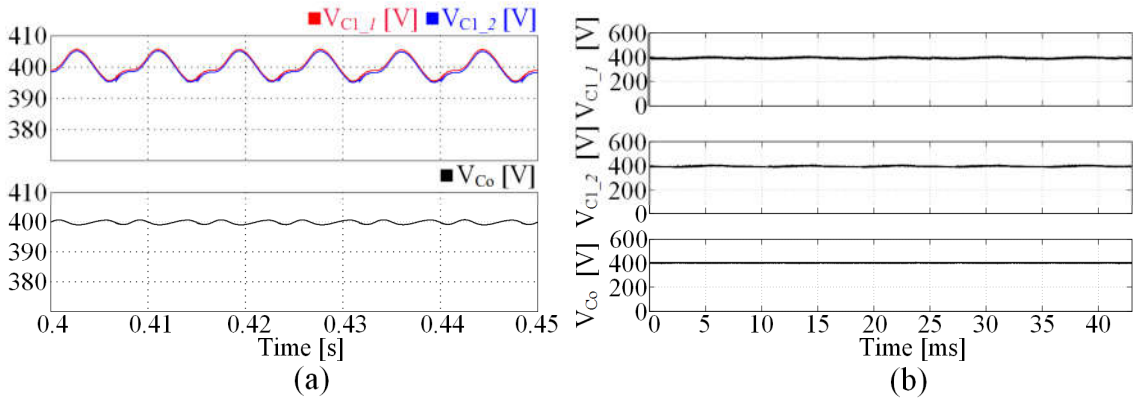
Figure 4.11 – Detailed two-module structure steady-state behavior for the multilevel voltages in the experimental test



SOURCE: Author's right.

The dc voltages are presented by Figure 4.12, where Figure 4.12a exhibits the dc link voltages in the simulation model. It is possible to note the regulation of all the dc voltages at the primary side of the MFT as a result of the dc link voltage control loop, since the dc voltages are regulated in 400 V of average value, for each module. The output voltage is, also, possible to see the good regulation of the output voltage control loop, as its value remains 400 V.

Figure 4.12 – Two-module structure steady-state behavior for the dc voltages in the simulation and experimental tests

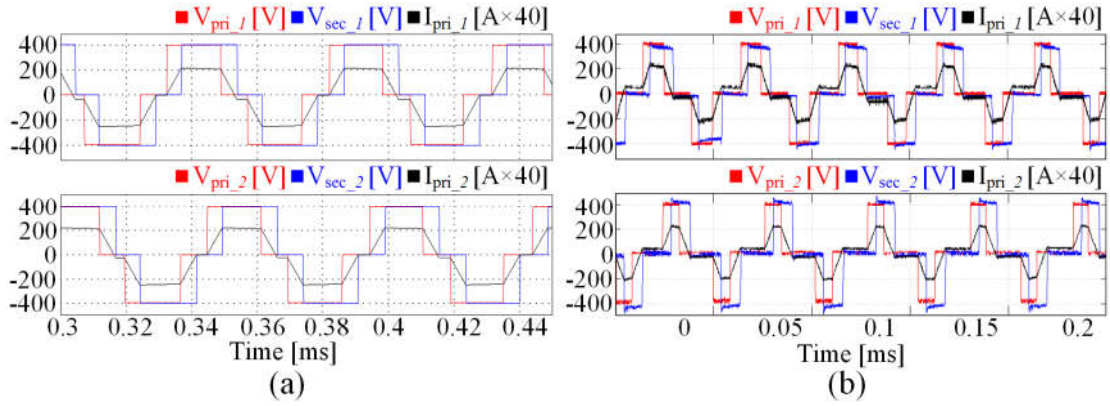


SOURCE: Author's right.

Figure 4.12b presents the experimental results for the same dc voltages. The regulation of such voltages are, also, archived in the experimental set up, as it is possible to see the average value of 400 V in the waveforms.

In Figure 4.13 is presented the waveforms of the voltages across the MFT terminals for each module. Figure 4.13a presents the waveforms regarding the results from the simulation, while the ones from experimental set up are presented in Figure 4.13b.

Figure 4.13 – Two-module structure steady-state behavior for the MFT voltages and its primary side current in the simulation and experimental tests



SOURCE: Author's right.

It is possible to see the correct behavior of the three-level voltages across both primary and secondary sides of the MFT in each module, ensuring the correct performance of the proposed modulation algorithm. Although, the frequency of such waveforms remains constant, their widths varies with the input current control loop, presented in chapter 3. Besides, the phase shift delay, it is also changeable by a control loop, regulating the power flow of the

proposed converter. All these characteristics are noted in Figure 4.13 both simulations and experimental tests.

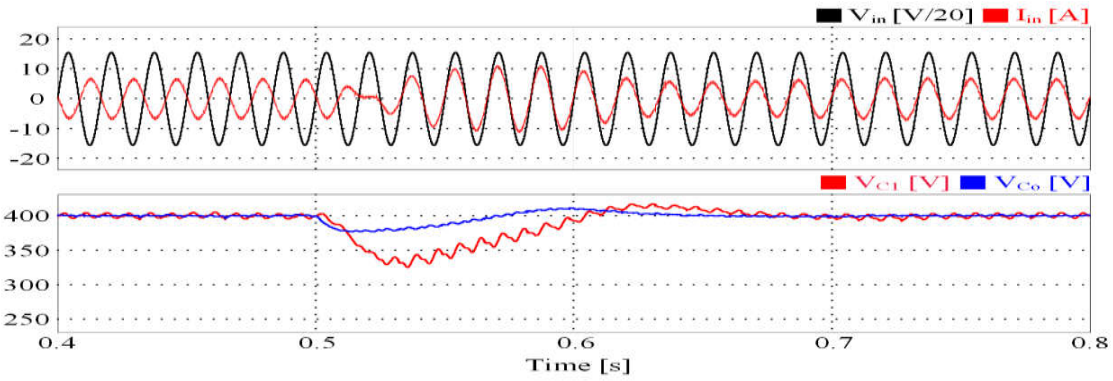
4.3 Dynamic behavior

This section present the dynamics result of both single-module and two-module structures during the reversion of the 100% to -100% of the rated load condition. These kind of tests demonstrate the performance of all control loops embedded in the DSC in a unique dynamic situation. Then, it is possible to evaluate the behavior of the regulated variables of the proposed power converters.

4.3.1.1 Single-module power converter structure

Figure 4.14 presents the result of the power inversion of 100% to -100% of the converter rated power in the simulation model. It is possible to seen the complete inversion (180º) of the ac input current phase in relation of the grid voltage, demonstrating the expected behavior of the test. The settling time for the ac input current is about 0.13 s and, since the test has the same amount of power at its begin and end, the ac input current has the same waveforms with the respective phase disposition in each step of the test.

Figure 4.14 – Single-module structure dynamic behavior for the reversion power flow test in the simulation model

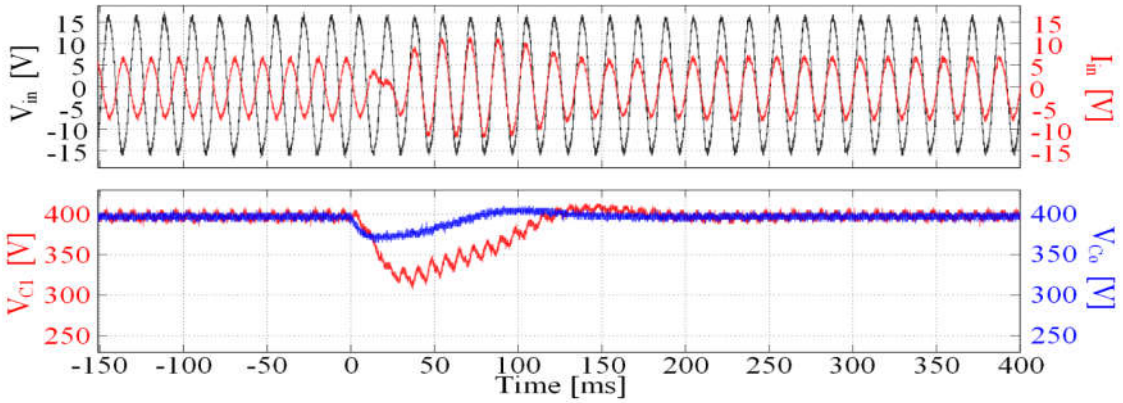


SOURCE: Author's right.

It is noted a drop in the dc link voltage, V_{C1}, during the test is about 80 V with a settling time about 0.2 s. The output voltage behavior, V_{Co} presents a voltage variations about 30 V, been regulated by the output voltage control loop to its reference value in 0.2 s, as well.

In Figure 4.15 it is presented the behavior of the same variables presented in the last figure, however for the experimental test. It is noted a very similar behavior among the variables in each test, since the simulation model was configured with the maximum number of parameters from the experimental set up, as well as, the same controllers gains.

Figure 4.15 – Single-module structure dynamic behavior for the reversion power flow test in the experimental setup



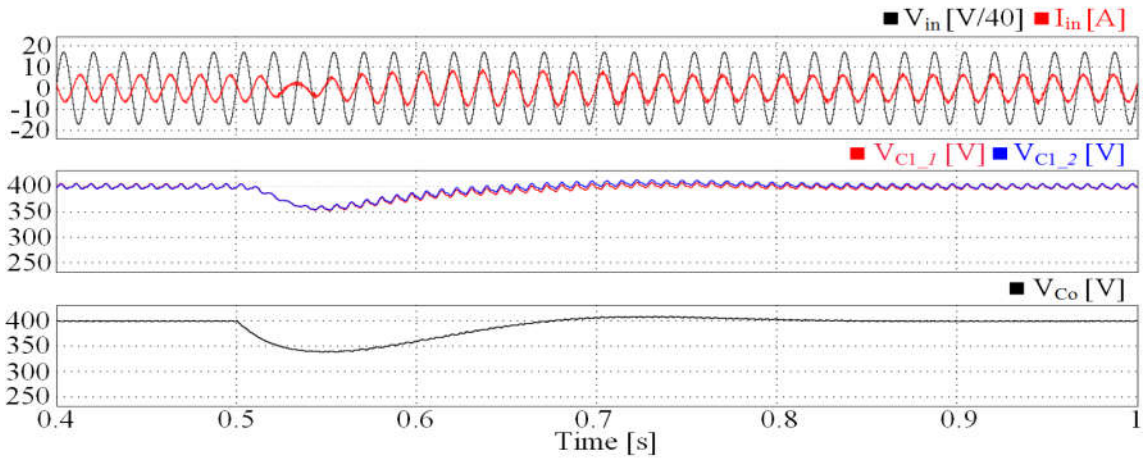
SOURCE: Author's right.

The ac input current has a settling time about 150 ms with the complete inversion of its phase angle compared with the one in the grid voltage, as expected by the nature of the test. The behavior of the dc voltages are, also, noted, where the V_{C1} and V_{Co} are regulated perfectly by the control loops. The V_{C1} has a drop about 80 V, while V_{Co} has about 30 V. The settling times of such dc voltages are 200 ms, similar with the ones presented in the simulation.

4.3.1.2 Tow-module power converter structure

The Figure 4.16 presents the behavior of the reversion power flow test with the two-module structure in the simulation model. Each module process 1 kW, resulting in a power flow of 2 kW. The grid voltage was increased to 440 V, then the ac input current characteristics were preserved.

Figure 4.16 – Two-module structure dynamic behavior for reversion power flow test in the simulation model



SOURCE: Author's right

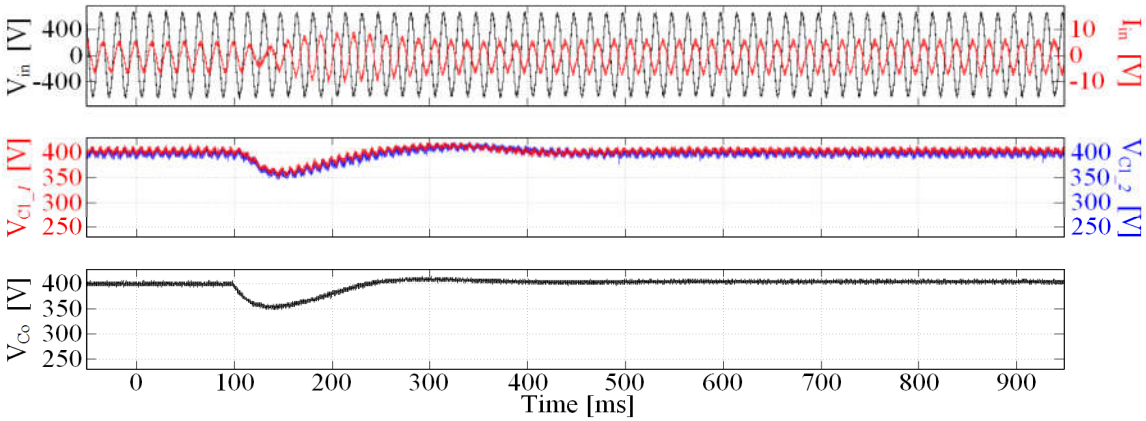
It is possible to noted that the ac input current maintain the same shape for both power flow conditions, besides the opposite phase angle, during the begin and end of the test. The settling time is about 200 ms.

The dc voltages in the primary side of the MFT for each module, V_{C1_1} and V_{C1_2}, respectively, present a good regulation during the test, since both voltages has very similar behavior with a maximum drop about 50 V and settling time about 350 ms.

The output voltage, also presents a good performance, since its regulation was correctly made by the output voltage control loop. It is possible to see a variation about 55 V.

In Figure 4.17 is presented the result of the same test made in the simulation model, however in the experimental set up.

Figure 4.17 – Two-module structure dynamic behavior for reversion power flow test in the experimental setup



SOURCE: Author's right

It is possible to note a very similar behavior among the variables from the simulation test and this one, for the same reasons mentioned before.

The ac input current waveform present the expect behavior of reversion of the phase angle and the power factor correction made by the input control loop. It is, also, possible to see the good behavior of the dc link voltages in each module, regulated by the dc link voltage balancing control and the dc link voltage control loops. With the dc link voltage balancing, it is possible to regulate the dc link in each module independently during the dynamics situations, as explained in the chapter 2. Then the variation about 50 V and the settling time about 350 ms is considered good result.

Finally, the output voltage present a drop about 50 V, as well with the same settling time presented before.

5 CONCLUSION

This thesis has presented a new concept for a bidirectional multilevel converter with cascaded structures feasible to traction applications. The qualitative and quantitative analysis is presented through the operating principle, theoretical waveforms, experimental results, as well as the comparative study for real railway parameters applications have been presented and discussed.

The theoretical analysis has demonstrated the impact of the interleaving technique based on coupled windings providing a simple solution for the current sharing among the semiconductors in the primary side of the MFT. Besides, the proper adjustments of the respective MFTs turns ratios in the modules allow the structure achieve low-voltage capability, thus increasing its flexibility. Even though it uses coupled-winding unlike other solutions with additional conversion stages, the proposed concept has presented satisfactory results, while nearly the same efficiency has been achieved for both arrangement of the proposed converter.

It was possible to note that even with the additional magnetic, it is possible to compensate the total magnetic volume due the good results of WTHD from the multilevel voltages which the proposed converter can provide for the application. Then, the magnetic volume of other topologies are similar of the one in the proposed converter, as it was presented in the comparative losses analysis.

The main contribution of this work lies in the conception of an interleaved cascaded modular converter adequate to high-voltage application. Its modularity resulting from the use of ISOP configuration is highly desirable in medium-voltage high-power application considering the minimization of voltages stresses across the semiconductors. Besides, it is possible to select spare modules for live system maintenance, which can be scaled up or down easily for distinct applications.

Possible future works from this thesis can be focus in the expansion of the number of modules for a high-voltage prototype, and then, using spared modules, it is possible to investigate the proposed converter failure tolerance.

Other possible branch, is to investigate the union of the MFT and interface transformer in one single magnetic core structure. Preliminaries studies with this matter, in the laboratory where this thesis was developed, shows promising results, like the reduction of the resulting magnetic volume.

In fact, the mature investigation of these aspects is the key to more efficient, versatile and reliable development of topologies with the same characteristics of the proposed converter.

5.1 Scientific Production

Some of the scientific or technical papers that it were published in the last five years during the PhD studies are presented as follow.

5.1.1 Proceeding Papers

a) HONÓRIO, D. A.; et al. Modular transformer in Isolated Multiport Power Converters. In: 2017 3RD ANNUAL SOUTHERN HEMISPHERE POWER ELECTRONIC CONFERENCE, 2017 Puerto Varas, Chile. **Conference Publications…** 4-7 dez. 2017, p. 1-5.

b) HONÓRIO, D. A.; et al. A solid state transformer based on a single-stage AC-DC modular cascaded multilevel converter. In: 2016 18TH EUROPEAN CONFERENCE ON OPWER ELECTRONICS AND APPLICATIONS, 2016 Karlsruhe, Germany. **Conference Publications…** 5-9 out. 2016, p. 1-9.

c) HONÓRIO, D. A.; et al. A Space Vector PWM scheme for a Single-stage Ac-Dc Modular Cascaded Multilevel Converter. In: 2015 IEEE 13TH BRAZILIAN POWER ELECTRONICS CONFERENCE AND 1ST SOUTHERN POWER ELECTRONICS CONFERENCE, 2015 Fortaleza, Brazil. **Conference Publications…** 29 nov.-2 dez. 2015, p. 1-6.

d) HONÓRIO, D. A.; OLIVEIRA, D. S.; BARRETO, L. H. S. C. An AC-DC Multilevel Converter Feasible to Traction Application. In: 2015 17TH EUROPEAN CONFERENCE ON POWER ELECTRONICS AND APPLICATIONS, 2015 Geneva, Switzerland. **Conference Publications…** 8-10 set. 2015, p. 1-9.

e) OLIVEIRA, S. O.; et al. A Single-State AC-DC modular Cascaded Multilevel Converter Feasible to SST Applications. In: 2015 INTERNATIONAL EXHIBITION AND CONFERENCE FOR POWER ELECTRONICS, INTELLIGENT MOTION, REWABLE ENERGY AND ENERGY MANAGEMENT, 2015 Nuremberg, Germany. **Conference Publications…** 19-20 mai. 2015, p. 1-8.

f) OLIVEIRA, S. O.; et al. A two-stage AC/DC SST based on modular multilevel converter feasible for AC railway systems. In: 2014 IEEE APPLIED POWER ELECTRONICS CONFERENCE AND EXPOSITION, 2014 Fort Worth, USA. **Conference Publications…** 16-20 mar. 2014, p. 1894-1901.

g) OLIVEIRA, S. O.; et al. A two-stage AC/DC SST based on modular multilevel converter. In: 2013 BRAZILIAN POWER ELECTRONICS CONFERENCE, 2013 Gramado, Brazil. **Conference Publications…** 27-31 out. 2013, p. 254-258.

5.1.2 Journal Papers

a) BARRETO, L. S. C.; et al. An Interleaved-stage Ac-Dc Modular Cascaded Multilevel Converters as a Solution for MV Railway Applications. **IEEE Transaction on Industrial Electronics**, early access, p. 1-9, set. 2017.

BIBLIOGRAPHY

(1) FITZGERALD, A. E.; KINGSLEY Jr, C.; UMANS, S. D. **Máquinas Elétricas com Introdução à Eletrônica de Potência.** São Paulo: Bookman, 2006.

(2) HUANG, A. Q., Medium-Voltage Solid-State Transformer: Technology for a Smarter and Resilient Grid. **IEEE Industrial Electronics Magazine**, v. 10, n. 3, p. 29-42, set. 2016.

(3) MCLYMAN, COLONEL WM. T. **Transformer and inductor design handbook.** California: CRC Press, 2004.

(4) POMPILI, M.; et al. Natural esters distribution transformers: A solution for environmental and fire risk prevention. In: AEIT INTERNATIONAL ANNUAL CONFERENCE, 2016 Capri, Italy. **Conference Publications…** 5-7 out. 2016, p. 1-5.

(5) DUJIC, D.; et al. Power Electronic Traction Transformer Technology. In: INT. POWER ELECTRONICS AND MOTION CONTROL CONFERENCE, 2012 Harbin, China. **Conference Publications…** 2-5 jun. 2012, p. 636-642.

(6) COSTA, L. F.; et al., The Smart Transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid. **IEEE Power Electronics Magazine**, v. 10, n. 2 p. 56-67, jun. 2017.

(7) HUBER, J. E.; KOLAR, J. W. Applicability of Solis-State Transformers in Today's and Future Distribution Grids. **IEEE Transaction on Smart Grids**, v. 00, n. 0 p. 1-1, ago. 2017.

(8) MEI, T. X.; QU, K.; Li, H. Control of wheel motors for the provision of traction and steering of railway vehicles. **IET Power Electronics**, v. 7, p. 2279-2284, fev. 2014.

(9) BARRETO, L. S. C.; et al. An Interleaved-stage Ac-Dc Modular Cascaded Multilevel Converters as a Solution for MV Railway Applications. **IEEE Transaction on Industrial Electronics**, early access, p. 1-9, set. 2017.

(10) HUBER, J. E.; KOLAR, J. W. Solid-State Transformers: On the Origins and Evolutions of Key Concepts. **IEEE Industrial Electronics Magazine**, v. 10, n. 3 p. 19-28, set. 2016.

(11) HEINEMANN, L.; MAUTHE, G.The universal power electronics based distribution transfromer, an unified approach. In: POWER ELECTRONICS SPECIALISTS CONFERENCE, 2001 Vancouver, Canada. **Conference Publications…** 17-21 jun. 2001, p. 504-509.

(12) FALCONES, S.; MAO, X.; AYYANAR, R. Topology comparison for Solid State Transformer implementation. In: 2010 IEEE POWER AND ENERGY SOCIETY GENERAL MEETING, 2010 Providence, USA. **Conference Publications…** 25-29 jul. 2010, p. 1-8.

(13) XU, S.; HUANG, A. Q.; BURGOS, R. Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems. **IEEE Journal of Emerging and Selected Topics in Power Electronics**, v. 1, n. 3 p. 186-198, ago. 2013.

(14) KOLAR, J. W.; ORTIZ, G. **Solid State Transformer Concepts in Traction and Smart Grid Applications** Seminar presented in the Applied Power Electronics Conference APEC 2013 Long Beach USA.

(15) DRÁBEK, P; et al. New Configuration of Traction Converter With Medium-Frequency transformer Using Matrix Converters. **IEEE Transaction on Industrial Electronics**, v. 51, p. 5041-5048, nov. 2011.

(16) KANG, M.; ENJETI, P. N.; PITEL, I. J. Analysis and Design of Electronic transformers for Electric Power Distribution System. **IEEE Transaction on Power Electronics**, v. 14, p. 1133-1141, nov. 1999.

(17) SABAHI, M. Flexible Power Electronic transformer. **IEEE Transaction on Power Electronics**, v. 25, p. 2159-2169, jan. 2010.

(18) WANG, G.; et al. Design and hardware implementation of Gen-1 silicon based solid state transsformer. In: IEEE APLLIED POWER ELECTRONICS CONFERENCE AND EXPOSITION, 2011 Fort Worth, USA. **Conference Publications…** 6-11 mar. 2011, p. 1344-1349.

(19) GU, C.; et al. Modeling and Control of a Multiport Power Electronic Transformer (PET) for Electric Traction Applications. **IEEE Transaction on Power Electronics**, v. 31, p. 915-927, fev. 2016.

(20) BIFARETI, S.; et al. Advanced Power Electronic Conversion and Control System for Universal and Flexible Power Management. **IEEE Transaction on Smart Grid**, v. 2, p. 231-243, mar. 2011.

(21) GLINKA, M.; MARQUART, R. A new AC/AC Multilevel Converter Family. **IEEE Transaction on Industrial Electronics**, v. 52, p. 662-669, jun. 2005.

(22) TAUFIQ, J. Power electronics technologies for railway vehicles. In: INTERNATIONAL POWER ELETRONICS MOTION CONTROL CONFERENCE, 2007 Nagoya, Japan. **Conference Publications…** 2-5 abr. 2007, p. 1388-1393.

(23) DROFENIK, U.; CANALES, F. European trends and technologies in traction. In: 2014 INTERNATIONAL POWER ELECTRONICS CONFERENCE, 2014 Hiroshima, Japan. **Conference Publications…** 18-21 mai. 2014, p. 1043-1049.

(24) MERMET-GUYENNET, M. New power technologies for traction drives. In: 2010 INTERNATIONAL SYMPOSIUM ON POWER ELECTRONICS ELECTRICAL DRIVES AUTOMATION AND MOTION, 2010 Pisa, Italy. **Conference Publications…** 14-16 jun. 2010, p. 719-723.

(25) FENG, J.; et al. Power Electronic Transformer-Based Railway Traction Systems: Challenges and Opportunities. **IEEE Journal of Emerging and Selected Topics in Power Electronics**, v. 5, p. 1237-1253, mar. 2017.

(26) KOLAR, J.; HUBER, J. E. Solid-state transformers in future traction and smart grids. In: INTERNATIONAL MOTION, RENEWABLE ENERGY AND ENERGY MANAGEMENT, 2015 Nuremberg, Germany. **Conference Publications…** 24-26 jun. 2015, p. 1-6.

(27) AGHEB, E.; HØIDALEN, H. K. Medium frequency high power transformers, state of art and challenges. In: 2012 INTERNATIONAL CONFERENCE ON REWABLE ENERGY RESEARCH AND APPLICATIONS, 2012 Nagasaki, Japan. **Conference Publications…** 11-14 nov. 2012, p. 1-6.

(28) DANNIER, A.; RIZZO, R. An overview of Power Electronic transformer: Control strategies and topologies. In: 2012 INTERNATIONAL SYMPOSIUM ON POWER ELECTRONICS, ELECTRICAL DRIVES, AUTOMATION AND MOTION, 2012 Sorrento, Italy. **Conference Publications…** 20-22 jun. 2012, p. 1552-1557.

(29) CHENG, L.; et al. The Topology Analysis and Compare of High-Frequency Power Electronic Transformer. In: 2012 ASIA-PACIFIC POWER AND ENERGY ENGINEERING CONFERENCE, 2012 Shanghai, China. **Conference Publications…** 27-29 mar. 2012, p. 1-6.

(30) MARTIN, J.; et al. Medium frequency transformer for railway traction: Soft switching converter with high voltage semi-conductors. In: INTERNATIONAL SYMPOSIUM ON POWER ELECTRONICS, ELECTRICAL DRIVES, AUTOMATION AND MOTION, 2008 Ischia, Italy. **Conference Publications…** 11-13 jun. 2008, p. 1180-1185.

(31) RONANKI, D.; WILLIAMSON, S. S. Evolution of Power Converter Topologies and Technical Considerations of Power Electronic Transformer based Rolling Stock Architectures. **IEEE Transaction on Transportation Electrification**, early access, p. 1-6, out. 2017.

(32) CHAUDHARY, P.; SENSARMA, P. Front-End Buck rectifier With Reduced Filter Size and Single-Loop Control. **IEEE Transaction on Industrial Electronics**, v. 60, p. 4359-4368, set. 2012.

(33) AKAGI, H. Classification, Terminology, and Application of the Modular Multilevel Cascaded Converter (MMCC). **IEEE Transaction on Power Electronics**, v. 26, p. 3119-3130, abr. 2011.

(34) WINKELNKEMPER, M.; KORN, A.; STEIMER, P. A modular direct converter for transformeless rail interties. In: 2010 IEEE INTERNATIONAL SYMPOSIUM ON INDUSTRIAL ELECTRONICS, 2010 Bari, Italy. **Conference Publications…** 4-7 jul. 2010, p. 562-567.

(35) COPPOLA, M.; PIZZO, A. DEL; IANNUZI, D. A power traction converter based on Modular Multilevel architecture integrated with energy storage devices. In: 2012 ELECTRICAL SYSTEMS FOR AIRCRAFT, RAILWAY AND SHIP PROPULSION, 2012 Bologna, Italy. **Conference Publications…** 16-18 out. 2012, p. 1-7.

(36) JOCA, D. R.; et al. Three-phase AC-DC solid-state transformer for low-voltage DC power distribution applications. In: 2016 12th IEEE INTERNATIONAL

CONFERENCE ON INDUSTRY APPLICATIONS, 2016 Curitiba, Brazil. **Conference Publications…** 20-23 nov. 2016, p. 1-8.

(37) PACHECO, J. DE O.; et al. Bidirectional modular multilevel PFC rectifier based on cascading full-bridge and interleaving technique suitable for SST applications. In: 2016 12th IEEE INTERNATIONAL CONFERENCE ON INDUSTRY APPLICATIONS, 2016 Curitiba, Brazil. **Conference Publications…** 20-23 nov. 2016, p. 1-7.

(38) MYSINSKI, W.; ZAJAC, W.; PLATEK, T. Resonance converter with a toroidal transformer for a tram-train vehicle. In: 2014 INTERNATIONAL SYMPOSIUM ON POWER ELECTRONICS, ELECTRICAL DRIVES, AUTOMATION AND MOTION, 2014 Ischia, Italy. **Conference Publications…** 18-20 jun. 2014, p. 1034-1037.

(39) ROY, S.; DE, A.; BHATTACHARYA, S. Current source inverter based cascaded solid state transformer for AC to DC power conversion. In: 2014 INTERNATIONAL POWER ELECTRONICS CONFERENCE, 2014 Hiroshima, Japan. **Conference Publications…** 18-21 mai. 2014, p. 651-655.

(40) SHU, Z.; et al. Diode-campled three-level multi-module cascaded converter based power electronic traction transformer. In: 2015 IEEE 2nd INTERNATIONAL FUTURE ENERGY ELECTRONICS CONFERENCE, 2015 Taipei, Taiwan. **Conference Publications…** 1-4 nov. 2015, p. 1-5.

(41) KEJIAN, S.; et al. High performance control strategy for single-phase three-level neutral-point-clamped traction four-quadrant converters. **IET Power Electronics**, v. 10, p. 884-893, jul. 2017.

(42) HUBER, J. E.; et al. Analysis and cell-level experimental verification of a 25 kW all-SiC isolate front end 6.6 kV/400 V AC-DC solid-state transformer. **CPSS Transaction on Power Electronics and Applications**, v. 2, p. 140-148, ago. 2017.

(43) ALI, M.; et al. 7-Level asymmetrical hybrid cascaded multilevel converter topology for traction system. In: 2017 INTERNATIONAL CONFERENCE ON ELECTRICAL ENGINEERING, 2017 Lahore, Pakistan. **Conference Publications…** 2-4 mar. 2017, p. 1-6.

(44) KOURO, S.; et al. Recent advances and Industrial Applications of Multilevel converters. **IEEE Transaction on Industrial Electronics**, v. 57, p. 2553-2580, ago. 2010.

(45) TORRICO-BASCOPE, G.; BARBI, I.. A single phase PFC 3 kW converter using a three-stage switching cell. In: 204 IEEE 35TH ANNUAL POWER ELECTRONICS SPECIALISTS CONFERENCE, 2004 Aachen, Germany. **Conference Publications…** 20-25 jun. 2004, p. 4037-4042.

(46) COUGO, B.; et al. Comparative Evaluation of Individual and Coupled Inductor Arrangements for Input Filters of PV Inverter Systems. In: 2012 7th INTERNATIONAL CONFERENCE ON INTEGRATED POWER ELECTRONICS SYSTEMS, 2012 Nuremberg, Germany. **Conference Publications…** 6-8 mar. 2012, p. 1-8.

(47) DONKER, R. W.; DIVAN, D. M.; KHERALUWALA, M. H. A three-phase soft-switching high power density DC/DC converter for high power applications. **IEEE Transaction on Industry Applications**, v. 27, p. 63-73, jan./fev. 1991.

(48) HONORIO, D.; OLIVEIRA, D.; BARRETO, L. H. An AC-DC Multilevel Converter Feasible to Traction Application. In: 2015 17th EUROPEAN CONFERENCE ON POWER ELECTRONICS AND APPLICATIONS, 2015 Geneva, Switzerland. **Conference Publications…** 8-20 set. 2015, p. 1-9.

(49) WU, B. **High-power converters and AC drivers.** California: Wiley-IEEE Press, 2006.

(50) HOLMES, D. G.; LIPO, T. A. **Pulse Width Modulation for Power Converters: principles ad practice.** California: Wiley-IEEE Press, 2003.

(51) SILVA FILHO, O. C. DA; Oliveira, D. DE S. Proposal of a new fanily of high frequency isolated single-phase AC-AC converters. In: 2016 12th INTERNATIONAL CONFERENCE ON INDUSTRY APPLICATIONS, 2016 Curitiba, Brazil. **Conference Publications…** 20-23 nov. 2016, p. 1-8.

(52) OGASWARA, S.; AKAGI, H.; NABAE, A. A novel PWM scheme of voltage source inverters based on space vector theory. **Electrical Engineering**, v. 74, p. 33-41, jun. 1990 ISSN: 0948-7921.

(53) HONORIO, D.; et al. A Space Vector PWM scheme for a single-stage Ac-Dc modular Cascaded Multilevel Converter. In: 2015 IEEE 13TH BRAZILIAN POWER ELECTRONICS CONFERENCE AND 1ST SOUTHERN POWER ELECTRONICS CONFERENCE, 2015 Fortaleza, Brazil. **Conference Publications…** 29 nov. – 2 dez. 2015, p. 1-6.

(54) ARAÚJO, J. W. M. Conversor ca-cc multinível de único estágio para aplicação em transformadores de estado sólido. 2018. Dissertação (Mestrado em Engenharia Elétrica) – Departamento de Engenharia Elétrica, Universidade Federal do Ceará, Ceará.

(55) SASSO, E. M.; et al.. Investigação dos Modelos de Circuitos de Sincronismo trifásicos Baseados na Teoria das Potências real e Imaginária Instantâneas (p-PLL e q-PLL). In: XVI CONGRESSO BRASILEIRO D AUTOMÁTICA, 2002 Natal, Brazil. **Conference Publications…** 22-5 nov. 2002, p. 480-485.

(56) SILVA, S. A. O.; NOVOCHADLO, R.; MODESTO, R. A. Single-Phase PLL Structure Applied to Utilty Connected Systems Using the Instantaneous Active Power Theory. In: IEEE POWER ELECTRONIC SPECIALISTS CONFERENCE, 2008 Rhodesm, Greece. **Conference Publications…** 15-19 jun. 2008, p. 4706-4711.

(57) CLARKE, E. **Circuit Analysis of A-C Power Systems.** New York: General Electric, vol. 2, 1950.

(58) EVERTS, J.; et al. Optimal ZVS Modulation o Single-Phase Single-Stage Bidirectional DAB AC-DC Converters. **IEEE Transaction on Power Electronics**, v. 29, p. 3954-3970, nov. 2014.

(59) CASANELLAS, F. Losses in PWM inverters using IGBTs **IEE Proceeding – electric Power Applications**, vol. 141, no. 5, pp. 235-239, Sep 1994.

(60) RUFER, A., -C; SCHIBLI, N.; BRIGUET, C. A direct coupled 4-quadrant multilevel converter for 16 2/3 Hz traction systems. In: SIXTH INTERNATIONAL CONFERENCE ON POWER ELECTRONICS AND VARIABLE SPEED DRIVES, 1996 Nottinhgham, UK. **Conference Publications…** 23-25 set. 1996, p. 448-453.

(61) OLIVEIRA, D., S.; et al. A two-stage AC/DC SST based on modular multilevel converter feasible to AC railway systems. In: 2014 29TH TWENTY-NINTH ANNUAL IEEE APPLIED POWER ELECTRONICS CONFERENCE AND EXPOSITION, 2014 Fort Worth, USA. **Conference Publications…** 16-20 mar. 2014, p. 1894-1901.

(62) OLIVEIRA, D., S.; et al. A single-Stage AC-DC Modular Cascaded Multilevel Converter Feasible to SST Applications. In: INTERNATIONAL EXHIBITION AND CONFERENCE FOR POWER ELECTRONICS, INTELLIGENT MOTION, RENEWABLE ENERGY AND ENERGY MANAGEMENT, 2015 Nuremberg, Germany. **Conference Publications…** 19-20 mai. 2015, p. 1-8.

(63) SCHWEIZER, M.; et al. Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies. In: 36TH ANNUAL CONFERENCE ON IEEE INDUSTRIAL ELECTRONICS SOCIETY, 2010 Nuremberg, Germany. **Conference Publications…** 7-10 nov. 2010, p. 391-396.

(64) VERNABLE, H., D. The K Factor: A New Mathematical Tool For Stability Analysis and Synthesis. In: REPRINTED FROM THE PROCEEDING OF POWERCON10, 1983 California, USA. **Conference Publications…** 22-24 mar. 1983, p. 1-12.

(65) TELLEGEN, B., D., H. The Gyrator, A New Electric Network Element. In: REPRINTED FROM PHILIPS RESEARCH REPOSITORY, 1948 Amsterdam, Netherlands. **Conference Publications…** abr. 1948, p. 81-101.

(66) DOS SANTOS, W. M.; MARTINS, D. C. Dual Active Bridge converters as gyrator. In: 2012 IEEE THIRD INTERNATIONAL CONFERENCE ON SUSTAINABLE ENERGY TECHNOLOGIES, 2012 Kathandu, Nepal. **Conference Publications…** 24-27 set. 2012, p. 169-176.

(67) TEXAS INSTRUMENTS **Delfino TMS320F28377D controlCARD R1.1 Information Guide**, ver. 1.5 Tokyo, Japan 2015, 16 p.