UNIVERSIDADE FEDERAL DO CEARÁ

CENTRO DE TECNOLOGIA

DEPARTAMENTO DE ENGENHARIA DE TELEINFORMÁTICA

CURSO DE GRADUAÇÃO EM ENGENHARIA DE TELECOMUNICAÇÕES

THIAGO AZEVEDO DE VASCONCELOS

DESIGN OF AN ELECTROMAGNETIC ENERGY HARVESTING CIRCUIT (RF-DC CONVERTER) APPLIED TO CMOS 45NM TECHNOLOGY

FORTALEZA

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Trabalho de Conclusão de Curso apresentado ao Curso de Graduação em Engenharia de Telecomunicações do Centro de Tecnologia da Universidade Federal do Ceará, como requisito parcial à obtenção do grau de Bacharelado em Engenharia de Telecomunicações.

Orientador: Prof. Dr. techn. Dr. h.c. Josef A. Nossek

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Dados Internacionais de Catalogação na Publicação
Universidade Federal do Ceará
Biblioteca Universitária
Gerada automaticamente pelo módulo Catalog, mediante os dados fornecidos pelo(a) autor(a)

V451d Vasconcelos, Thiago Azevedo de.
Design of an Electromagnetic Energy Harvesting Circuit (RF-DC Converter) Applied to CMOS 45nm Technology / Thiago Azevedo de Vasconcelos. – 2018.
66 f. : il. color.

Trabalho de Conclusão de Curso (graduação) – Universidade Federal do Ceará, Centro de Tecnologia, Curso de Engenharia de Telecomunicações, Fortaleza, 2018.
Orientação: Prof. Dr. Josef Anton Nossek.
Coorientação: Prof. Dr. André Lima Férrer de Almeida.

1. Energy Harvesting. 2. RF-DC. 3. Dickson Voltage Multiplier. 4. Multiplicador de Tensão de Dickson. I. Título.

CDD 621.382

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Aprovada em: 25 June, 2018

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I offer this work to my parents Solange and Guilherme, who have carefully and passionately raised me and my brother, giving us the best of the education one could ask for.

ACKNOWLEDGEMENTS

I am first of all, thankful to God, for He deserves all the glories from men. Because I have found peace in His beautiful philosophy taught by His son, Jesus Christ, and in my prayers for Him and for our Mother, Mary. Also for all of the important people He put on my life.

Many have helped me to become who I am in all spheres of my life, but here those who have contributed to my professional and ethical educations are mentioned.

I would like to thank my family, specially my mother Solange, my father Guilherme and my brother Felipe for the my dear daily life and support. To my girlfriend Marina, who has also made part of it being a true partner for all days.

Many of my friends have given me support and assistance on matters related to my professional formation since elementary school. Friends from my elementary and high school; from UFC's Electrical Engineering, Teleinformatics Department, GPSI and Chemical Engineering.

On my foreign studies in France, I have made some valuable friends to whom I also thank. Specially to Rafael Kotchetkoff Carneiro, who was my partner in an early project back in 2015 from which a report was produced. This report served as one of the most important foundations for this project. He also designed the layout of the integrated circuit in the annex.

There have been many important professors in my life, so I must restrict my selfelf and cite only the most important since past year, with whom I shared knowledge, perspectives and concerns about the career and friendly talks. Special thanks to: André Lima Férrer, Josef Anton Nossek (advisor of this project) and Felix Antreich.

"Let your light so shine before men, that they may see your good works, and glorify your Father which is in heaven."

(Jesus Christ, Matthew 5:16)

RESUMO

O assunto principal deste projeto é o design de um circuito de Energy Harvesting usando uma arquitetura proposta pelo artigo (ASL; ZARIFI, 2014) e pela tese de doutorado (SEIGNEURET, 2011). Essa arquitetura é o Multiplicador de Tensão de Dickson, um circuito capaz de aumentar a tensão de saída de um circuito que, neste caso, é alimentado por energia de baixa potência proveniente do ambiente. Esta monografia impõe algumas restrições e diretivas ao projeto e inicia-se pela análise das equações e curvas do circuito básico da arquitetura do Multiplicador de Tensão de Dickson. Após a sua análise e a compreensão do seu funcionamento, o foco do projeto muda para criar um circuito capaz de satisfazer os objetivos e limitações definidos no início. Simulações são feitas, como a de Monte Carlo, e depois dos resultados conclusões sobre a perfomance do circuito são feitas. O layout de um circuito integrado feito para este circuito é apresentado nos anexos.

Palavras-chave: Energy Harvesting (Colheita de Energia). Conversor RF-DC. Multiplicador de Tensão de Dickson.

ABSTRACT

The main topic of this project is a design of an Energy Harvesting circuit using an architecture proposed by a paper (ASL; ZARIFI, 2014) and a doctor thesis (SEIGNEURET, 2011). This architecture is the Dickson Voltage Multiplier, a circuit capable for increasing the output voltage of a circuit which is, in this case, fed with low power energy from the environment. This monograph imposes some constraints and directives to the project and starts by analyzing the equations and curves of the basic circuit of the Dickson Voltage Multiplier architecture. After its analysis and understanding of its basic behavior, the project's focus changes to create a circuit which satisfy the objectives and constraints set at the beginning. Simulations are performed, like Monte Carlo, and after the results, conclusions about the performance of the circuit are made. The layout of an integrated circuit designed for this circuit is presented on the annex.

Keywords: Energy Harvesting. RF-DC Converter. Dickson Voltage Multiplier.

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LIST OF ABBREVIATIONS

AC	Alternating Current
AC-DC	Alternating Current to Direct Current
DC	Direct Current
DC-DC	Direct Current to Direct Current
DVM	Dickson Voltage Multiplier
GPDK	Generic Process Design Kits
IoT	Internet of Things
IV	Current-voltage
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MIMO	Multiple-Input Multiple-Output
RF	Radio-Frequancy
RF-DC	Radio-Frequency to Direct Current
RF-ID	Radio-Frequency Identification
UHF	Ultra High Frequency

LIST OF SYMBOLS

v	Voltage drop
i	Electrical current
C	Capacitance or capacitor
R	Resistance or resistor
D	Diode
f	Frequency
t	Time
ω	Radian frequency
τ	Time constant
α	Generic scaling factor for quantities
W	NMOS transistor's channel width
P	Power
η	Power efficiency

TABLE OF CONTENTS

1 INTRODUCTION

Energy harvesting is the process of capturing electromagnetic energy from external sources and "recycle"it in order to feed electronic circuits with available and not used energy surrounding us.

This energy can come from various sources. Specially from Wi-Fi and Bluetooth signals "echoing"on small environments; from antenna's radiations emitted by base stations of AM or FM radios, of television channels, of telephony; from heated materials [Israel (2018)]; from mechanical sources and many other sources.

For example, in (SHINDE *et al.*, 2014), the authors' work's objective was to sustain military and paramilitary applications in order to avoid shortage. This is one important use: avoiding crucial small systems to run out of energy during shortages. There, they harnessed energy from vibrations, thermal energy and electromagnetic energy.

As another example focused on mechanical sources, the authors in (OTTMAN *et al.*, 2002) have used a vibrating piezoelectric device which captures mechanical vibrations and transforms it into electrical Alternating Current (AC) energy. The authors converted this energy using Alternating Current to Direct Current (AC-DC) converters and then Direct Current to Direct Current (DC-DC) converters with adaptive control techniques, enabling optimal power transfer and storing.

Wasted electromagnetic waves of communications systems are the one of the most important kind of energy aimed by the energy harvesting domain and by this project. This implies that circuits possess antennas responsible for capturing those waves.

This kind of technology already enables us to power Radio-Frequency Identification (RF-ID) tags (such as said by (SEIGNEURET, 2011)) meant for countering thefts, used on access granting badges, for electronic toll collection and many other uses. Most importantly: without requiring any battery.

In the future, when Internet of Things (IoT) -gradually becoming a daily reality- will be broadly used, many systems will have electronic circuits functioning, spread around the world. Some will capture signals (sensors), some will process those signals, some will take decisions depending on the processed signals and some will act to execute a command based on the decisions taken.

When dealing with IoT, even clothes become an environment for development. In (AHN *et al.*, 2015), the authors create a system which integrates tactile sensors in fabric form

with energy harvesters.

In such a scenario, there's no way to feed every single one of those circuits with wires, that would be incredibly impractical and costly. So either many long life-time and easily chargeable batteries will be produced or many circuits will be powered wirelessly. A great opportunity to reduce the complexity of charging these systems and save resources is reusing the wasted energy.

For the studies followed by GTEL and the Teleinformatics Department, the greatest interest is in the MIMO communications domain: for powering radio-frequency electronic chains coupled to antennas in a scenario where there will be many antennas. Thus, several electronic components like phase-shifters, low-noise amplifiers, filters, high-frequency oscillators and other components can be self powered.

All of those applications are low power applications, but already some works, like (GORLATOVA *et al.*, 2013), aim at ultra-low power outputs. In this article, the authors have made long-term indoor measurements and have used them as inputs to design algorithms and a system for those ultra-low power applications. The algorithm optimizes the generation of energy of the system.

I have aimed at designing a circuit which will receive energy from an antenna capturing frequencies around 900MHz and then transform it into Direct Current (DC) energy. However, some other strategies are also studied such as ignoring a AC-DC converting circuit and relying solely in an antenna which can perform this conversion alone, as in (SUN *et al.*, 2012).

In this project, the Objectives (chapter 1) and the Scope Statements (chapter 3) determine the direction this project must follow and the guidelines to impose less degrees of freedom, reducing the complexity.

The Radio-Frequency to Direct Current (RF-DC) converter will be designed as an integrated circuit, so it is, at the end, a circuit whose architecture can be analyzed and its behavior understood. The theory in chapter 4 describes throughout its extent many features and details involving the architecture of the circuit.

The Methodology (chapter 5) and the Development (chapter 6) represent how the circuit is designed and it depends on simulations performed in this same chapter. The results of these simulations and performances of the circuit are in chapter 7.

At last, the Conclusion (chapter 8) weights every aspect of the project, the features of the resulting design and the scenarios; and will conclude on the circuit's viable usability.

The layout of the integrated circuit along with its main features and points explained is presented at the annex A.

2 OBJECTIVES

To study the architecture of the circuit and to design it using *Cadence Virtuoso* a RF-DC voltage converter which will output a voltage difference higher than 1 Volt to power a load.

The load is here considered as a generic piece of equipment which could be, depending on the situation, any kind of electronic system present in a RF chain of a transmitter or receiver in a MIMO Communications scenario. As it will be seen in the Conclusions, chapter 8, the very low output power could be used for sensors in a sensor array.

Firstly a theory concerning the architecture of the circuit must be developed and after the circuit is consistently modelled with good values for its elements, the "real"circuit's layout must be drawn.

This study does not deal with the issues related to electromagnetic compatibility between those feeding antennas, the communications's antennas and any other possible EMC impacts on the communications systems.

3 SCOPE STATEMENTS

The following points are the author's impositions to this project. Those parameters are constraints to be followed for successfully producing the desired circuit:

- Input RF signal in 900MHz frequency and 0dBm power (1mW);
- Output voltage difference higher than 1V;
- Output power higher than 10μW (1% of the input power);
- Use 45nm CMOS technology.

Those statements serve as guidelines to achieve the final design which not only can fulfill its purpose, to convert radio frequency energy into direct current, but also to make sure that if one can achieve those specifications, one can achieve others, if needed.

4 THEORY OF THE DICKSON VOLTAGE MULTIPLIER

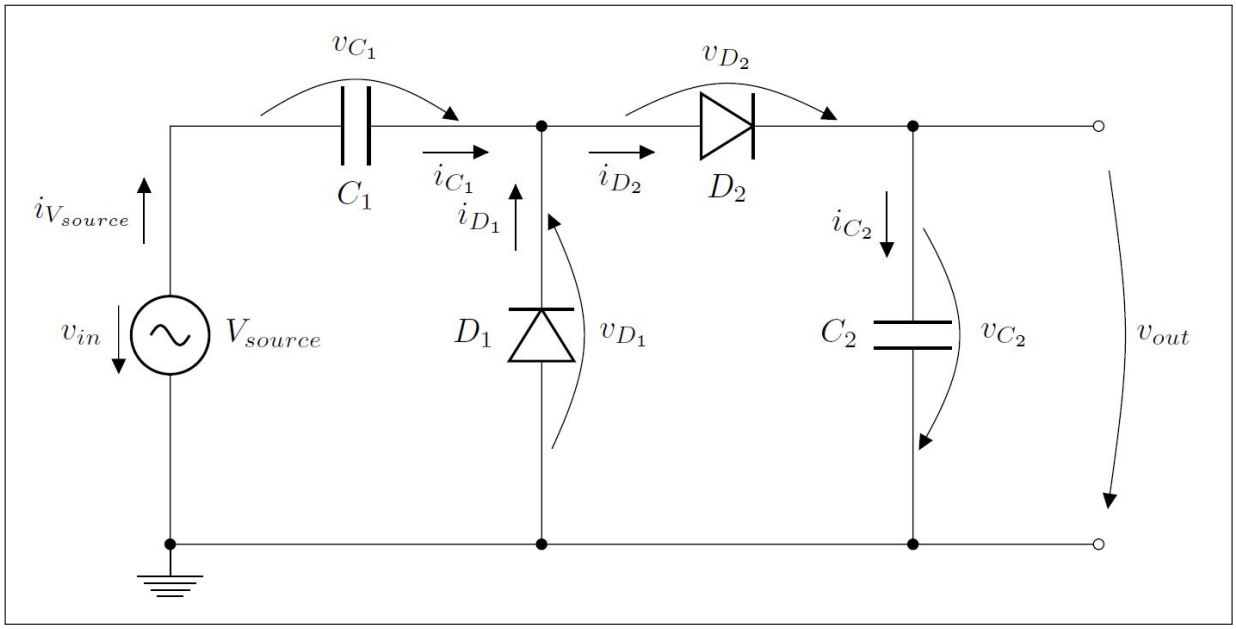
The RF-DC Converter is, basically, an AC-DC converter, being the AC frequencies very high. Those frequencies are classified among the radio-frequencies, which is not, by itself, a precise term, since Radio-Frequancy (RF) is a term employed for almost every transmission frequency in wireless communication systems.

In this project, such is the case, since the aimed electromagnetic waves lie around 900MHz, a portion of the Ultra High Frequency (UHF), frequencies used, among other uses, for amateur radio communications.

Here is shown and explained the heart of the DC signal generation, so to speak. It is the DVM, which is responsible for converting the RF signal (AC signal) into the DC output signal.

The DVM circuit is adopted by some references, such as (ASL; ZARIFI, 2014). In this paper, 13 stages were designed and used, whereas for this project, only three. The simple circuit is shown in Fig. 1, and it basically counts as a single stage. Fig. 1 is also depicting the ideal circuit, where only the converter's elements appear, without loads or sources resistances or any kind of impedance.

Figure 1 – The Ideal Dickson Voltage Multiplier, the AC-DC converter



Source: The author.

In the Section 4.1, the concept and functioning is explained for a single stage. The complete circuit's functioning with all stages, is presented only in chapter 6. Every circuit, is

followed by simulation results acquired from *LT Spice*. Those simulations help to understand the impact of each element in the conversion.

The models of diodes and transistors used are also explained. Following the explanation of the ideal single stage's functioning, section 4.1, real components of the circuit are discussed in the section 4.2.

For a single stage DVM circuit, the equations were derived and the behavior of the circuit for different instants of time is previewed with the help of those equations. The simulation results not only confirm the behaviors predicted, but are also a visual tool for this step by step derivation.

Nonetheless, for the multi stages circuit in the Development, only simulations are presented. At this level, there are too many elements whose behaviors are closely connected, so the system becomes too complex to analyze "by hand".

4.1 Architecture of the basic Dickson Voltage Multiplier (the Single Stage circuit)

To illustrate the DVM's architecture, Fig. 1 is used. Considering that the input voltage comes from the sinusoidal voltage source (V_{source}) and the output voltage is measured at the open circuit's terminals (v_{out}), the (4.1) to (4.8) are derived.

The first two are Kirchhoff's Voltage Law (KVL) equations and the following two are Kirchhoff's Current Law (KCL) equations. Then, the two diodes' IV relations in (4.5) and (4.6), which lead to the polarization analysis of both. At last, the two capacitor's voltage and current equations. Those relations allow for the understanding and prediction of the circuit's behavior.

$$v_{in}(t) = v_{C_1}(t) - v_{D_1}(t) \tag{4.1}$$

$$v_{D_1}(t) + v_{D_2}(t) + v_{C_2}(t) = 0V \tag{4.2}$$

$$i_{C_1}(t) + i_{D_1}(t) = i_{D_2}(t) \tag{4.3}$$

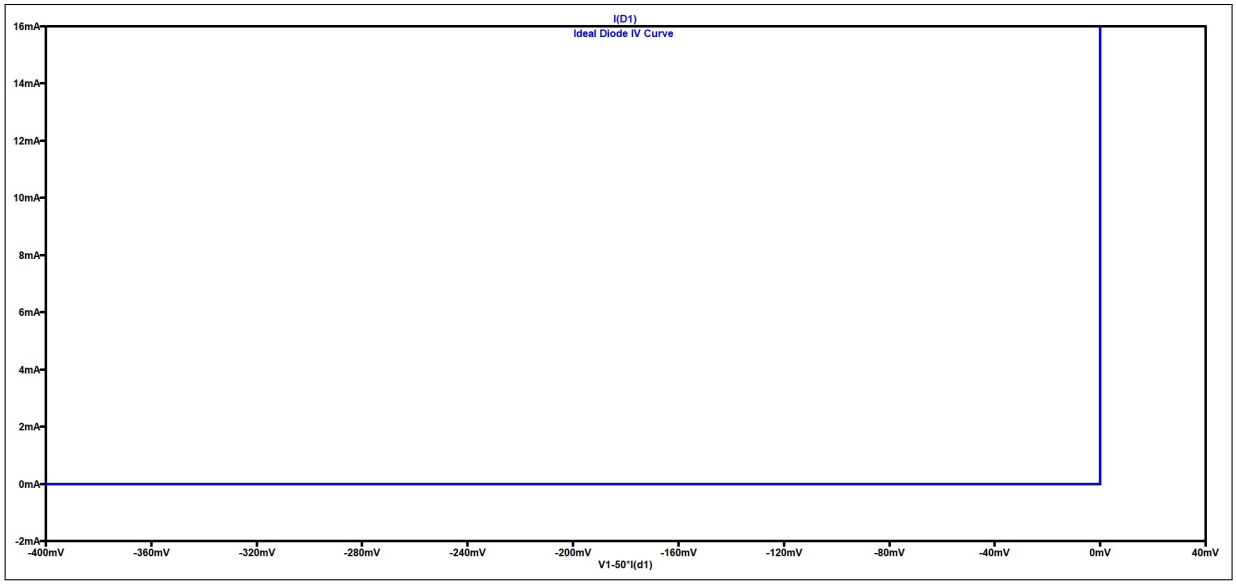
$$i_{C_2}(t) = i_{D_2}(t) \tag{4.4}$$

Both diodes are considered as ideal diodes:

$$\begin{cases} v_{D_1}(t) < 0V \Rightarrow i_{D_1}(t) = 0A \\ i_{D_1}(t) > 0A \Rightarrow v_{D_1}(t) = 0V \end{cases} \tag{4.5}$$

$$\begin{cases} v_{D_2}(t) < 0V \Rightarrow i_{D_2}(t) = 0A \\ i_{D_2}(t) > 0A \Rightarrow v_{D_2}(t) = 0V \end{cases} \tag{4.6}$$

Figure 2 – The ideal diode's IV curve



Source: The author.

$$\begin{aligned} i_{C_1}(t) &= C_1 \frac{dv_{C_1}(t)}{dt} \\ v_{C_1}(t) &= v_{C_1}(t_0) + \int_{t_0}^{t} i_{C_1}(\tau)\, d\tau \end{aligned} \tag{4.7}$$

$$\begin{aligned} i_{C_2}(t) &= C_2 \frac{dv_{C_2}(t)}{dt} \\ v_{C_2}(t) &= v_{C_2}(t_0) + \int_{t_0}^{t} i_{C_2}(\tau)\, d\tau \end{aligned} \tag{4.8}$$

The capacitors are equal, so:

$$C_1 = C_2 \tag{4.9}$$

The initial conditions: the initial value of the input voltage is 0V, which is valid for a sinusoidal voltage source, and the capacitors' initial voltages are 0V as well (both discharged at the beginning).

$$v_{in}(t) = \begin{cases} v_0 \sin(2\pi f t) & \text{for } t \geq 0s \\ 0V & \text{for } t < 0s \end{cases} \tag{4.10}$$

$$\begin{aligned} v_{C_1}(t = 0s) &= 0V \\ v_{C_2}(t = 0s) &= 0V \end{aligned} \tag{4.11}$$

The next procedure is to compute "by hand"the equations for some time intervals whose outcomes are predictable. For the simulations whose graphics will be displayed after the computations of each interval, the same circuit as in Fig. 1 is built in *LT Spice*. Equations in 4.12 summarize some important parameters of the simulations.

$$\begin{aligned} &C_1 = C_2 = 1pF \\ &v_{in}(t) = v_0 \sin 2\pi f t \\ &\text{where,} \\ &v_0 = 350mV \\ &f = 1GHz \end{aligned} \tag{4.12}$$

The instants of time are not analyzed only in t-space (*seconds*), but also in $2\pi ft$-space (*radians*) which is easier to relate to the sinusoidal variations of the voltage source in (4.10). In the analysis, those angles ($2\pi ft$) change as the time (t) runs in the nanoscale (because the frequencies are close to 1 gigahertz). For conciseness, $2\pi f$ will be replaced by ω.

4.1.1 The first time interval

$$\begin{aligned} &\text{For } t \in [0, 250ps] \Rightarrow \omega t \in [0, \pi/2] \\ &v_{in}(t) \geq 0V,\ v_{D_1}(t) \leq 0V,\ v_{D_2}(t) = 0V \\ &i_{D_1}(t) = 0A,\ i_{C_1}(t) = i_{C_2}(t) = i_{D_2}(t) \end{aligned} \tag{4.13}$$

Combining (4.1) and (4.2) with the voltages in (4.13), equations (4.14) to (4.15) are obtained:

$$\begin{aligned} &v_{C_1}(t) = v_{C_2}(t) = \frac{1}{2}v_{in}(t) = \frac{v_0}{2}\sin(\omega t) \\ &v_{D_1}(t) = -\frac{v_0}{2}\sin(\omega t) \\ &v_{D_2}(t) = 0V \\ &v_{out}(t) = v_{C_2}(t) \end{aligned} \tag{4.14}$$

$$i_{C_1}(t) = i_{C_2}(t) = \omega\frac{v_0}{2}C_1\cos(\omega t) = \begin{cases} \omega t = 0 \Rightarrow i_{C_1}(t) = i_{C_2}(t) = \omega\frac{v_0}{2}C_1 \\ \omega t = \frac{\pi}{2} \Rightarrow i_{C_1}(t) = i_{C_2}(t) = 0A \end{cases} \tag{4.15}$$

So the output voltage varies in the same sinusoidal manner as the input voltage. Both of them evolve with the same phase and frequency. The difference is that the output voltage has half of the amplitude value from the input voltage. Fig. 3 demonstrates this.

As to the other voltage drops, v_{C_1} is equal to v_{C_2} during this interval. The voltages at the diodes can indicate when they are conducting (0V) or reversely polarized (negative voltages), blocking the currents to pass through.

In the sequence, Fig. 4 prints the currents as calculated in (4.15). During this interval, because the diode 1 is not conducting, all the current which passes through the capacitor 1 flows to the diode 2 (the same output current).

Both Fig.s 3 and 4 are plots of voltages and currents respecting the orientations established on the circuit from Fig. 1.

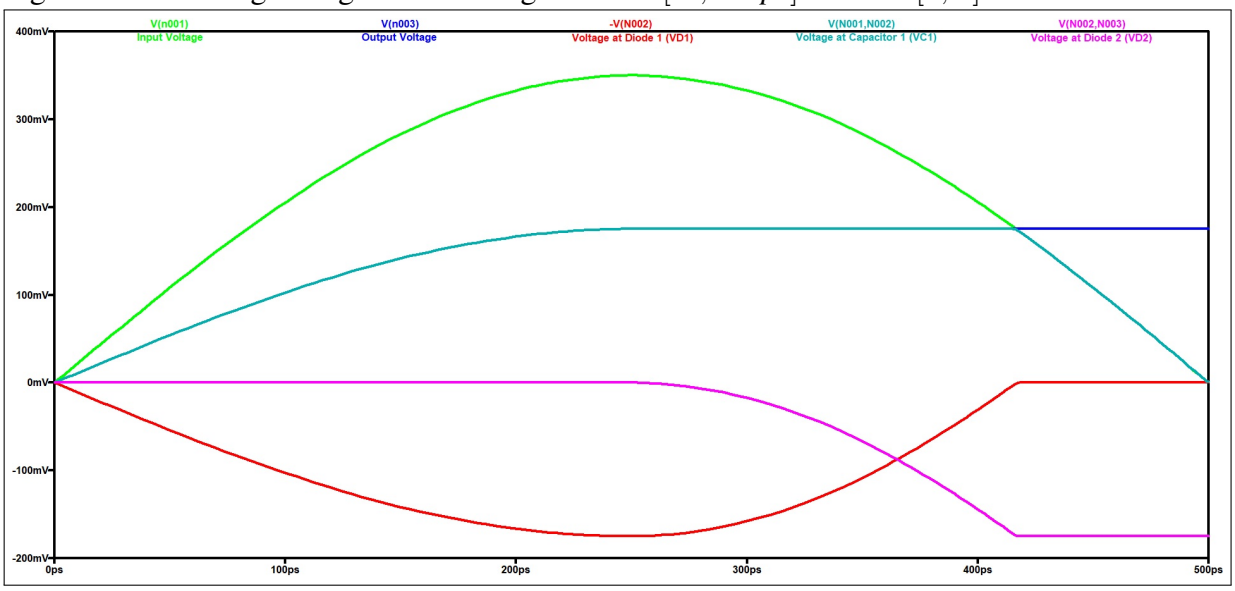
4.1.2 The second time interval

The analysis continues in the second time interval - as well comprised on the plots from Fig.s 3 and 4 - which results on the *radians*' interval:

$$\text{For } t \in [250ps, 417ps] \Rightarrow \omega t \in [\pi/2, 5\pi/6] \tag{4.16}$$

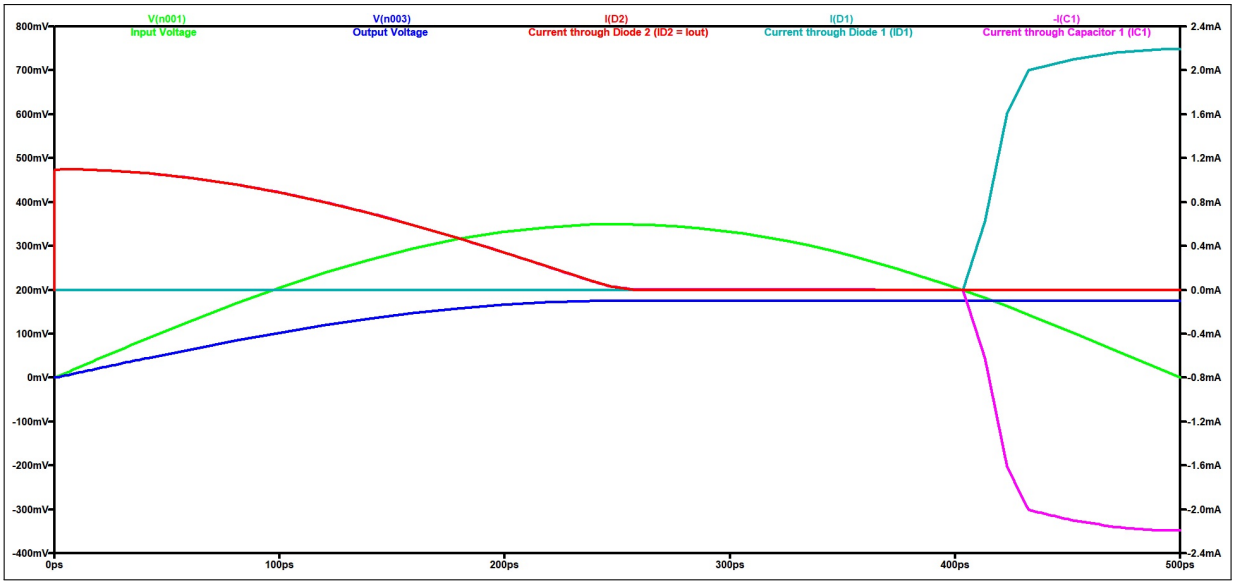
During this interval, the input voltage drops to a value below its maximum, which was divided equally in half between both capacitors. Thus, the voltage at the diode 2 drops to under 0V and so no current flows anymore through the circuit. The capacitors remain, hence, with their voltages constant at $v_0/2$.

Figure 3 – The Single Stage DVM voltages for $t \in [0s, 500ps] \Rightarrow \omega t \in [0, \pi]$



Source: the author.

Figure 4 – The Single Stage DVM currents for $t \in [0s, 500ps] \Rightarrow \omega t \in [0, \pi]$



Source: the author.

$$v_{D_1}(t) < 0V \Rightarrow i_{D_1}(t) = 0A$$
$$v_{D_2}(t) < 0V \Rightarrow i_{D_2}(t) = 0A \tag{4.17}$$

$$v_{C_1}(t) = \frac{v_0}{2}$$
$$v_{C_2}(t) = \frac{v_0}{2} \tag{4.18}$$

$$i_{C_1}(t) = 0A$$
$$i_{C_2}(t) = 0A \tag{4.19}$$

4.1.3 The third time interval

$$\text{For } t \in [417ps, 750ps] \Rightarrow \omega t \in [5\pi/6, 3\pi/2] \tag{4.20}$$

During the interval (4.20), the diode 2 is still not conducting, implying that the voltage at the capacitor 2 (the same output voltage) remains constant at $v_0/2$. But now, the input voltage has reached the same voltage level of the capacitor 1 ($v_0/2$) and further drops below this level, setting the diode 1 in direct polarity (conducting).

Current flows on the opposite direction through the capacitor 1 and its voltage follows the exact same value of the input voltage until the source reaches its lowest voltage, -350mV ($-v_0$) at t = 750ps.

$$i_{C_2}(t) = i_{D_2}(t) = 0A \Rightarrow v_{C_2}(t) = \frac{v_0}{2} \tag{4.21}$$

$$v_{D_1}(t) = 0V \Rightarrow i_{D_1}(t) = -i_{C_1}(t) \tag{4.22}$$

$$v_{C_1}(t) = v_{in}(t) = v_0 \sin wt = \begin{cases} \omega t = \frac{5\pi}{6} \Rightarrow v_{C_1}(t) = \frac{v_0}{2} \\ \omega t = \frac{3\pi}{2} \Rightarrow v_{C_1}(t) = -v_0 \end{cases} \tag{4.23}$$

$$i_{C_1}(t) = C_1 \frac{dv_{C_1}(t)}{dt} = C_1 v_0 \omega \cos \omega t = \begin{cases} \omega t = \frac{5\pi}{6} \Rightarrow i_{C_1}(t) = -\frac{\sqrt{3}}{2} C_1 v_0 \omega \\ \omega t = \frac{3\pi}{2} \Rightarrow i_{C_1}(t) = 0A \end{cases} \tag{4.24}$$

Fig.s 5 and 6 are the plots for the (4.21) to (4.24). The time ranges from 0.25ns until the upper limit of the interval (4.20), 0.75ns.

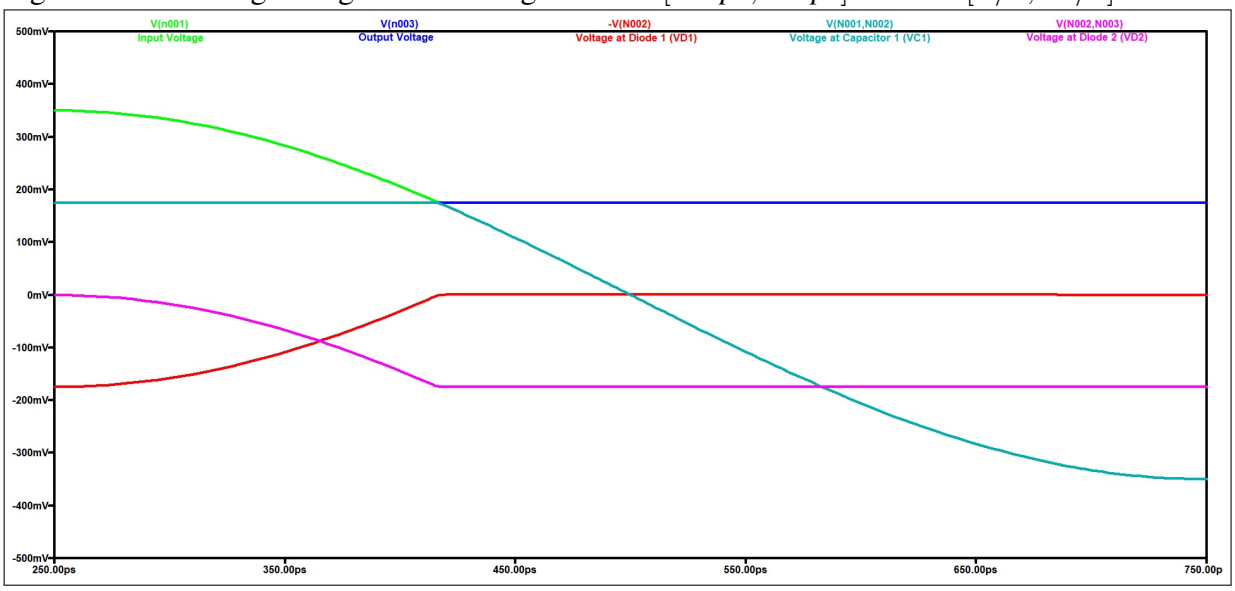
4.1.4 The fourth time interval

$$\text{For } t \in [750ps, 833ps] \Rightarrow \omega t \in [3\pi/2, 10\pi/6] \tag{4.25}$$

Here, the output voltage will range from $-v_0$ at $t = 750ps$ until $-v_0/2$ at $t = 833ps$. By (4.1) and (4.24), the increment in the input voltage will reversely polarize the diode 1, blocking the current flow through it:

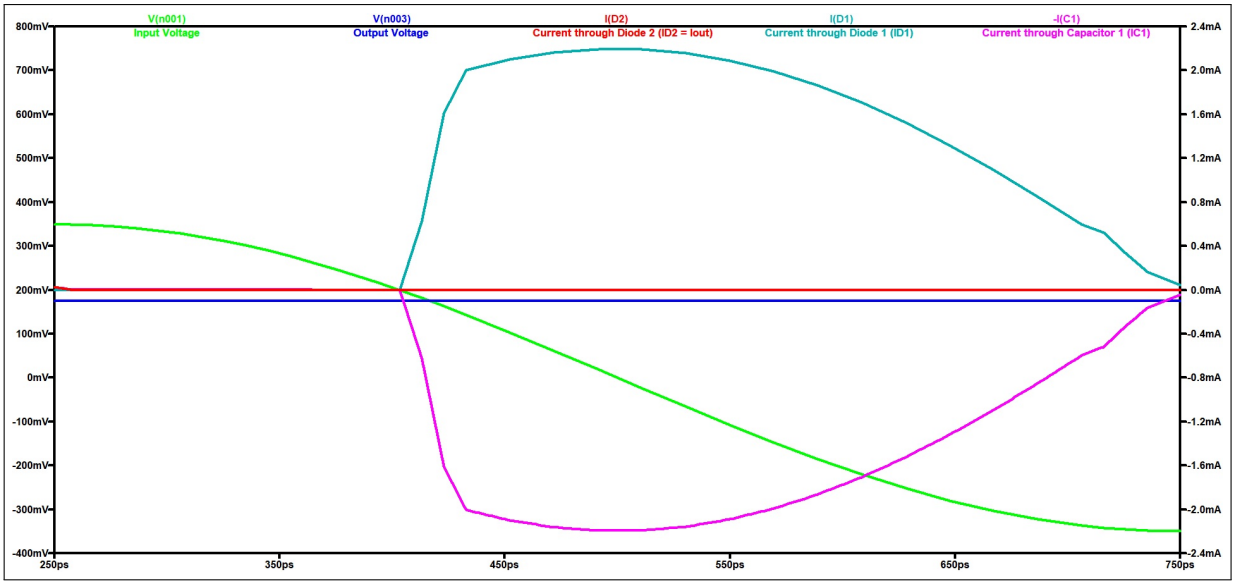
$$\begin{aligned} v_{D_1}(t) < 0V \Rightarrow i_{D_1}(t) = 0A \\ v_{D_2}(t) < 0V \Rightarrow i_{D_2}(t) = 0A \end{aligned} \tag{4.26}$$

Figure 5 – The Single Stage DVM voltages for $t \in [250ps, 750ps] \Rightarrow \omega t \in [\pi/2, 3\pi/2]$



Source: the author.

Figure 6 – The Single Stage DVM currents for $t \in [250ps, 750ps] \Rightarrow \omega t \in [\pi/2, 3\pi/2]$



Source: the author.

Thus, no current will flow through the whole circuit, implying that the voltages at the capacitors will remain the same, since they won't discharge.

$$\begin{aligned} i_{C_1}(t) = 0A \Rightarrow v_{C_1}(t) = -v_0 \\ i_{C_2}(t) = 0A \Rightarrow v_{C_2}(t) = \frac{v_0}{2} \end{aligned} \tag{4.27}$$

The plots of voltages and currents are on the Fig.s 7 and 8 at the next subsection.

4.1.5 The fifth time interval

$$\text{For } t \in [833ps, 1.25ns] \Rightarrow \omega t \in [10\pi/6, 5\pi/2] \tag{4.28}$$

At $t = 833ps$, the input voltage reaches a value of $-v_0/2$, by (4.1) and (4.2) the voltage at the diode 2 becomes 0V again, and it resumes conducting current:

$$\begin{aligned} &v_{D_1}(t) < 0V \Rightarrow i_{D_1}(t) = 0A \\ &v_{D_2}(t) = 0V \Rightarrow i_{D_2}(t) \geq 0A \end{aligned} \tag{4.29}$$

Taking (4.1), (4.2), (4.3), (4.4) and the capacitors' current to voltage relations (4.7) and (4.8), they all result in:

$$\begin{aligned} &v_{C_1}(t) + v_{C_2}(t) = v_{in}(t) \\ &\text{Because } i_{C_1}(t) = i_{C_2}(t), \\ &v_{C_1}(t = 833ps) + v_{C_2}(t = 833ps) + 2\int_{833ps}^{t} i_{C_1}(\tau)\, d\tau = v_{in}(t) \\ &\frac{v_0}{2} - v_0 + 2\int_{833ps}^{t} i_{C_1}(\tau)\, d\tau = v_{in}(t) \\ &\int_{833ps}^{t} i_{C_1}(\tau)\, d\tau = \frac{v_{in}(t) + \frac{v_0}{2}}{2} = \frac{v_{in}(t)}{2} + \frac{v_0}{4} \end{aligned} \tag{4.30}$$

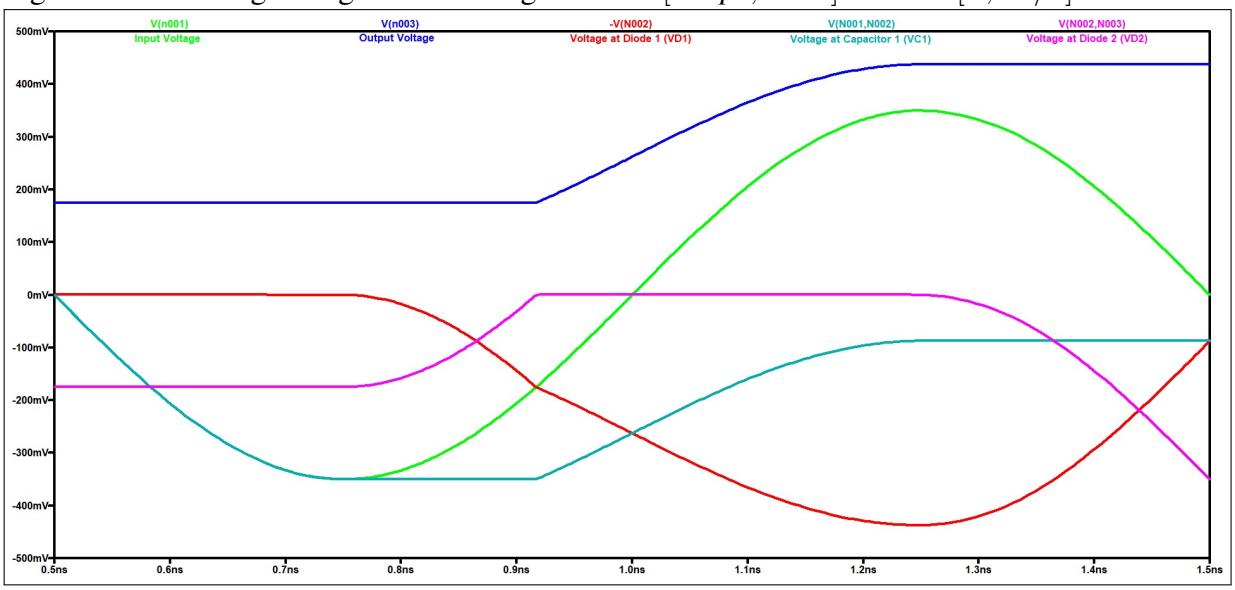
$$\begin{aligned} &v_{C_1}(t) = -v_0 + \int_{833ps}^{t} i_{C_1}(\tau)\, d\tau = -\frac{v_0}{2} + \frac{v_{in}(t)}{2} = \\ &= \begin{cases} t = 833ps \Rightarrow v_{C_1}(t) = -v_0 = -350mV \\ t = 1.5ns \Rightarrow v_{C_1}(t) = 0V \end{cases} \\ &v_{C_2}(t) = \frac{v_0}{2} + \int_{833ps}^{t} i_{C_1}(\tau)\, d\tau = \frac{3v_0}{4} + \frac{v_{in}(t)}{2} = \\ &= \begin{cases} t = 833ps \Rightarrow v_{C_2}(t) = \frac{v_0}{2} = 175mV \\ t = 1.083ns\ (\omega t = 2\pi + \frac{\pi}{6}) \Rightarrow v_{C_2}(t) = v_0 = 350mv \\ t = 1.5ns \Rightarrow v_{C_2}(t) = \frac{5v_0}{4} = 437.5mV \end{cases} \end{aligned} \tag{4.31}$$

By the equations and values obtained in (4.31), it is possible to see that after 1 complete cycle and a sixth of another cycle ($\simeq$ 1.083ns) the output voltage , which previously

reached 175mV (half of the maximum input voltage), now attained the same 350mV and will surpass this value. From this point on, the effect of voltage increasing begins.

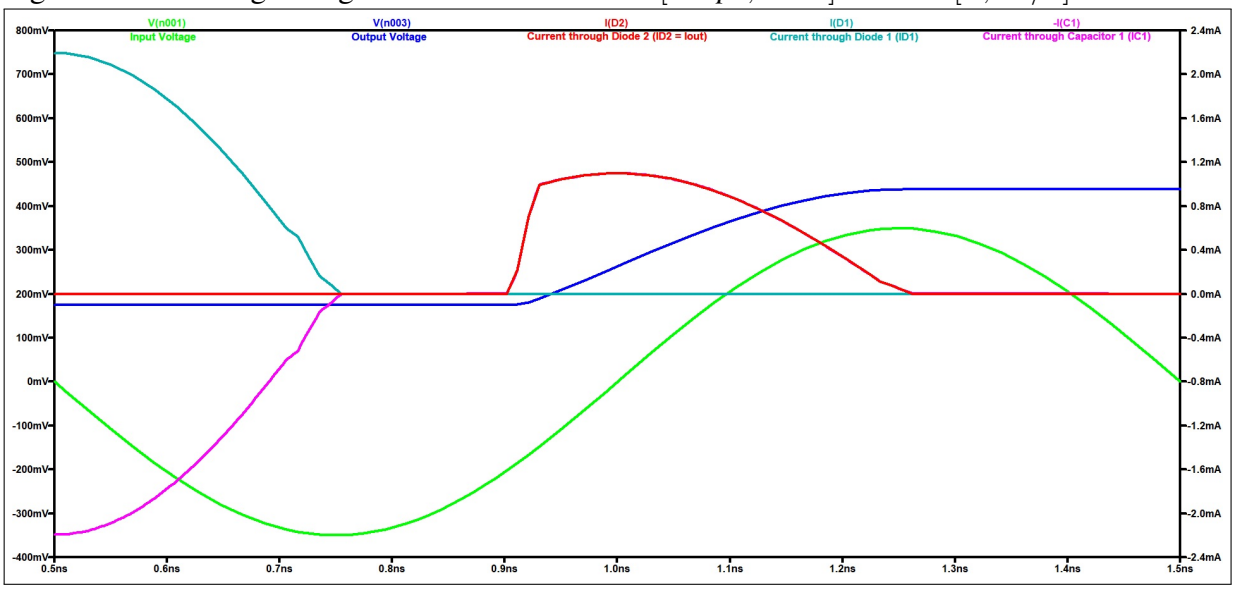
Fig.s 7 and 8 demonstrate those behaviors on the plots. The time domain of those plots ranges from 0.5ns to 1.5ns. The interval (4.28) is comprised and also the previous fourth interval (4.25).

Figure 7 – The Single Stage DVM voltages for $t \in [500ps, 1.5ns] \Rightarrow \omega t \in [\pi, 5\pi/2]$



Source: the author.

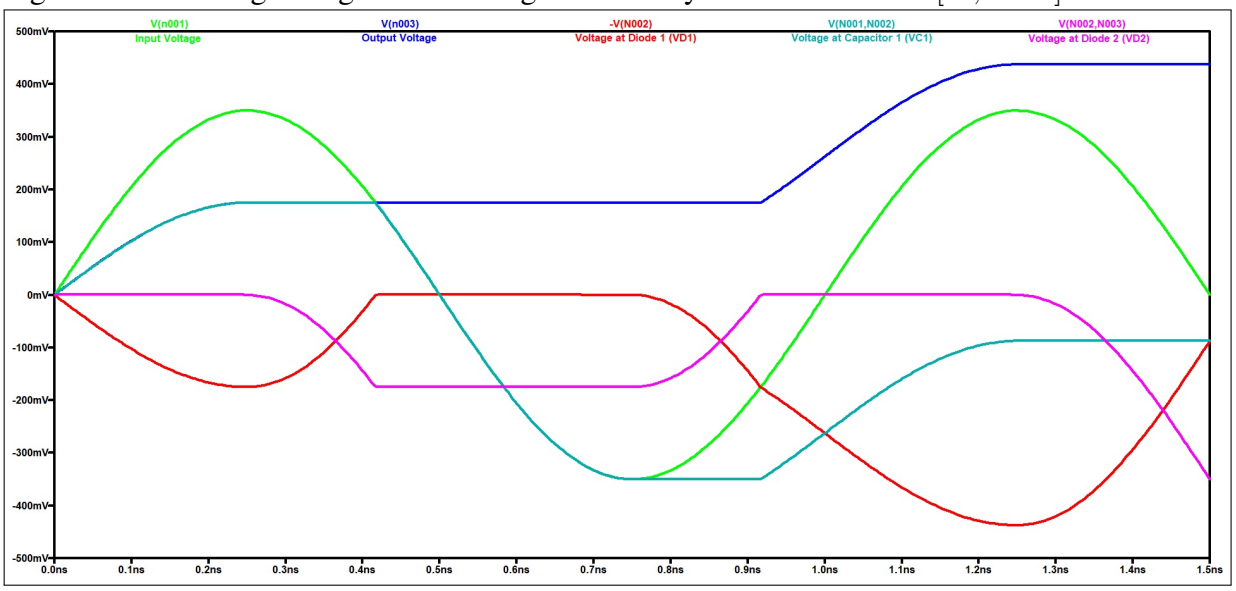
Figure 8 – The Single Stage DVM currents for $t \in [500ps, 1.5ns] \Rightarrow \omega t \in [\pi, 5\pi/2]$



Source: the author.

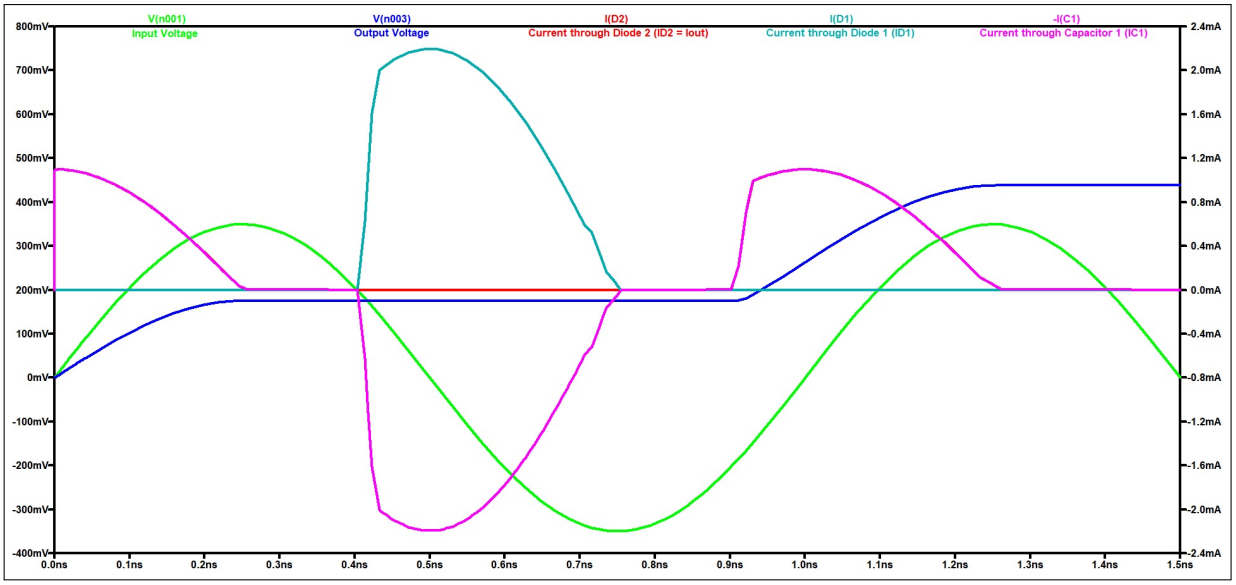
Finally, the complete first cycle and the first half of the next cycle of the Single Stage DVM circuit are plotted on Fig.s 9 and 10.

Figure 9 – The Single Stage DVM voltages for one cycle and a half: $t \in [0s, 1.5ns]$



Source: the author.

Figure 10 – The Single Stage DVM currents for one cycle and a half: $t \in [0s, 1.5ns]$



Source: the author.

4.1.6 Single Stage's Stable State

The DVM of only one stage reaches stable state after some cycles operating. Until then, the output voltage is gradually increased. After the 5 intervals explained on the previous subsection, the circuit's behaviour restarts and the fifth interval (4.28) already presents some of the features from the first interval (4.13).

The differences between the beginning of the operation and further operation points are the voltage levels of the capacitors and of the diodes. Capacitor 1's voltages are gradually decreasing and capacitor 2's gradually increasing following the same variations at the same

phases (ωt) at all cycles.

Just like in (4.31), and each subsequent cycle, the capacitors' voltage levels change based on their previous charges. This directly impacts on the terms: $v_{C_1}(t_0)$ and $v_{C_2}(t_0)$ from (4.7) and (4.8), when t_0 is equal to the instant of time preceding the decreasing of $v_{C_1}(t)$ and increasing of $v_{C_2}(t)$ at each cycle.

Those variations continue for the capacitor 2 until the output voltage, $v_{C_2}(t)$, has reached its maximum value, around 700mV. For the capacitor 1, when its voltage, $v_{C_1}(t)$, has also reached a stable point at a voltage level of -350mV.

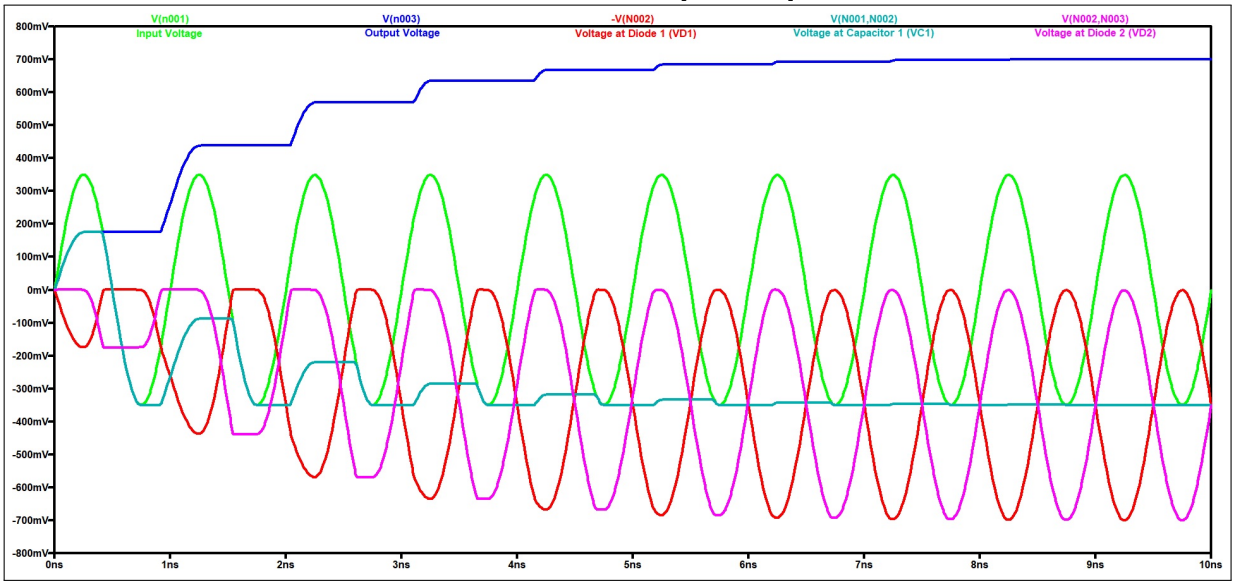
As to the diodes' voltages, as the circuit operates through the cycles, eventually they stabilize at oscillations similar to the oscillation of the input voltage: same sinusoidal variation, same frequency and same peak-to-peak voltages.

But the phases of the voltages are different: $v_{D_2}(t)$ and $v_{in}(t)$ are in phase and $v_{D_1}(t)$ and $v_{in}(t)$ are out of phase by 180 degrees. The last difference is that both diodes have in their voltages a DC component of -350mV.

Fig.s 11 and 12 display the plots demonstrating the behaviors described in this subsection. The stable state is reached at around 9ns, when the output voltage reaches the double of the maximum of the input voltage, 700mV, and has such a slow and low oscillation that it can be considered DC voltage.

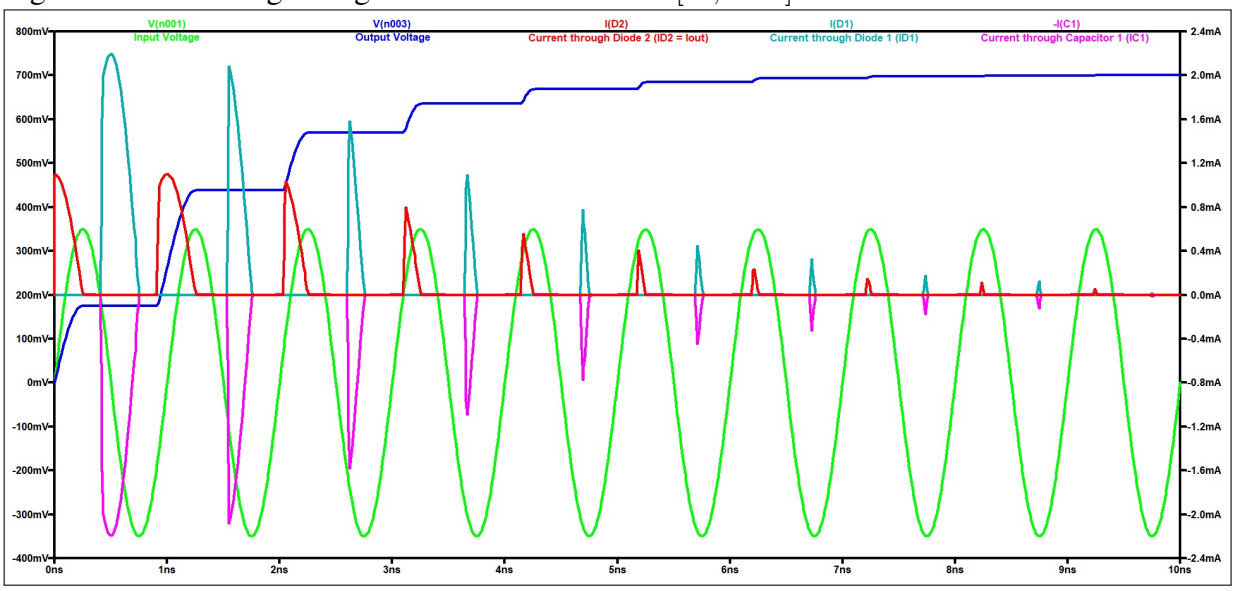
So the DVM has "doubled"the input voltage and has converted it from AC to DC.

Figure 11 – The Single Stage DVM voltages for $t \in [0s, 10ns]$



Source: the author.

Figure 12 – The Single Stage DVM currents for $t \in [0s, 10ns]$



Source: the author.

4.2 Real Elements on the Single Stage Dickson Voltage Multiplier

The points taken into account here are basically the existence of resistances previously not considered and the non-ideality of some elements. In this project, to transform the ideal circuit from Fig. 1 into a more realistic circuit, some considerations are added:

- Real semiconductors
- Source Resistance R_{source}
- Load Resistance R_{load}

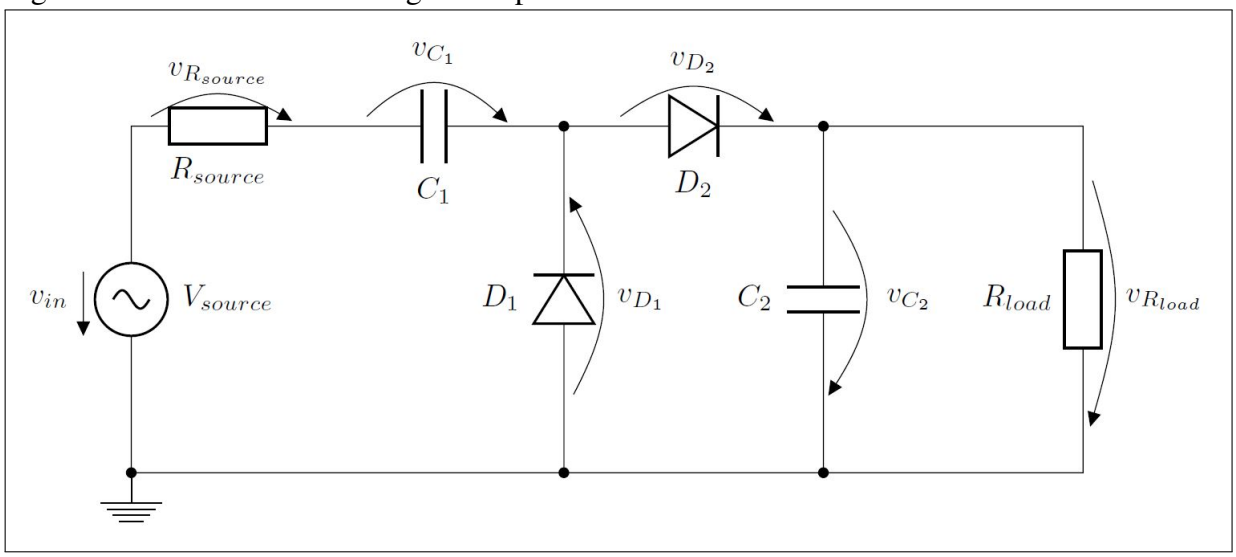
Basically, the three items will cause energy losses in the circuit. Nonetheless, they are not specified taking into consideration only this aspect. As it is explained in the subsections of this section, each of those three items count for other effects.

Besides those points, two important consideration which do not affect the design of the circuit: the sinusoidal voltage source of the circuit is, in reality, a built-in antenna receiving electromagnetic waves at a carrier-frequency of 900MHz and of 0dBm power.

For the DVM circuit's simulation, the sinusoidal voltage source of 350mV amplitude and the 1GHz frequency will be kept, since replacing them for their real counterparts would make no great difference on the results aimed at this chapter.

The circuit considered now is on Fig. 13.

Figure 13 – The Dickson Voltage Multiplier with real elements



Source: the author.

4.2.1 Non-ideal diodes

The diodes from section 4.1 were both ideal diodes, whose IV curve was printed in Fig. 2. They strictly follow the relations in (4.5) (or (4.6) for the second diode).

When non-ideal diodes are used, their IV curves should be noted, such as the curve in Fig. 15 from the simplest *LT Spice* non-ideal diode model. Practical diodes do not only have a higher threshold voltage, as the IV relation also follows an exponential relation, rather than the simple IV relations aforementioned.

The plot on Fig. 15 was generated using, in *LT Spice*, the same circuit as the circuit of Fig. 14. The simulation sweeps the voltage source V_{in} from -400mV up to 800mV.

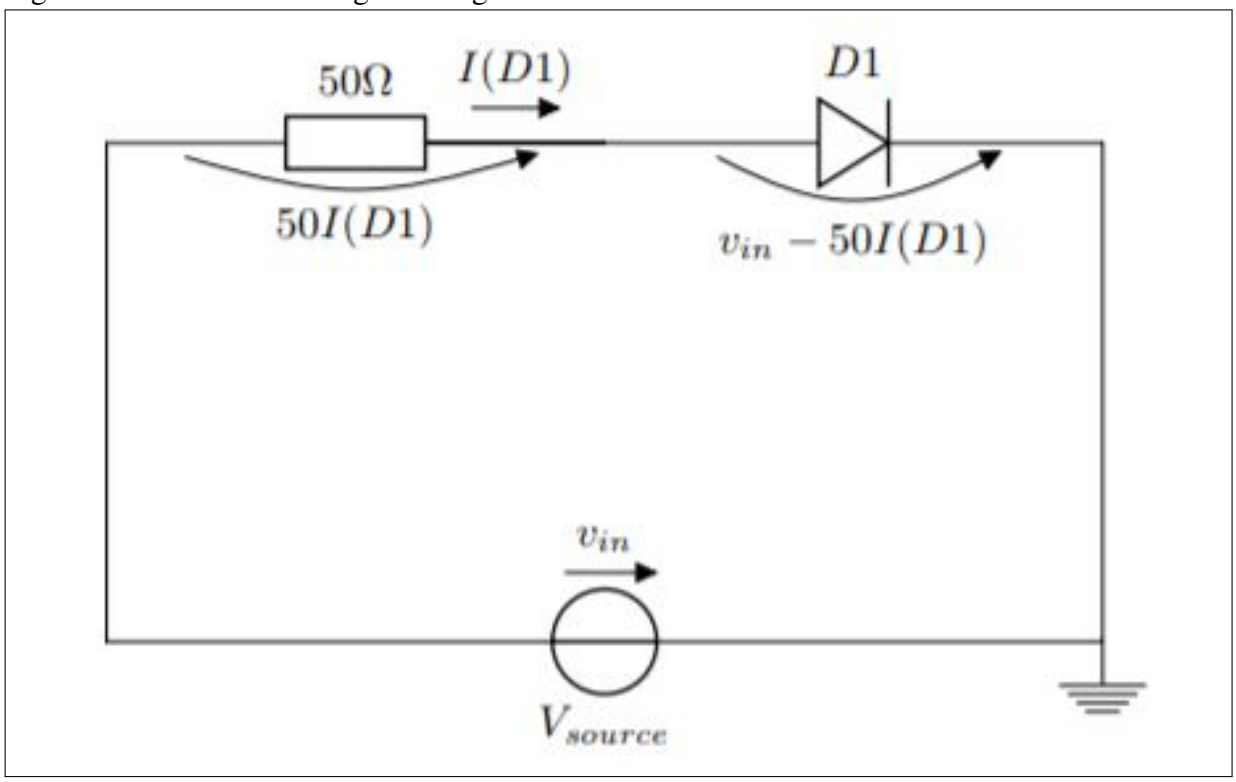
Unfortunately, this forward-biased threshold voltage of the diode is too large for an application whose input voltage's amplitude is in the order of 350mV. If such a diode is put inside the circuit, the diodes will never conduct.

So an element with lower threshold voltage is required, and it would be a Schottky diode, a diode whose forward-biased threshold voltage is lower than normal silicon diodes. Unfortunately, *LT Spice* has not a good model for the Schottky diode, which basically reproduces the behavior on Fig. 15.

Thus, the same silicon diode is modified using *directives* (commands) in *LT Spice*. For this case, only one directive is written, which changes the threshold voltage to whichever value is wanted.

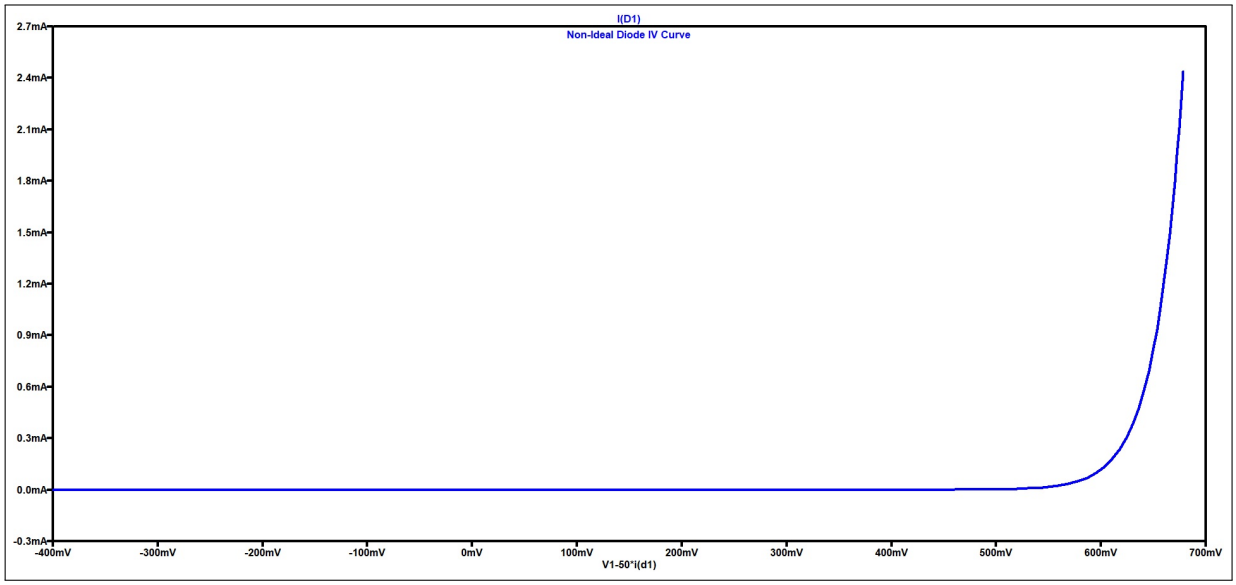
In order to have more realistic results when using this modified model of the diode,

Figure 14 – Schematic for generating the IV curve of the non-ideal diode



Source: the author.

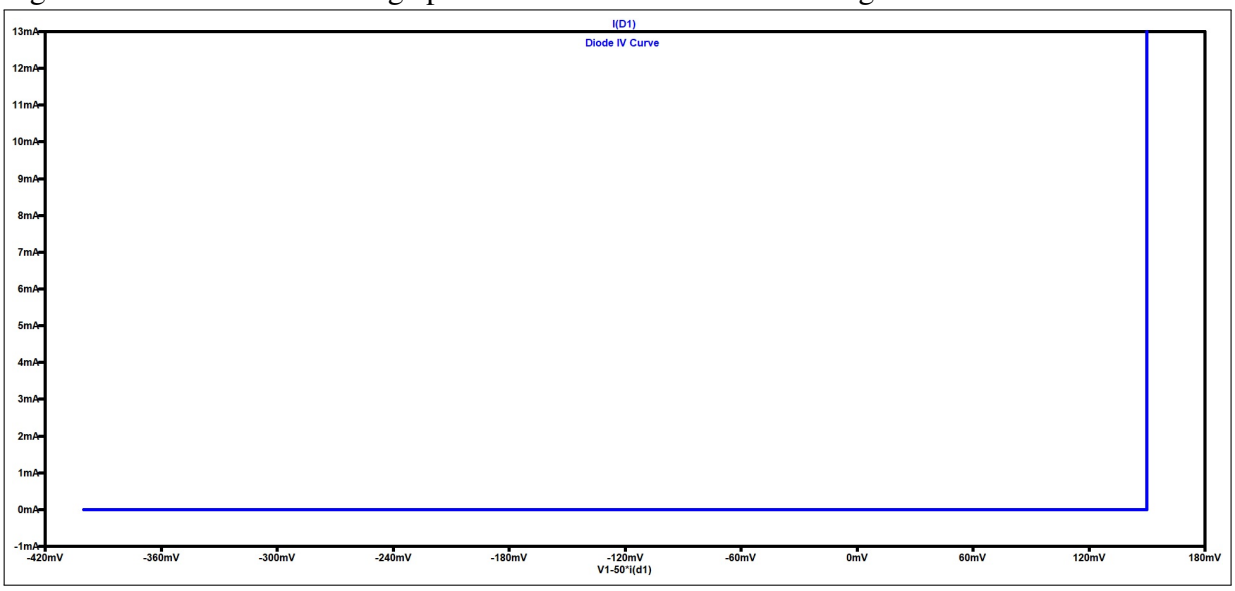
Figure 15 – The current-voltage plot of the non-ideal diode



Source: the author.

the threshold voltage is changed to 150mV, an achievable value for Schottky diodes. However, this directive also modifies the behavior of the IV curve, turning it into an ideal behavior, whose

Figure 16 – The current-voltage plot of the 150mV threshold voltage diode



Source: the author.

characteristic can be written as in (4.32) and seen on Fig. 16.

$$\begin{cases} v_{D1}(t) < 150mV \Rightarrow i_{D1}(t) = 0A \\ i_{D1}(t) > 0A \Rightarrow v_{D1}(t) = 150mV \end{cases} \tag{4.32}$$

4.2.2 Diode connected NMOS transistor

A diode whose forward biased threshold voltage is of a few millivolts (150mV in the previous case) fits perfectly inside the circuit when simulating. On real applications, when making the integrated circuit, it does not fit that well.

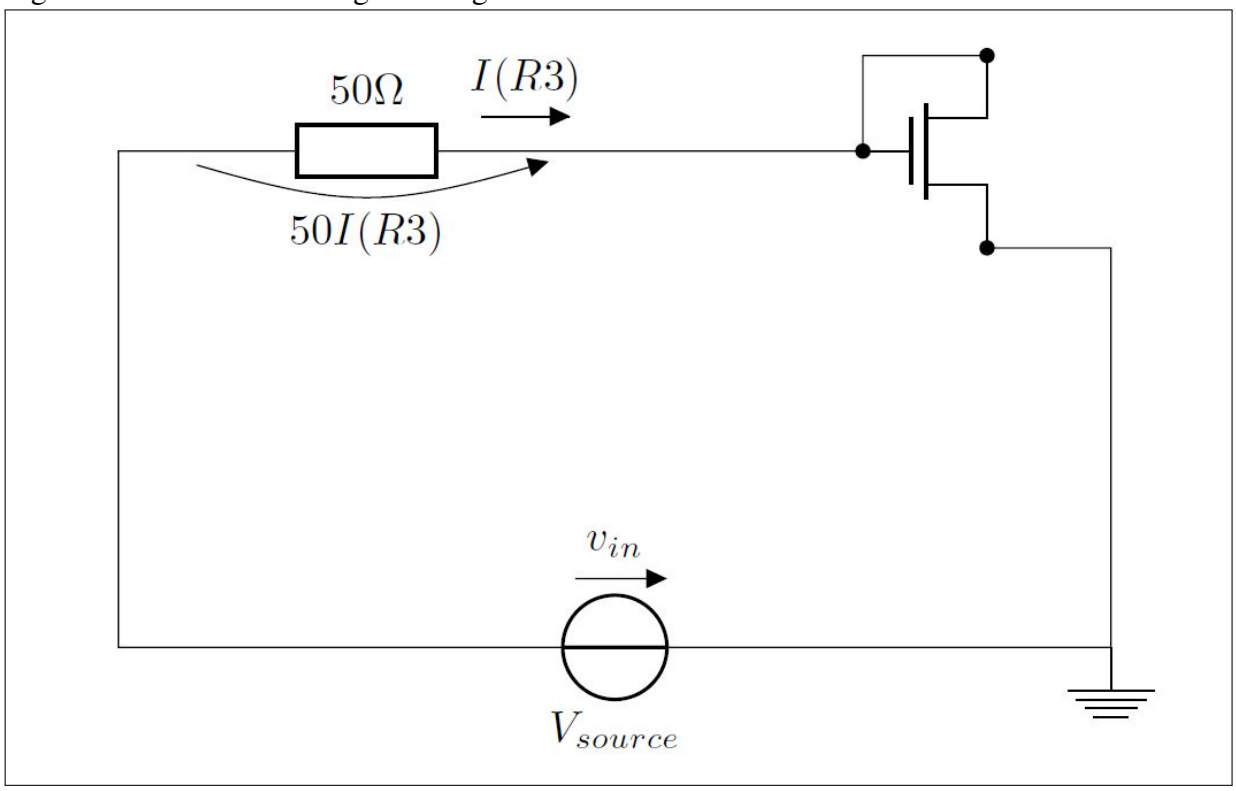
The manufacturing of an integrated circuit involves using the same technology for every component. Diodes are not usually available for applications inside integrated CMOS circuits due to their lack in the technologies used.

A possibility is to employ NMOS transistors to behave as diodes. Typically, NMOS transistors are small in size, have good electron mobility and many circuits have them integrated, important features to confirm that such transistors are good choices.

An NMOS transistor can show diode characteristics when the drain and the gate terminals are connected. Fig. 17 pictures the equivalent circuit of the diode schematic on Fig. 14 using an NMOS transistor.

Fig. 18 shows the IV curve of such a schematic, where $v_{in} - 50I(R3)$ is the voltage at the NMOS transistor. It is confirmed that connecting a NMOS transistor in this fashion produces

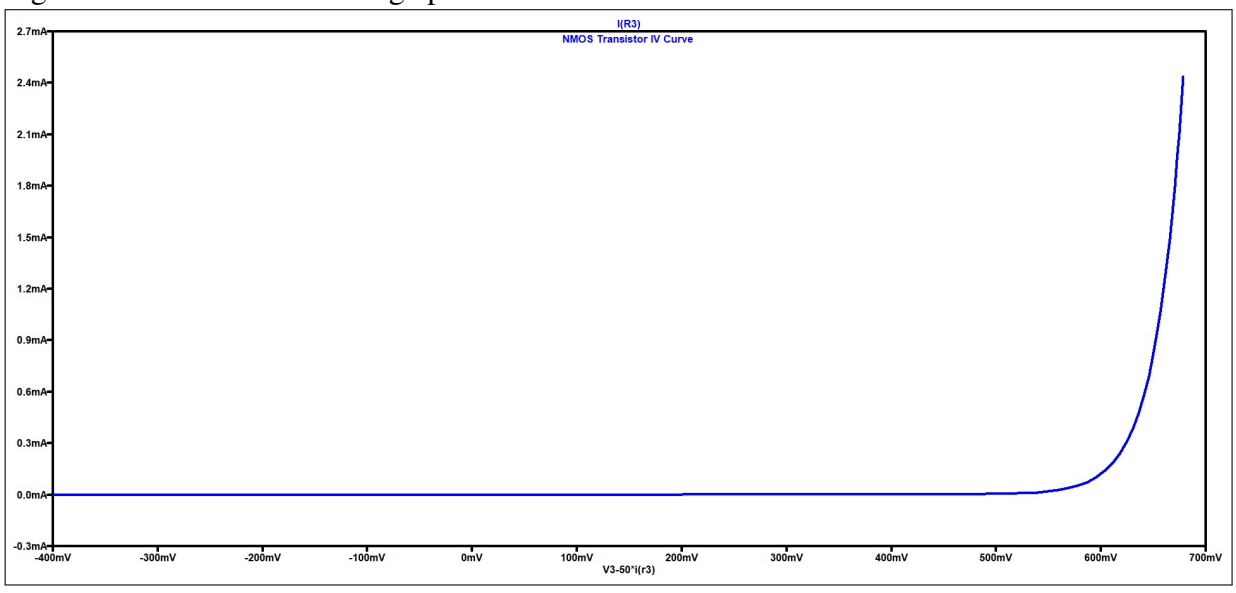
Figure 17 – Schematic for generating the IV curve of the diode connected NMOS transistor



Source: the author.

a similar effect of the diode.

Figure 18 – The current-voltage plot of the diode connected NMOS transistor



Source: the author.

Unfortunately, *LT Spice* has again shown some limitations: it was not possible to find an NMOS transistor model whose "threshold voltage"is less or equal to 200mV. Below that voltage level, the circuit is not guaranteed to work properly. It was neither found how to change

the "threshold voltage"level using an *LT Spice* directive.

Therefore, the theories and simulations involving NMOS transistors in this chapter 4 are developed and done using the diode whose IV curve is on Fig. 16. Despite not having the exponential behavior characteristic of real diodes, it does not affect the main effect of causing voltage division when it is forward biased (150mV over the diode when conducting).

The use of NMOS transistors is resumed in chapter 6.

4.2.3 Source Resistance

The sinusoidal voltage source of the simulations is, as mentioned before in the beginning of section 4.2, an antenna. This antenna should be modeled as a voltage source with a series resistance, to have more accurate simulations. The existence of a source resistance consumes power, so it should be minimum, of about 50Ω.

50Ω is a valid choice for an antenna output resistance as it is achievable by manufactures in reality. But, this resistance must be varied in order to check what kind of impact a source resistance has in the Dickson Voltage Multiplier.

In this case, for the circuit in the Fig. 13, the load resistance should be removed and the open circuit terminals kept -as in Fig. 1. Also, the diodes should be ideal. In this way, only the effect of changing the source resistance stands out.

In the sequence, two simulations are presented: the first (Fig. 19) plots all the voltages over the elements of the circuit for 50Ω at the source resistance; the second (Fig. 20) plots all the output voltages for the different source resistances' values.

Fig. 19 resembles Fig. 11 from the ideal circuit. The difference lies on the small impact that the 50Ω causes on the circuit: the output voltage reaches only 690mV (approximately) in stable state, whereas the ideal circuit reaches 700mV. So there's a loss of 10mV.

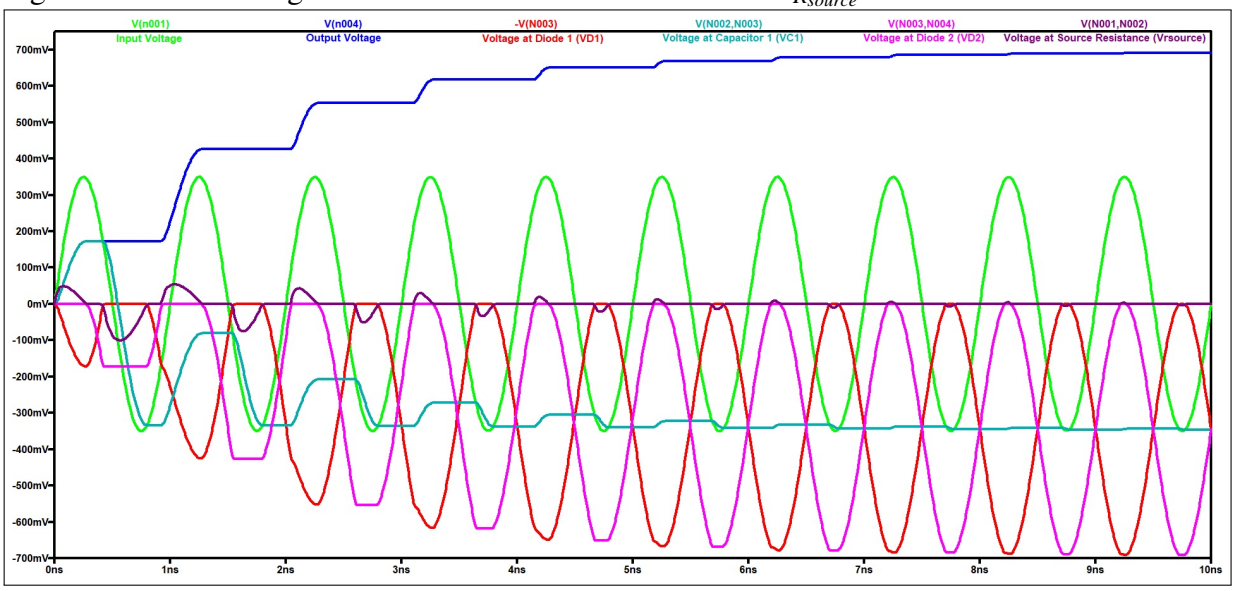
On Fig. 20, the reason for the worse output voltages when R_{source} is greater than 50Ω is the time constant of the capacitor C_1 and the source resistance R_{source}.

$$\tau = R \times C \tag{4.33}$$

For the capacitor 1 and the source resistance:

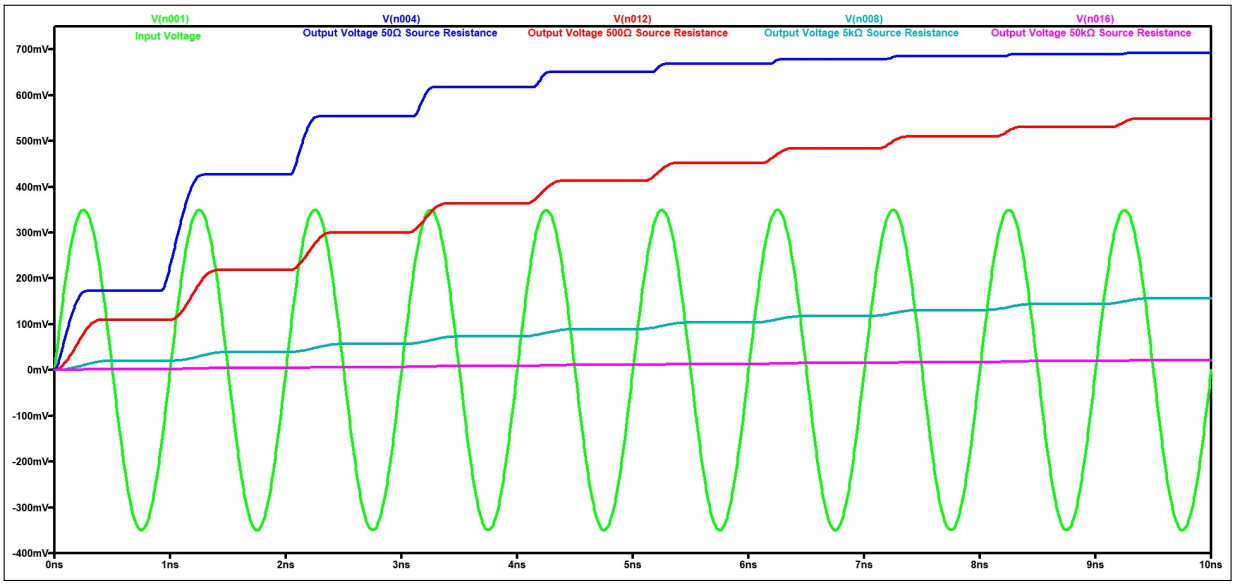
$$\tau = R_{source} \times C_1 \tag{4.34}$$

Figure 19 – The voltages at the elements of the DVM when $V_{R_{source}} = 50\Omega$



Source: the author.

Figure 20 – The output voltages for different R_{source} values



Source: the author.

$$\tau = R \times C = \begin{cases} \text{when } R = 50\Omega \Rightarrow 50\Omega \times 1pF = 50ps \\ \text{when } R = 500\Omega \Rightarrow 500\Omega \times 1pF = 500ps \\ \text{when } R = 5k\Omega \Rightarrow 5k\Omega \times 1pF = 5ns \\ \text{when } R = 50k\Omega \Rightarrow 50k\Omega \times 1pF = 50ns \end{cases} \tag{4.35}$$

The higher the value of R_{source}, the higher the time constant (equation (4.35) demonstrates it) and the slower capacitor 1 will charge and discharge. If the time constant is very small, capacitor 1 will charge and discharged as quickly as necessary to ensure the circuit's functioning.

In section 4.1, for the time intervals DVM circuit's equations were derived and its behavior analyzed. Back then, the voltage levels of the capacitor 1 were important for creating voltage references responsible for forward or backward biasing the diodes 1 and 2 as the input voltage levels rise above or fall below the capacitor 1's voltage levels.

For a 50Ω source resistance and capacitor 1 with 1pF, the time constant is equal to 50ps, which is 20 times smaller than the period of a 1GHz frequency wave (1ns). This way the voltage at the capacitor 1 can behave properly because it can change faster than the input voltage.

On the other hand, for a 50kΩ source resistance, the time constant is equal to 50ns (50 times higher than one cycle's period). In such an amount of time, the capacitor 1 will never have appropriate charge and discharge cycles during one period, as the input voltage rises and falls.

4.2.4 Load Resistance

Usually, since there's a source resistance in the circuit, the normal procedure is to have the load resistance chosen to pair it. This procedure is known as impedance matching, meant for achieving maximum power transfer (Jacobi's Law) from the source to the load. In order to do this, the load resistance should be modelled as having the same resistance of the source, 50Ω.

However, power transfer is not the only issue to be concerned. The next simulations will show that there is a huge impact on the output voltage when those resistances vary.

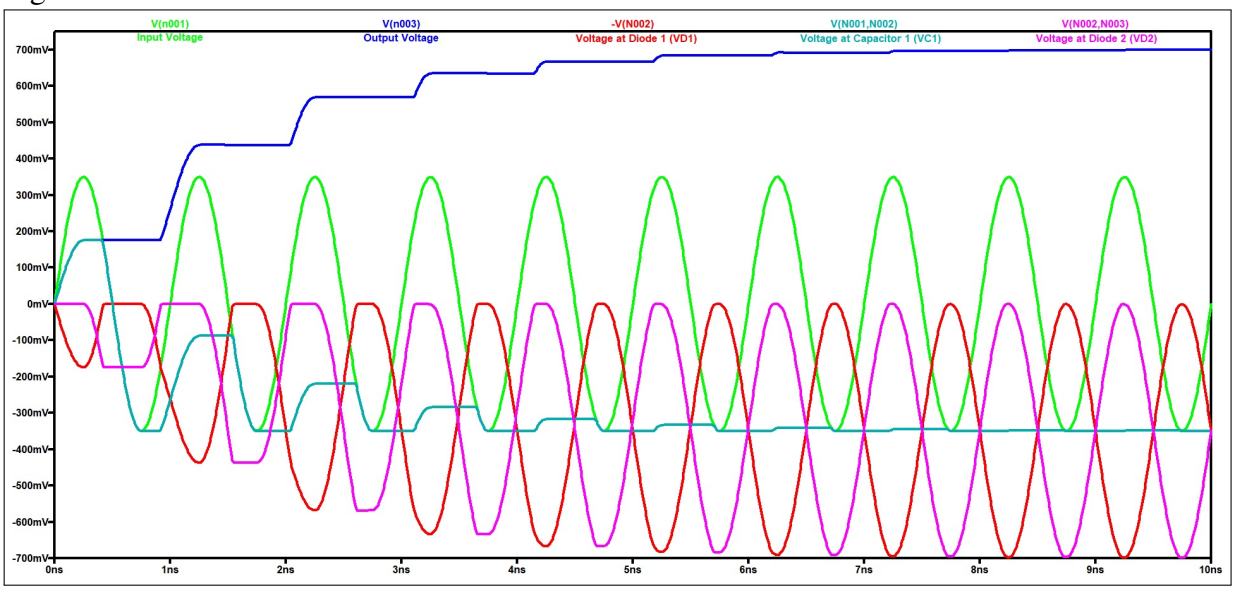
As seen on the ideal Dickson Voltage Multiplier circuit (Fig. 1), the load impedance should be as high as possible to achieve a similar effect of an open circuit section. So, the first simulation (Fig. 21) starts with a very large resistance, of 1MΩ, and Fig.22 plots the output voltages for each load resistance.

The schematic used for performing those simulations is the circuit on Fig. 13, where R_{load} varies from 1MΩ to 1kΩ, the source resistance was removed -and is now a short circuit- and the diodes are ideal.

As it can be seen, curve on Fig. 21 is almost equal to the ideal circuit's curve on Fig. 11. The output voltage on the stable state reaches 700mV, equal to the ideal circuit's case.

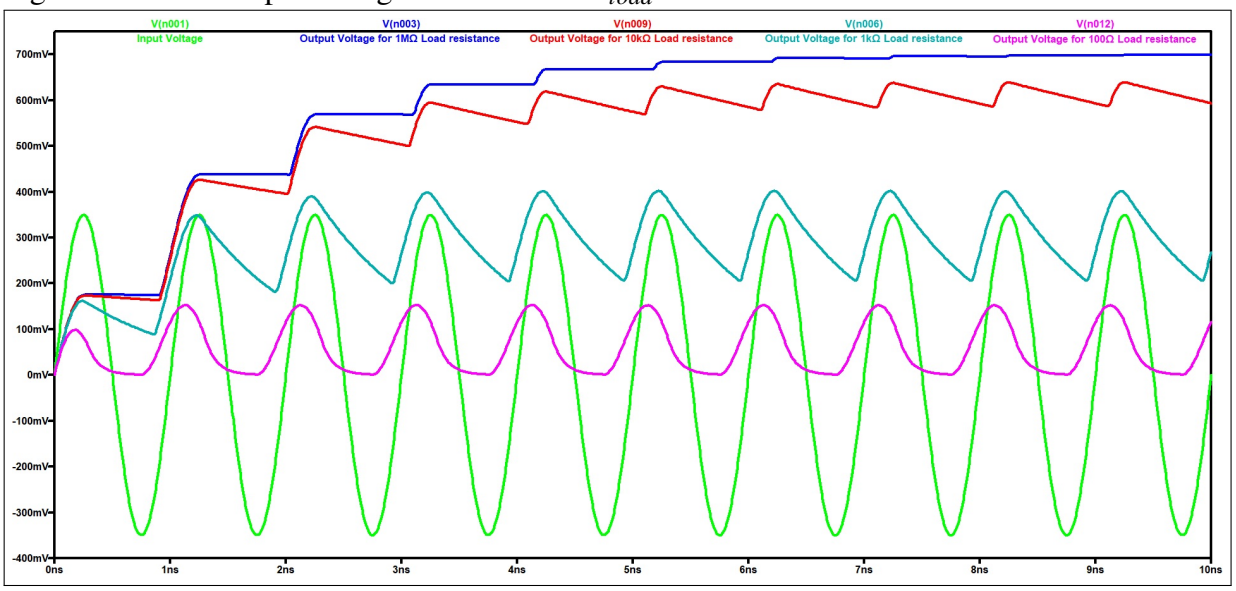
This happens, again, due to the time constant of the capacitor 2 and the resistor R_{load}.

Figure 21 – The real DVM circuit with 1MΩ load resistance



Source: the author.

Figure 22 – The output voltages for different R_{load} values



Source: the author.

Taking again (4.33), (4.36) is derived for the different values of the load resistance.

$$\tau = R \times C = \begin{cases} \text{when } R = 1M\Omega \Rightarrow 1M\Omega \times 1pF = 1\mu s \\ \text{when } R = 10k\Omega \Rightarrow 10k\Omega \times 1pF = 10ns \\ \text{when } R = 1k\Omega \Rightarrow 1k\Omega \times 1pF = 1ns \\ \text{when } R = 100\Omega \Rightarrow 100\Omega \times 1pF = 100ps \end{cases} \tag{4.36}$$

Initially, as seen on the time intervals in section 4.1, diode 2 is conducting and diode 1 is not. During that time, capacitor 2 is charged up to a certain voltage before diode 2 is reversely

biased.

When diodes 2 is not conducting and capacitor 2 is not charging anymore, a circuit comprising capacitor 2 and the load resistance forms. In this "temporary"circuit, the capacitor works as a source to the load, and discharges the accumulated energy on the load.

If the time constant for this association (capacitor 2 and load resistance) is as big as 1μs (for 1MΩ), compared to the 1ns period of the input voltage (one thousandth of 1μs), the capacitor will discharge so slowly that the voltage level over it remains almost constant while the diode 2 is not conducting (blue line in Fig. 22).

In other words, if the time constant is many times higher than the input voltage's period, capacitor 2 discharges many times slower than it recharges.

On the other hand, if the time constant is as small as 1ns (for 1kΩ load resistance), the capacitor 2 does not hold the voltage level for enough time, because it discharges (while diode 2 is not conducting) before diode 2 begins to re-conduct and it resumes recharging (gray line in 22).

4.2.5 Conclusion on the elements

Regarding the capacitances and the resistances on the circuit: there's a trade-off which must be considered between these two points and the frequency of operation.

As seen in the subsections 4.2.3 and 4.2.4, the resistances' sizes are designed based on values of the time constants which guarantee the proper functioning of the circuit

If the source resistance or the capacitance 1 (Fig. 13) should be changed, subsection 4.2.3 explains that the time constant (equation 4.34) must be many times smaller than the input voltage's period (1ns). For the standard values, the time constant is equal to 50ps, 20 times smaller than the period.

According to Fig. 20 and (4.35), if the source resistance is raised, the capacitance must be diminished in the same proportion, so the time constant remains the same.

For example, if the source resistance changes from 50Ω to 1kΩ, capacitor 1 must shrink more than 20 times, to less than 50fF. Another option is to work with waves whose periods are 20 times greater, in other words frequencies 20 times smaller.

In the case of the load resistance and of the capacitor 2, according to Fig. 22 and (4.36) if the load resistance shrinks the time constant turns too small compared to the period of 1ns and the circuit's operation fails. So if the load resistance should shrink, capacitance 2 must

be enlarged in the same proportion to keep the same time constant.

For example, for a new load resistance of 10kΩ, the new capacitance 2 should be larger than 100pF. Or the circuit must work with new waves whose periods are less than 100 times the original time, which implies 100 times higher frequencies (around 100GHz).

There's no point on considering source resistances smaller than 50Ω or load resistances larger than 1MΩ, because for respective values smaller or larger, the circuit approaches the ideal circuit and no other modifications are needed.

Two important points: capacitors 1 and 2 must have the same capacitance so they can store the same amount of charge and ensure the functioning of the circuit (section 4.1); and the larger the capacitance, usually the larger the size of the capacitor.

The table 1 resumes the impact of changing the load resistance and the capacitance on the source resistance and on the frequency of operation. The first two are chosen to be changed because they are the easiest to fix on a wanted value and then the other two are analysed.

Table 1 – Trade-Off between capacitances, resistances and frequency of operation when changing R_{load} and the capacitances

Capacitors 1 and 2 \ Load Resistance	Enlarges ($\times\alpha$)		Shrinks ($\div\alpha$)		Remains constant (-)	
Enlarges ($\times\alpha$)	R_{source} ($\div\alpha$)	Frequency (-)	R_{source} ($\div\alpha$)	Frequency (-)	R_{source} ($\div\alpha$)	Frequency (-)
Shrinks ($\div\alpha$)	R_{source} (-)	Frequency (-)	R_{source} ($\div\alpha$)	Frequency ($\times\alpha^2$)	R_{source} (-)	Frequency ($\times\alpha$)
Remains constant (-)	R_{source} (-)	Frequency (-)	R_{source} ($\div\alpha$)	Frequency ($\times\alpha$)	R_{source} (-)	Frequency (-)

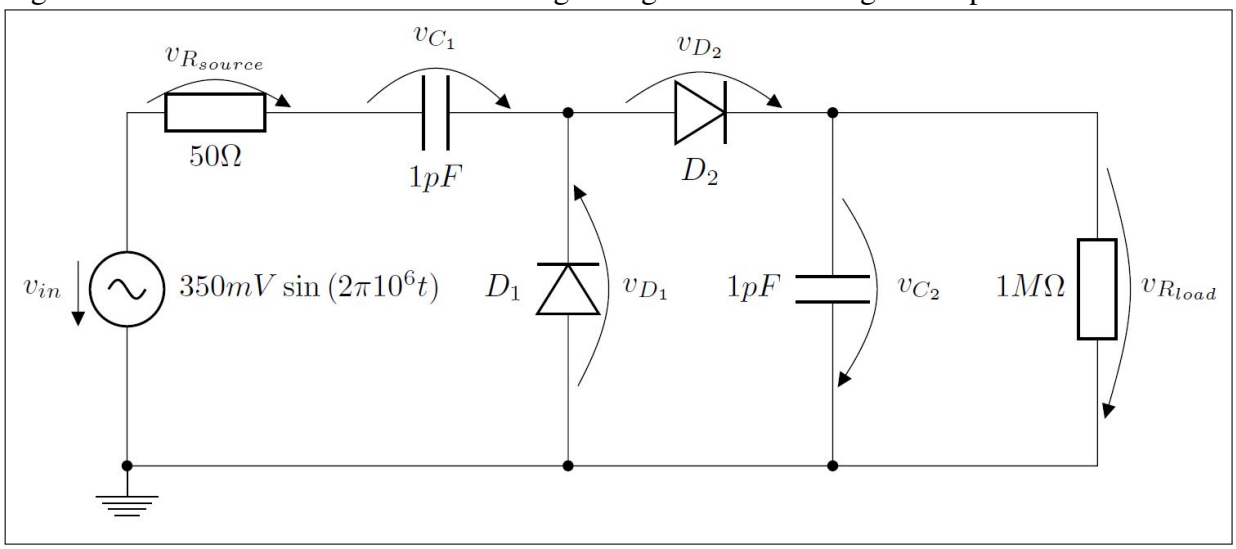
Source: the author.
Source: All of the scaling factors α are the same

To satisfy all the demands: little size of the capacitor; achievable large and small values of resistances; and frequency of operation of 900MHz (1GHz was only for simplifying the equations and simulations), the values of the elements on Fig. 23 were chosen. And the output voltages follow on Fig. 24 and the currents on 25.

Thus, the circuit operates correctly and the elements can be very small, including the capacitors. However, one issue is noticed: the voltage at the stable state is considerably smaller than the stable state's voltage of the ideal circuit on Fig. 11.

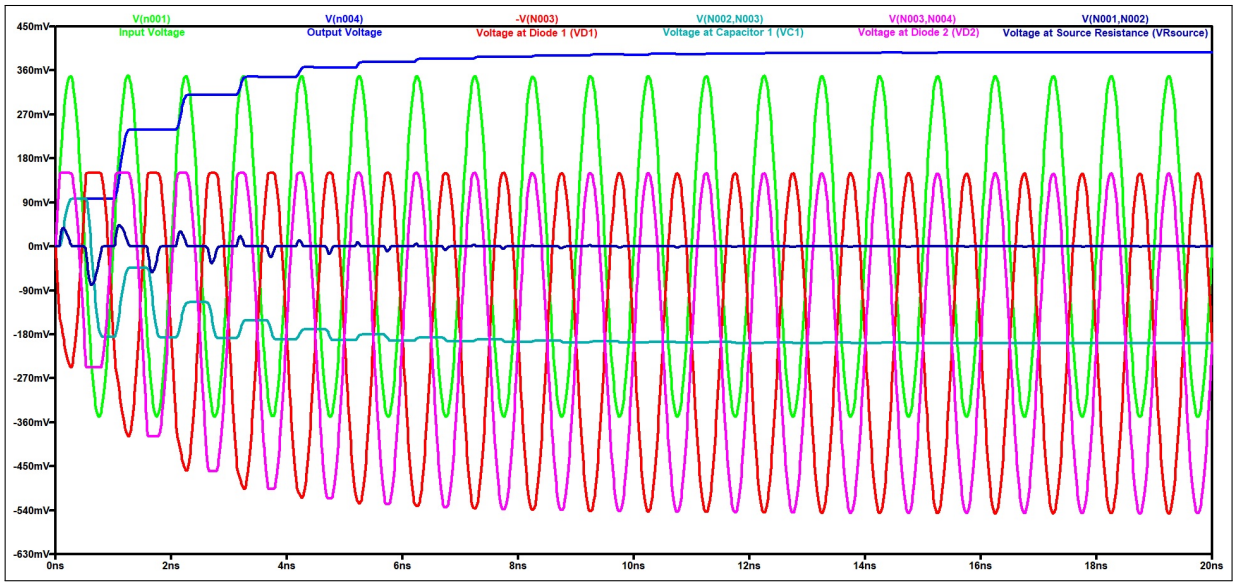
The output voltage only reaches 397mV (approximately 400mV) at 17ns, whereas the ideal circuit reaches 700mV at stable state (starting at 9,2ns), which means the circuit is no longer multiplying by 2 when non-ideal elements are placed and connected. Even when the circuit only had a load resistance, the circuit reached 700mV.

Figure 23 – Non-ideal elements on the Single Stage Dickson Voltage Multiplier



Source: the author.

Figure 24 – Voltages at the non-ideal elements on the DVM

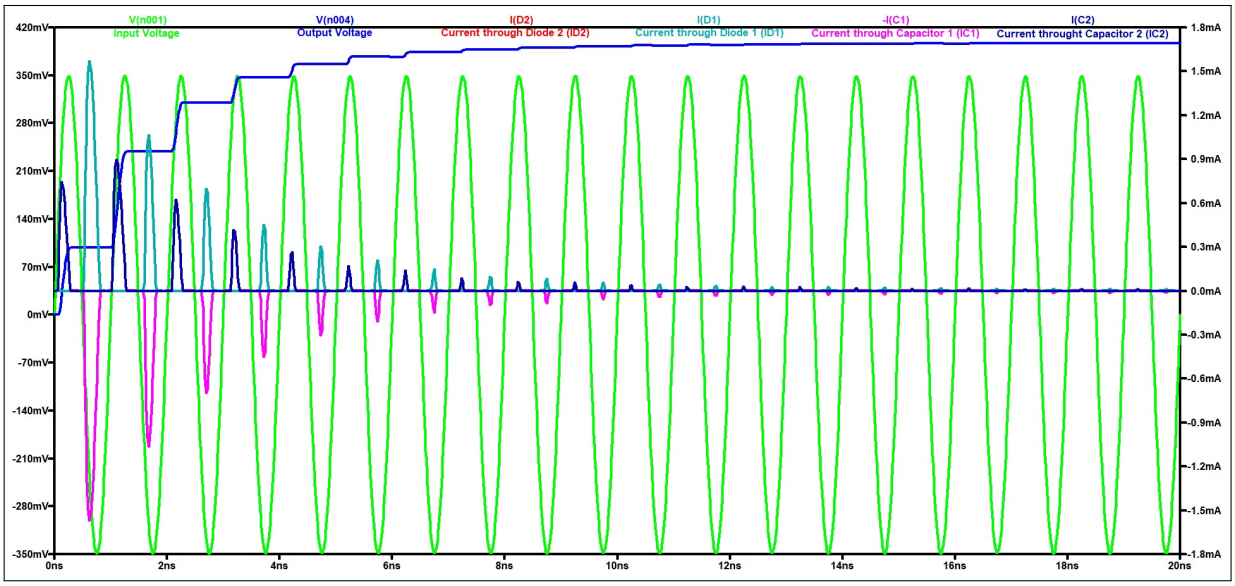


Source: the author.

Thus, this lower output voltage is due to the voltages at the diodes when conducting -the forward-bias threshold voltage of 150mV- and to the source resistance, which is responsible for: the voltage division between itself and the rest of the circuit and some power dissipation.

On the next chapters, the results and the final circuit, whose elements' values were deduced throughout the development of the theory, are used as a base to be improved or modified and analyzed in order to attain the objectives stated at chapter 3.

Figure 25 – Currents through the non-ideal elements on the DVM



Source: the author.

5 METHODOLOGY FOR DESIGNING THE CIRCUIT

The DC energy harvested from the RF is submitted to a boost converter's (Dickson Voltage Multiplier) action and raised to a voltage level above 1V, in order to power the grid of the load. After being boosted, the energy is delivered from the RF-DC converter to the application.

However, as seen on subsection 4.2.5 on Fig. 24, the output voltage is of 400mV at stable state. Thus, the circuit needs more voltage boosts. Each additional voltage boost is a stage added to the DVM.

Gradually, stages are added to the circuit. If, for each new stage, the output voltage is still unable to reach at least 1V, one more stage is added. This process continues until the output voltage surpasses 1V.

When the total number of stages needed is found and the complete circuit is built, the performance analysis based on power efficiency is performed. Then, the simulation environment changes from *LT Spice* to *Cadence Virtuoso*.

On *Virtuoso*, modifications on the DVM are made to make the results more realistic and simulations of parameters' values are done.

Firstly, the antenna is modelled as a power source working at the frequency of 900MHz - bandwidth comprised between 860MHz and 960MHz - and exposed to 0dBm power, according to the Scope Statements (chapter 3).

In the sequence, the diodes from subsection 4.2.1 are replaced by diode-connected NMOS transistors. The width of those transistors must be decided based on their impact on the Three Stages DVM.

Everything was projected, designed and simulated in (CARNEIRO; VASCONCELOS, 2015) applied to CMOS 45nm technology, using the library Generic Process Design Kits (GPDK) 45nm: a free for use library available for a 30 day trial of the software.

To verify the coherence of the circuit's design with reality: typical simulations from *Cadence Virtuoso*, *Monte Carlo* simulation for the 3-σ validation and were executed.

Next, the results are all exposed on chapter 7, were brief discussions explain the outcomes and decide whether the circuit is functional or not.

At last, after the design of the final circuit, the integrated circuit designed by Rafael is presented in the annex A. The layout was drawn according to the some basic techniques of RF design, which imposes several constraints on materials' employment, elements' positioning and also their orientation.

6 DEVELOPMENT

In this chapter, the optimal number of stages of the Dickson Voltage Multiplier and the optimal width of the NMOS transistors are sought.

The development of this project takes all of the results from the theory in chapter 4 to start from the basic Single Stage DVM whose elements' values are specified on Fig. 23.

The number of stages is raised each time the output voltage of the DVM does not reach 1V with the current number of stages. Thus, one more is added. When the 1V requirement is met, the circuit ceases to be incremented.

After this procedure, already on *Cadence Virtuoso*, the Multi Stage DVM now is designed with NMOS transistors connected in such a way they reproduce the same effect of the diodes. Nevertheless, using transistors require the analysis of one more parameter: the width W of the transistor's channel.

This parameter is firstly set as an unknown and the circuit's performance is simulated for various values of W. When a value is found, the execution of the *Monte Carlo* simulation validates the circuit.

6.1 Multi Stages Dickson Voltage Multiplier

As seen on Fig. 24, the output voltage reaches 400mV DC. This is incompatible to the first assumption, where 700mV DC were expected. Before, it would be expected that just another added stage would be enough to meet the 1V requirement.

Unfortunately, the only way to know how many stages are needed, is to simulate the circuit adding, at each step, another stage and verifying its output voltage.

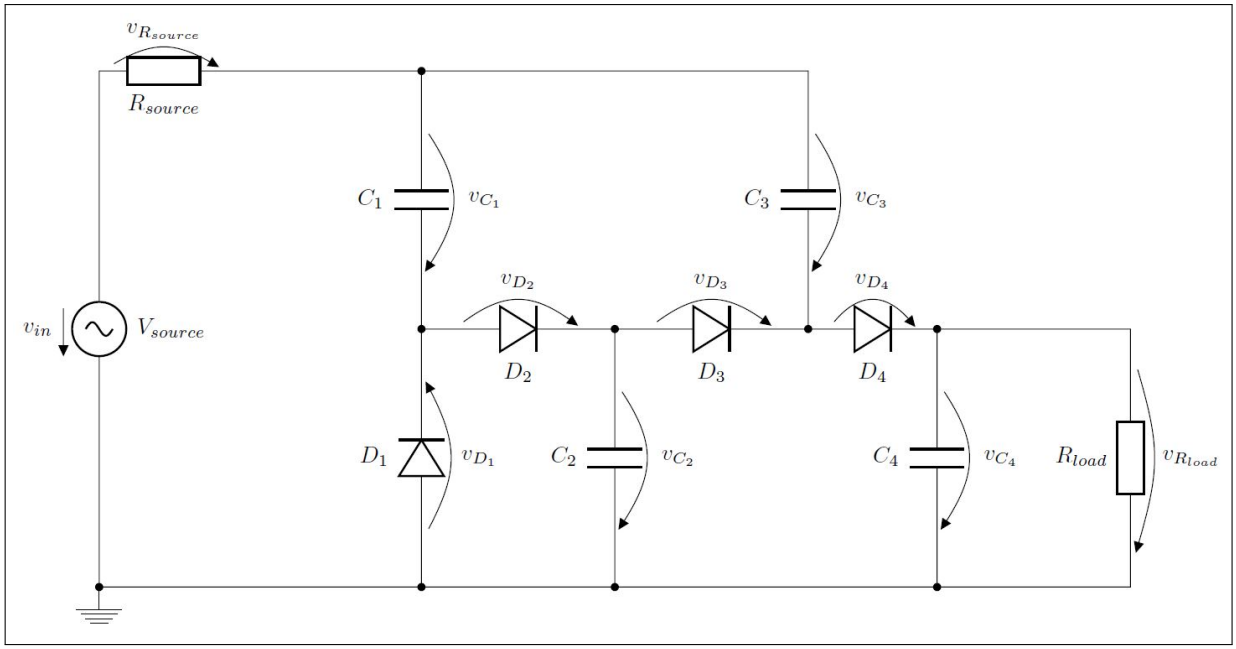
To add more stages, cascading is not the answer: an unusual "cascade"is necessary, where the output of the first stage is connected to the first diode (here NMOS transistor) of the second stage; both the first capacitors coming from each the first and the second stages are connected to the RF voltage source, or the antenna.

Basically, all of the first capacitors of each stage is charged directly by the RF source and the first diodes of the subsequent stages (after the first stage) are connected to the output of the previous stage.

For example, for the Two Stages DVM on Fig. 26, the first capacitors of the first and second stage, C_1 and C_3 respectively, are powered by the RF source directly. And the first diode

of the second stage (D_3) is connected to the output of the first stage (the node above C_2).

Figure 26 – Two Stages Dickson Voltage Multiplier



Source: the author.

Where,

- Voltage source: $v_{in} = 350mV \sin(2\pi 10^6 t)$;
- Non-ideal diodes described by (4.32);
- $R_{source} = 50\Omega$;
- $R_{load} = 1M\Omega$;
- Capacitors of 1pF.

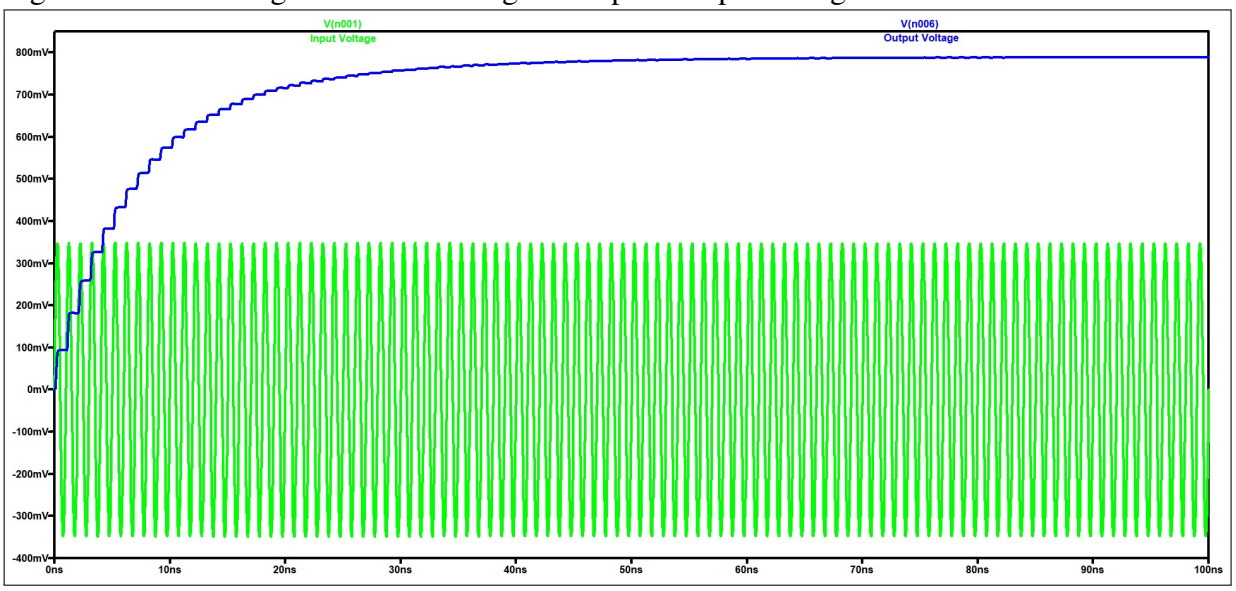
Fig. 27 demonstrates that the output voltage has increased, but the stable state takes longer to be reached. At, approximately, 60.3ns the circuit attain 785.5mV. Later, at 80.3ns, the final value is reached by the circuit on 788.3mV.

The output voltage has not even surpassed 800mV, so a third stage is necessary to boost the output voltage. The third stage's connections are easy to made following the same procedure of designing the Two Stages DVM.

The first diode of the third stage D_5 is connected to the node above the output capacitor of the second stage C_4 and the first capacitor of the third stage C_5 is also connected to the voltage source. Fig. 28 demonstrates the connections and the elements on its schematic.

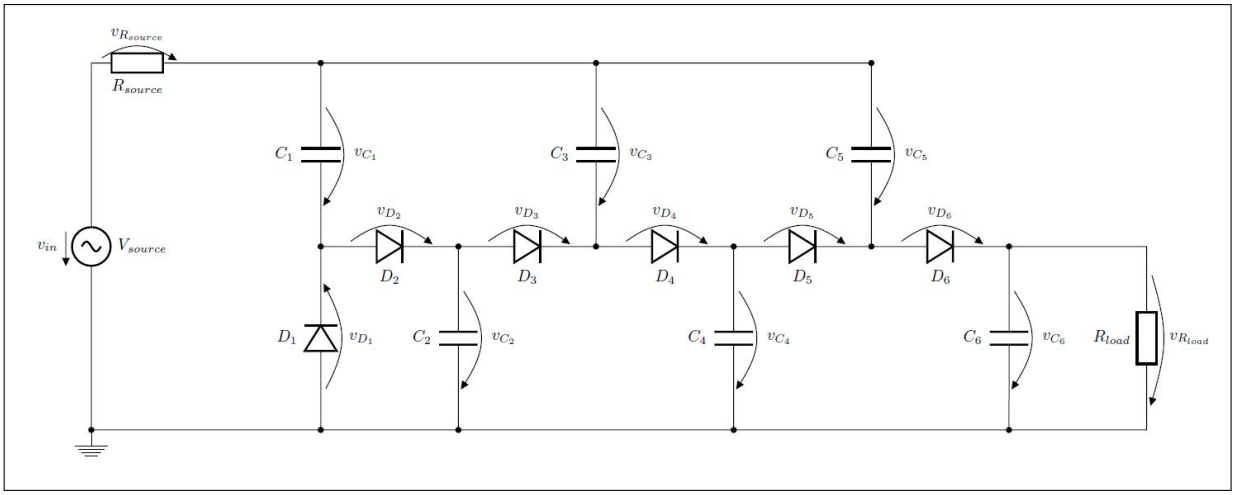
The Fig. 29 results from the simulation of the Three Stages DVM using the following parameters:

Figure 27 – Two Stages Dickson Voltage Multiplier output voltage



Source: the author.

Figure 28 – Three Stages Dickson Voltage Multiplier



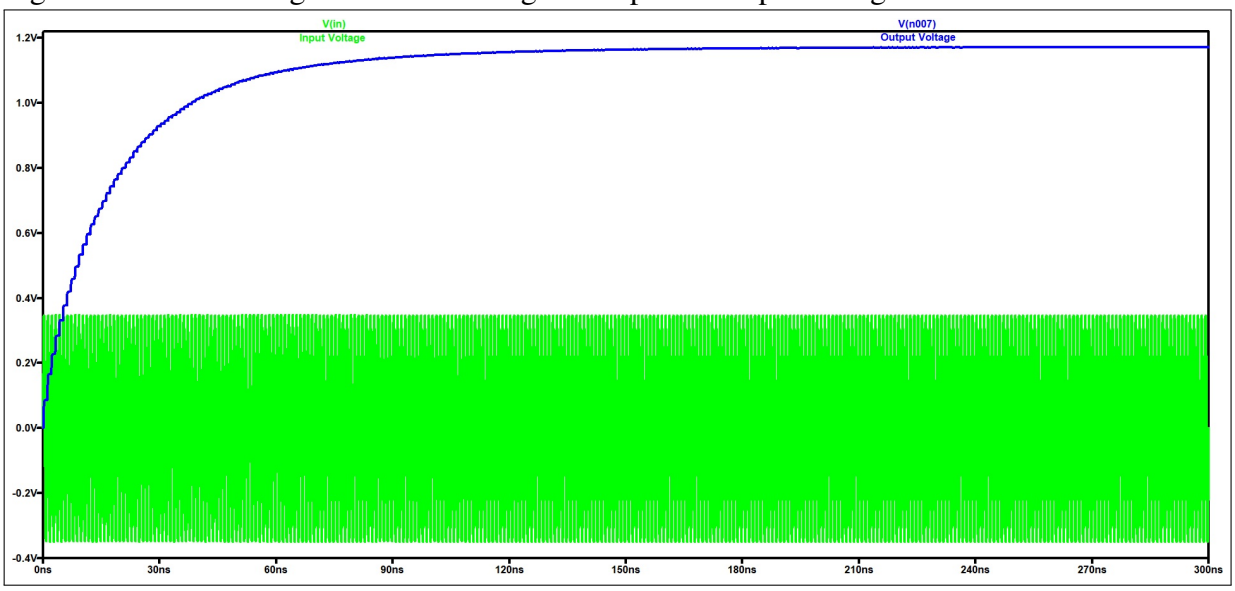
Source: the author.

- Voltage source: $v_{in} = 350mV \sin(2\pi 10^6 t)$;
- Non-ideal diodes described by (4.32);
- $R_{source} = 50\Omega$;
- $R_{load} = 1M\Omega$;
- Capacitors of 1pF.

With three stages, the circuit has managed to attain an output voltage of 1.17V at 199.6ns and 1.172V at 259.3ns, the stable state. The three stages fulfill the requirement of the output voltage over 1V and can be chosen for the project. But before that, four stages should be tested.

The simulation results for the four stages follow on Fig. 30, using the same para-

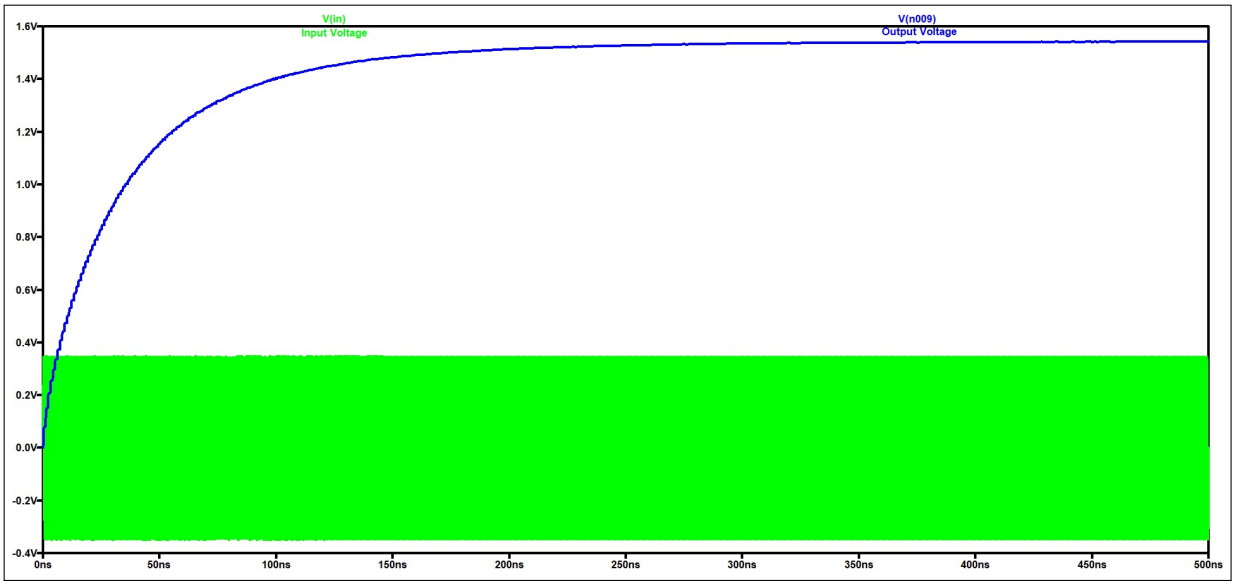
Figure 29 – Three Stages Dickson Voltage Multiplier's output voltages



Source: the author.

meters for the two and three stages' simulations. It reaches an output voltage level of 1.5V at 172.7ns, approximately, and the stable state at 442.4ns with 1.542V at the output.

Figure 30 – Four Stages Dickson Voltage Multiplier's output voltages



Source: the author.

As it can be seen, from three stages to four stages, the additional stage added an increase of 370mV at the final value. The four stages circuit could be implemented to ensure that the output voltage will be higher than 1V. However, it shouldn't be done due to one main reason, the size of the integrated circuit.

Each new stage of the DVM adds two capacitors to the circuit. As it will be seen in the annex A, the capacitors are larger than all of the other elements of the circuit. Thus, to

implement a fourth stage and gain 370mV, when at three stages the output voltage has already attained more than 1V, is not worth it.

Therefore, the Three Stages DVM's architecture is used.

6.2 Implementing the NMOS transistors

At this moment, the NMOS transistors finally substitute the non-ideal diodes. When this is done, the last parameter to be specified is the width of the transistor. To make this specification, the width's value must be swept inside a range to check what is the optimal value which will optimize the output voltage's level.

LT Spice has proven to be a very good tool for simulating architectures, unfortunately, it was not possible to go further with it, because it was not found how to model an NMOS transistor's size parameters. For this matter (finding the optimal transistor size), *Virtuoso* was employed.

The value of W is still not determined, but the value of the channel length is well determined by the technology adopted, 45nm.

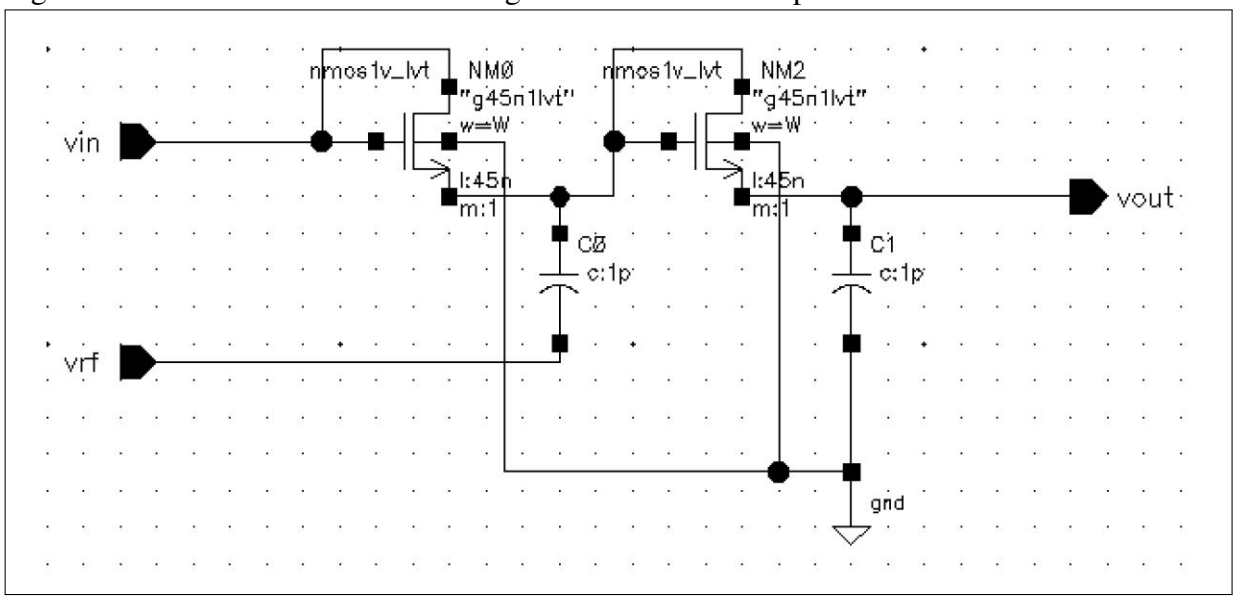
In the first place, a basic cell of the project's circuitry was created, this cell corresponds to an isolated stage of the DVM. Comparing the schematics in the sequence with that from Fig. 28:

- v_{in} is the equivalent of the input of the first diode of each stage, like D_1, D_3 and D_5;
- v_{rf} is the equivalent of the source voltage which is connected to the first capacitors of each stage;
- v_{out} is the equivalent of the node above the output capacitor of each capacitor;
- As explained in subsection 4.2.2, the gates are connected to the drain of the transistors and, thus, both transistors behave like diodes.

It is important to remark that the source is now a 0dBm sinusoidal source whose frequency of operation is of 900MHz, it has inner resistance and there is a load resistance of 1MΩ at the output of the voltage. Now the simulations are executed with W as a variable.

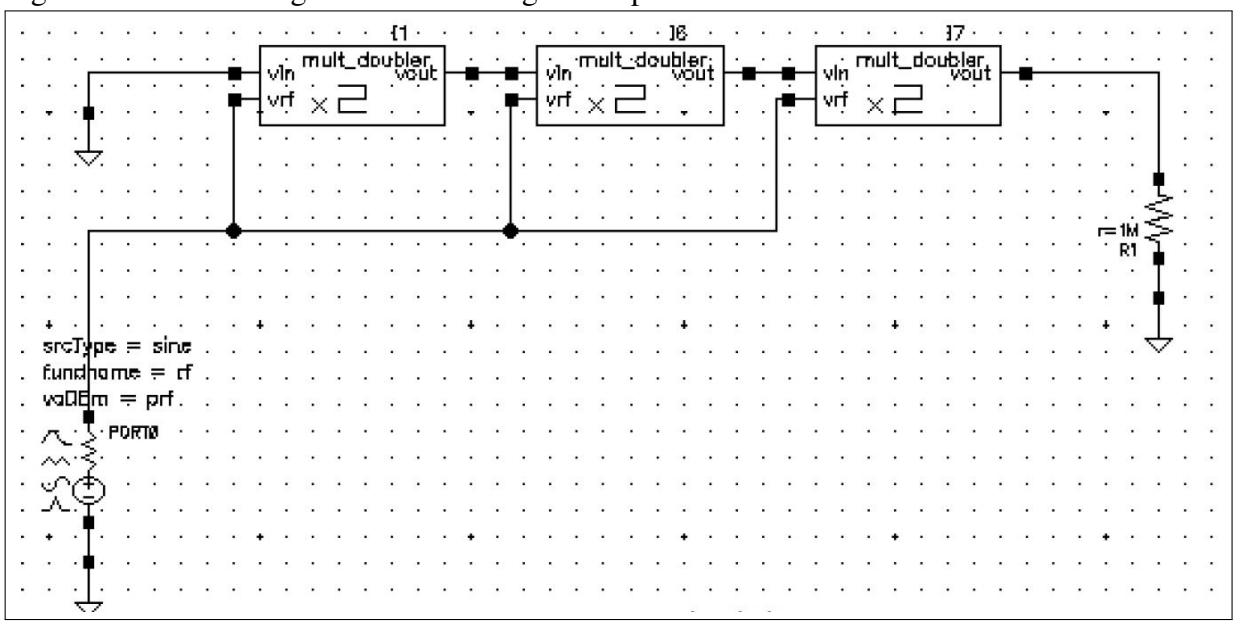
After all pertinent simulations, the optimal transistor's width is found (12μm), always taking into account the layout's viability and conserving the estimated occupied surface of the integrated circuit minimum. Finally, the circuit is completely modelled and can be transformed into an integrated circuit. This procedure is done in the annex A.

Figure 31 – Basic cell of the Three Stages DVM circuit *W* dependent



Source: (CARNEIRO; VASCONCELOS, 2015).

Figure 32 – Three Stages Dickson Voltage Multiplier



Source: (CARNEIRO; VASCONCELOS, 2015).

In the next chapter (8), the results from all the simulations are printed and analyzed. Some of them have already been used during the development, such as the simulations to discover the optimal transistor's width *W*.

6.3 Power Efficiency Analysis

Power efficiency is an important topic. The Three Stages DVM may work as expected and produce a voltage at the output higher than 1V, but the efficiency must be analyzed. On the

Fig. 28, R_{load} represents a load, which will draw and consume power from the source.

Power efficiency can, thus, be simply computed dividing the power consumed by R_{load} by the available power in the ambient captured by the antenna at the circuit's input, 0dBm or 1mW, as stated in the Scope Statements (chapter 3) and mentioned on the Methodology (chapter 5).

$$\eta = \frac{P_{load}}{1mW} \tag{6.1}$$

To calculate the power dissipated at the load resistance, calculations can be made by hand based on the voltage values from Fig. 29 and the instantaneous power is obtained, as in (6.2).

$$P_{load}(t) = \frac{v_{load}^2(t)}{R_{load}} \tag{6.2}$$

There is also a reliable option which can automatically compute not only the instantaneous power dissipated at the load resistance but also the instantaneous power delivered by the source, which is using *LT Spice* for measuring the instantaneous power absorbed or emitted by each element of the circuit.

The voltage source used throughout the Theory (chapter 4) and the Development (chapter 6) always gives outputs a sinusoidal voltage of 350mV amplitude and 10MHz frequency, independently of the circuit connected. Nevertheless, if the circuit needs a certain amount of power, this same amount can be drawn from the source.

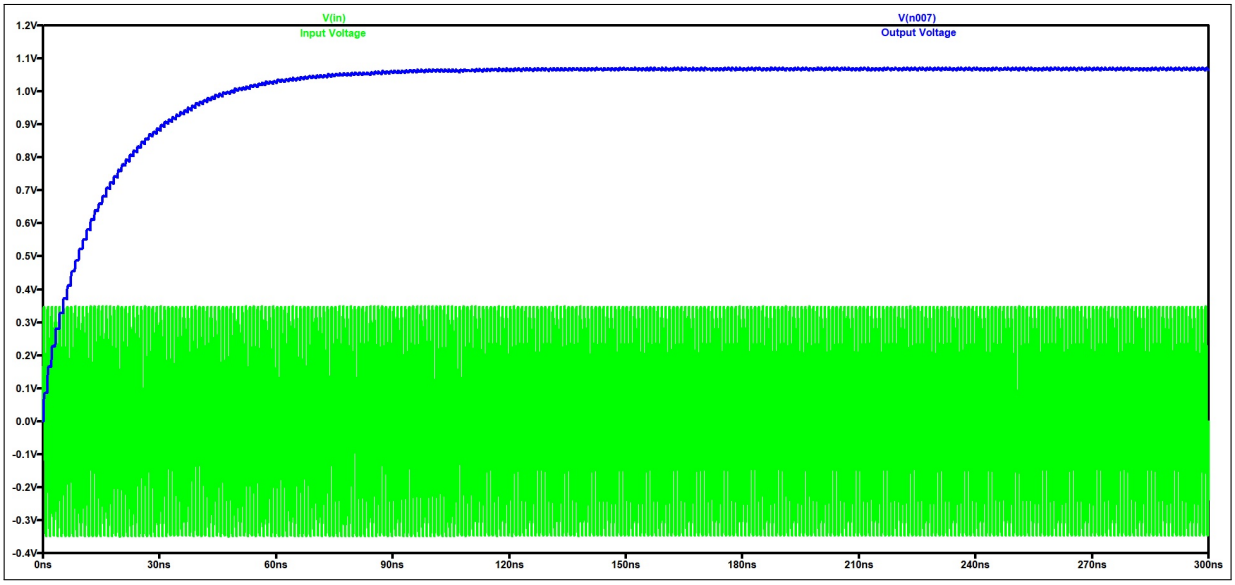
Unfortunately, as it can be found in section 7.2, the efficiency is very poor for the Three Stages DVM modeled at section 6.1. This can be changed, however.

Equation (6.2) shows that if R_{load} shrinks, the power will rise. But that would mean changing the circuit designed for this project up to now.

As it was seen in table 1, if every parameter of the circuit remains unchanged, including the values of the elements, reducing the load resistance below 1MΩ has impacts over the output voltage (subsection 4.2.4).

But if the load resistance shrinks in a factor of 10, resulting in 100kΩ, there are no major impacts on the output voltage, as Fig. 33 depicts. The output voltage reaches 1.07V at stable state, and has more fluctuations -than the output of the 1MΩ circuit- which is less similar to a DC voltage.

Figure 33 – Three Stages Dickson Voltage Multiplier Output Voltage and Power for $R_{load} = 100k\Omega$



Source: the author.

The results of those measurements are also found in chapter 7, section 7.2.

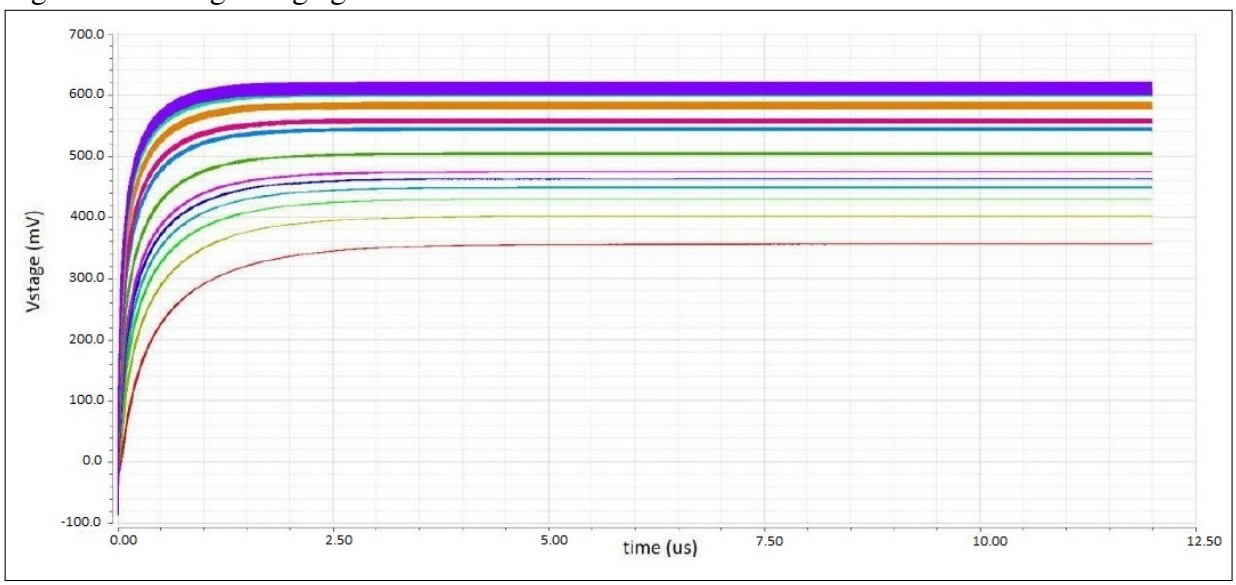
7 RESULTS

7.1 Desired Values

At this moment, the project has a dimensioned and functional circuit which has produced results here displayed. By parametric simulations, the optimal value of the MOS technology's width was found aiming for an output voltage level larger than 1V.

For the single stage gain, making the width W vary from 1μm (bottom brown line) to 58μm (top violet line) the graphic on figure 34 was plotted. The higher the line, the bigger the value of the corresponding W.

Figure 34 – Single stage gain in function of time for 58 different values of W



Source: (CARNEIRO; VASCONCELOS, 2015).

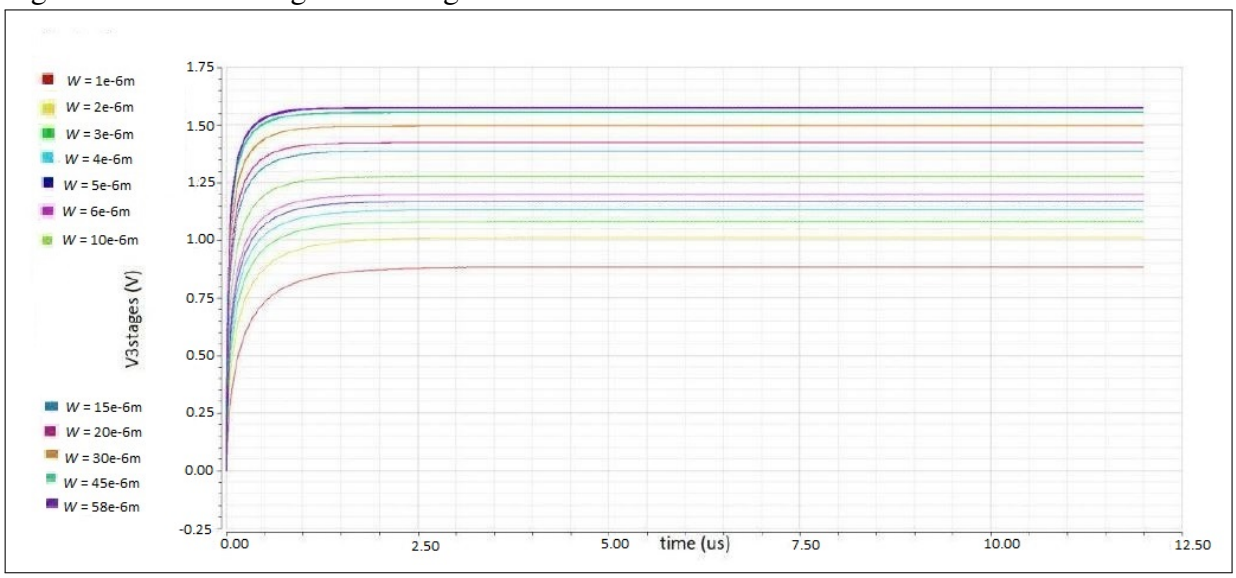
Based on this result, a simulation for three stages (figure 35) was also performed. But for this graphic, only a few values of W out of the 58 on figure 34 are selected and printed, as the graphic indicates in its legends.

In order to better visualize and interpret the results, an additional graphic (Fig. 36) was plotted and its output voltage at stable state is put in function of all of the 58 values calculated of W.

7.2 Power Efficiency

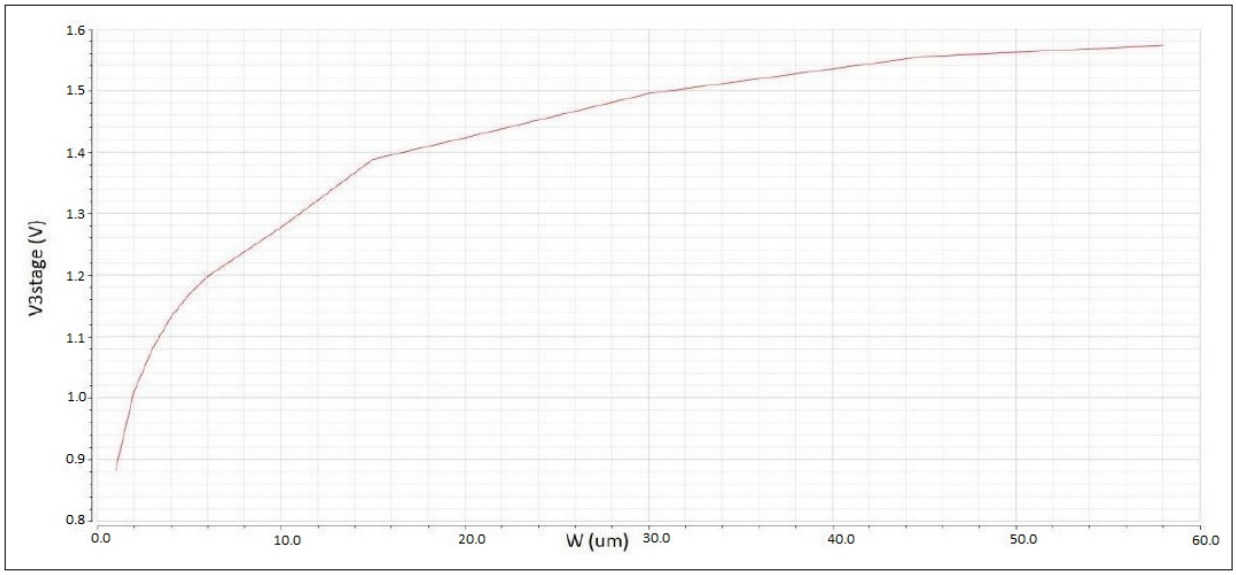
Fig. 37 displays the plot of the power dissipated at the load resistance (output power), the power delivered by the voltage source (input power) and the input and output voltages. On

Figure 35 – Three Stages DVM's gain in function of time for different values of *W*



Source: (CARNEIRO; VASCONCELOS, 2015).

Figure 36 – Three stages gain in function *W*



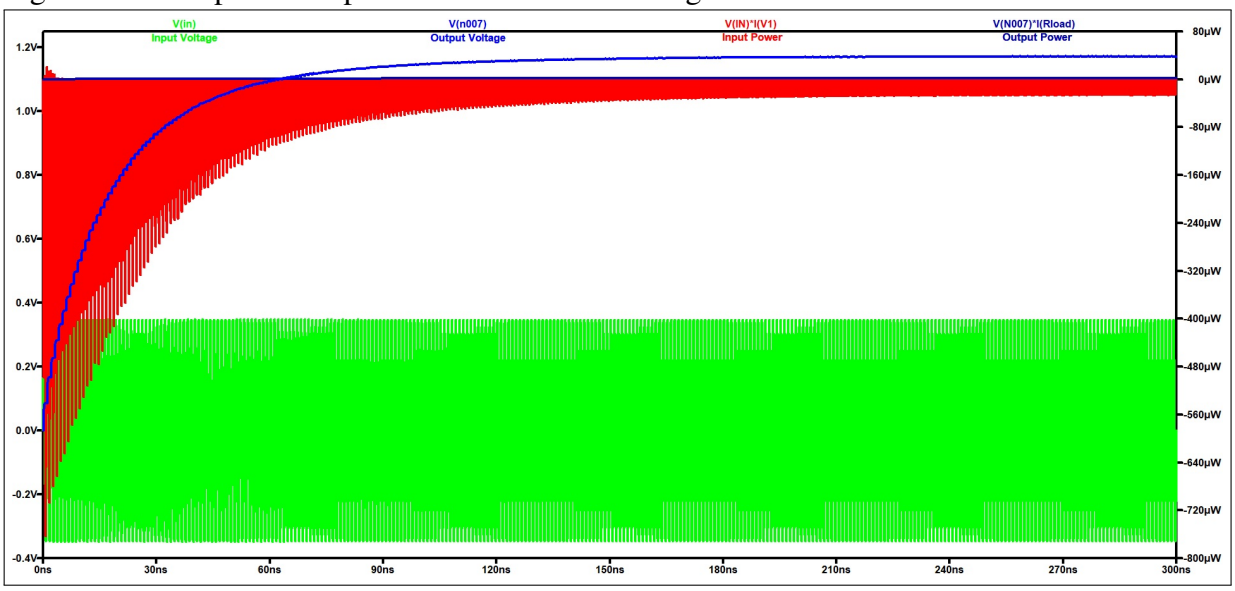
Source: (CARNEIRO; VASCONCELOS, 2015).

this figure, the input power has big variations: at first, the source delivers many times more power than at the end.

The fluctuations on the input power plot stabilize around 200ns, which coincides with the time when the output voltage of the Three Stages DVM also starts to stabilize, according to section 6.1. The overall behavior also coincides with the behavior of the output voltage as seen on the same figure.

This means that while the output voltage is rising, the circuit draws more power from the voltage source. As the output voltage stabilizes and rises less than at the beginning, the power drawn from the source becomes smaller.

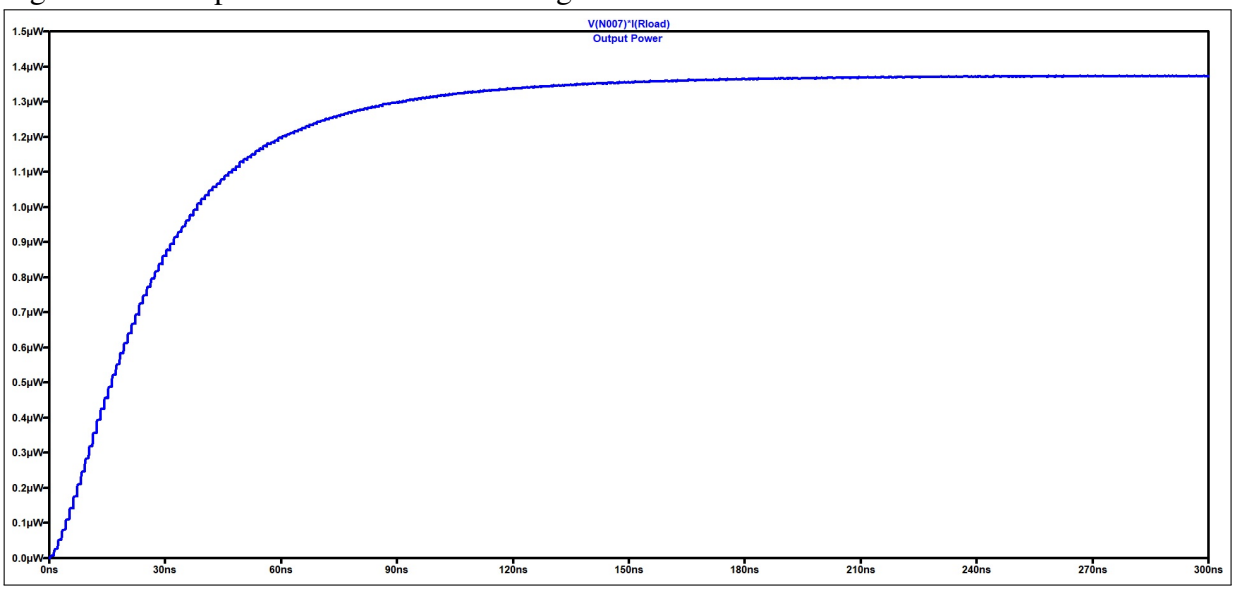
Figure 37 – Output and Input Power of the Three Stages DVM



Source: the author.

The output power -the purple line almost negligible on Fig. 37- is better depicted on Fig. 38. The output power starts at 0W and grows gradually. At 40ns it reaches 1μW and then, at 91ns it reaches 1.3μW. Finally, it reaches the stable value of 1.37μW around 200ns. This behavior is expected, since the instantaneous power grows accordingly to the voltage, as (6.2) confirms.

Figure 38 – Output Power of the Three Stages DVM



Source: the author.

Finally, by (7.1) and considering the instantaneous power starting from 200ns as the average power, because on the stable state its fluctuations are negligible, the power efficiency of

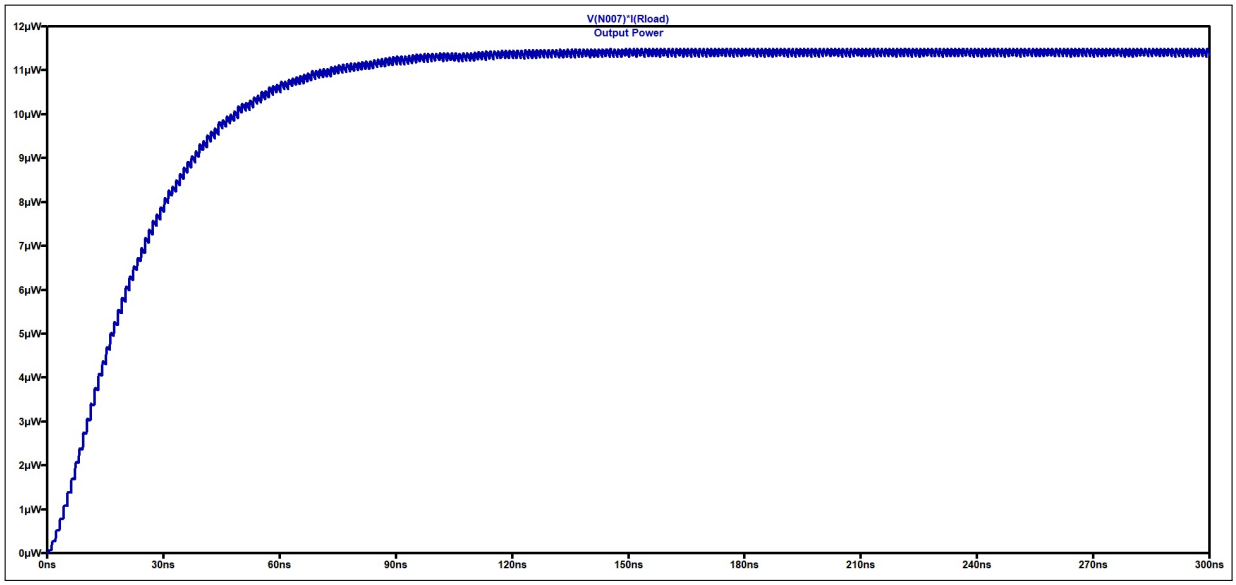
the circuit is as low as:

$$\eta = \frac{P_{load}}{1mW} = \frac{1.37\mu W}{1mW} = 0.137\% \tag{7.1}$$

0.137% is a poor efficiency for a circuit. This leads to trying to improve the efficiency reducing the value of the load resistance to 100kΩ as discussed at the end of section 6.3.

Despite the poorer performance of the 100kΩ at the load, it still works inside a tolerance range (fluctuations of less than 0.8% peak-to-peak) and could be an option to obtain more output power (depending on the application), as Fig. 39 shows. It attains an average value of 11.4μW at the stable state, which implies an efficiency of 1.14%.

Figure 39 – Output Power of the Three Stages DVM for $R_{load} = 100k\Omega$



Source: the author.

The efficiency has increased at the cost of the performance of the circuit whose output voltage quality becomes poorer due to the fluctuations.

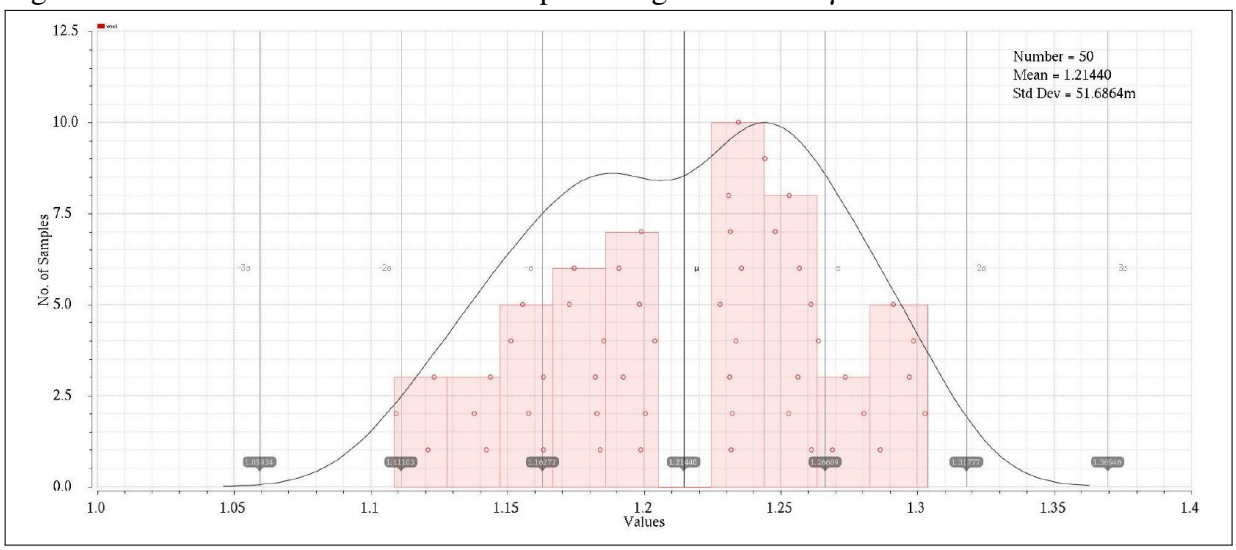
7.3 Monte Carlo simulation and 3-σ validation

For the 3-σ validation, the Monte Carlo statistical simulations were ran with 50 points chosen arbitrarily over three strategically chosen values of W, from the layout's point of view: 6μm, 10μm and 12μm, which had 1.2V, 1.28V and 1.32V respectively.

The histogram corresponding to W of 12μm was the only one to succeed on the 3-σ criteria. The other two presented on the validation test minimum output voltages of 908,2mV for the 6μm and 987,2mV for the 10μm.

On the following histogram (Fig. 40), the average of the output voltage is of 1.22V, its standard-deviation of 51,69mV and the minimum output voltage on the 3-σ was 1,06V.

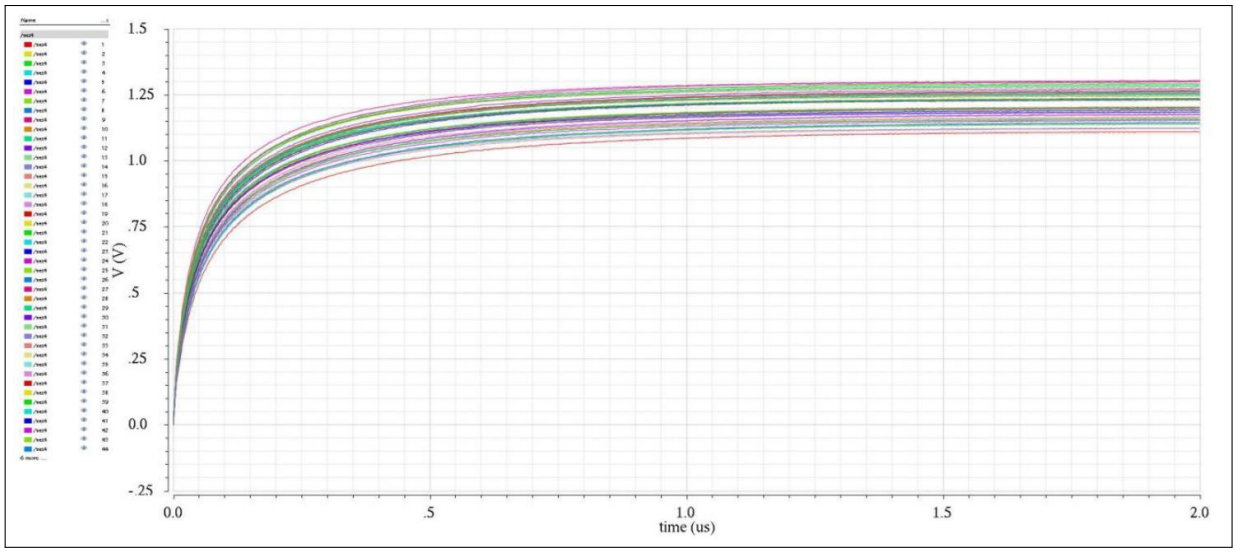
Figure 40 – Values' distribution of the output voltage for $W = 12\mu$m



Source: (CARNEIRO; VASCONCELOS, 2015).

In order to better visualize this distribution, a graphic with every voltage curves as a function of time is also plotted on figure 41. This graphic demonstrates the possible outcomes calculated by the Monte Carlo simulations. As it can be seen, indeed none of the simulations has previewed an output voltage smaller than 1V at stable state.

Figure 41 – Values' distribution of the output voltage for $W = 12\mu$m in function of time



Source: (CARNEIRO; VASCONCELOS, 2015).

8 CONCLUSION

The results from the simulations performed led to the conclusion that the circuit indeed fulfills the objective of providing a DC output voltage larger than 1V from a RF source, which is the environment. For such a purpose, the circuit is useful.

However, as seen on section 7.2, being the power efficiency as low as of 0.137%, the circuit becomes questionable whether it is or not worth the production and all of the subsequent costs related to installing it to the systems it will supply power.

If the fact that the low efficiency is not important, the circuit is still capable of providing 1.37μW, a value that could build up with other energy harvesting schemes to supply enough energy to power important devices for IoT, Multiple-Input Multiple-Output (MIMO) Communications scenarios, industry 4.0.

This output power is capable of feeding energy to low power sensors in a sensor array or network used to capture signals which will be processed and used by other electronic systems.

The output power of the DVM can also be increased if the load is reduced enough to make the efficiency grow as much as 10 times (end of section 7.2) but not too much as to induce the circuit into failure due to low load resistances.

Overall, from the electronic architecture point of view, there's not much to improve on the RF-DC converters' situation, unless more advanced concepts are applied. The Dickson Voltage Multiplier seems to have better efficiency for small load resistances, which can only be used when either the frequency is very low and/or the capacitors can be very large in capacitance and in size.

Another approach is to invest in materials science and search for components of better quality for this application. As a matter of fact, when dealing with RF, the materials have crucial importance, because no ordinary component can work properly in a domain constantly dealing with high frequencies. Discrete elements and conductors are replaced by other kinds of elements such as wave-guides, strip-lines, resonators and many others.

Future smaller technologies may be also a problem, since reducing the size of a technology implies also reducing the insulator and the overall dimension of the capacitor. A smaller insulator may result in insufficient capacity to stand voltages as high as 1V.

Despite the low efficiency of this project's circuit, I believe energy harvesting is a valuable concept and it more efforts should be made towards this objective.

BIBLIOGRAPHY

AHN, Y.; SONG, S.; YUN, K.-S. Power generating tactile sensor array in woven fabric form. In: IEEE. **Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS), 2015 Transducers-2015 18th International Conference on**. [S.l.], 2015. p. 161–163.

ASL, M. B.; ZARIFI, M. H. Rf to dc micro-converter in standard cmos process for on-chip power harvesting applications. **AEU-International Journal of Electronics and Communications**, Elsevier, v. 68, n. 12, p. 1180–1184, 2014.

CARNEIRO, R. K.; VASCONCELOS, T. A. d. **Conception d'un Circuit de Récupération d'Énergie Électromagnétic sous CMOS 45nm**. Dissertação (First Year Undergraduate Synthesis Project) — Department of Electronic Systems, Centrale-Supélec, Paris, 2015.

GORLATOVA, M.; WALLWATER, A.; ZUSSMAN, G. Networking low-power energy harvesting devices: Measurements and algorithms. **IEEE Transactions on Mobile Computing**, IEEE, v. 12, n. 9, p. 1853–1865, 2013.

HASTINGS, A. **The Art of Analog Layout**. [S.l.]: Prentice Hall, 2001.

ISRAEL, B. **Thin film converts heat from electronics into energy**. 2018. Disponível em: <http://news.berkeley.edu/2018/04/16/thin-film-converts-heat-from-electronics-into-energy/>. Acesso em: June 18th, 2018.

JOHNSON, H. W.; GRAHAM, M. *et al.* **High-speed digital design: a handbook of black magic**. [S.l.]: Prentice Hall Upper Saddle River, NJ, 1993. v. 1.

OTTMAN, G. K.; HOFMANN, H. F.; BHATT, A. C.; LESIEUTRE, G. A. Adaptive piezoelectric energy harvesting circuit for wireless remote power supply. **IEEE Transactions on power electronics**, IEEE, v. 17, n. 5, p. 669–676, 2002.

SEIGNEURET, G. **Analyse et Optimisation de télé-alimentation pour systèmes RFID UHF**. Tese (Doctor of University of Aix Marseille 1) — Aix Marseille 1, 2011.

SHINDE, M. R.; SALUNKE, P. M.; CHASKAR, V. A.; PRAJAPATI, U. B.; WAGH, P. M.; YADAV, V. Multisource energy harvesting for low power applications. In: IEEE. **India Educators' Conference (TIIEC), 2014 Texas Instruments**. [S.l.], 2014. p. 118–123.

SUN, H.; GUO, Y.-x.; HE, M.; ZHONG, Z. Design of a high-efficiency 2.45-ghz rectenna for low-input-power energy harvesting. **IEEE Antennas and Wireless Propagation Letters**, IEEE, v. 11, p. 929–932, 2012.

ANNEX A – LAYOUT OF THE THREE STAGES DICKSON VOLTAGE MULTIPLIER IN AN INTEGRATED CIRCUIT

This layout was designed by Rafael K. Carneiro at Centrale-Supélec in 2015, when both Rafael and Thiago were in an early joint project (CARNEIRO; VASCONCELOS, 2015), advised by Professor Pietro Maris Ferreira from the Department of Electronic Systems at Centrale-Supélec.

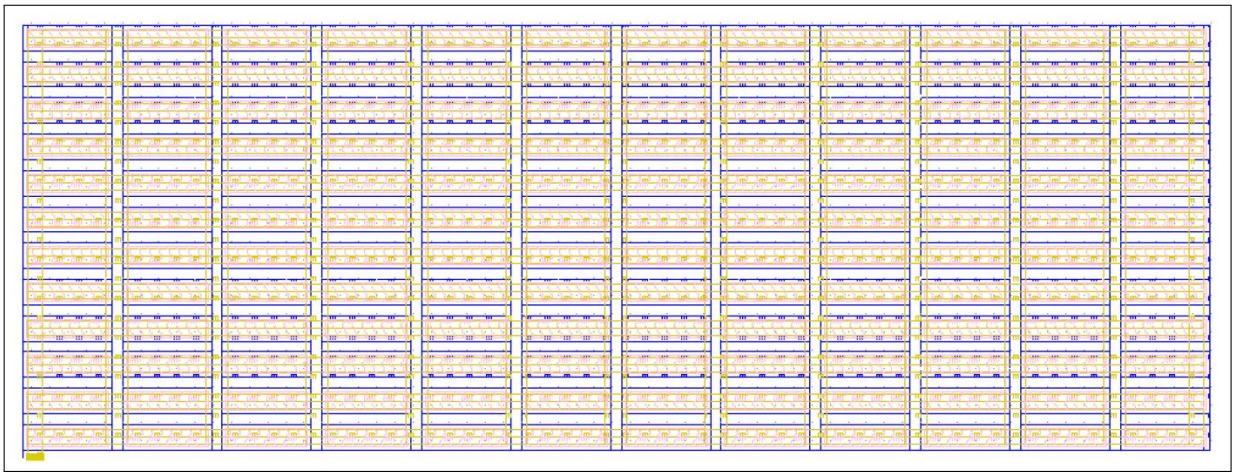
This project resumed in a report presented to professors from Supélec. Here, the main points of the project were reproduced, the details of the integrated circuit layout in the report.

The layout of the circuit is one of great importance because it aims to design an integrated circuit which can reliably harvest energy from electromagnetic waves surrounding the device. Thus, some layout techniques are needed as well as some knowledge on electromagnetic effects on high-speed electronic elements.

The layout techniques were taken from (HASTINGS, 2001) and also taught by Professor Pietro.

To begin with, a 1pF capacitor of type *Metal-Insulator-Metal* was designed divided in 144 parts of identical capacitances and symmetrically designed in the fashion of Fig. 42. The result follows:

Figure 42 – Capacitor's layout



Source: (CARNEIRO; VASCONCELOS, 2015).

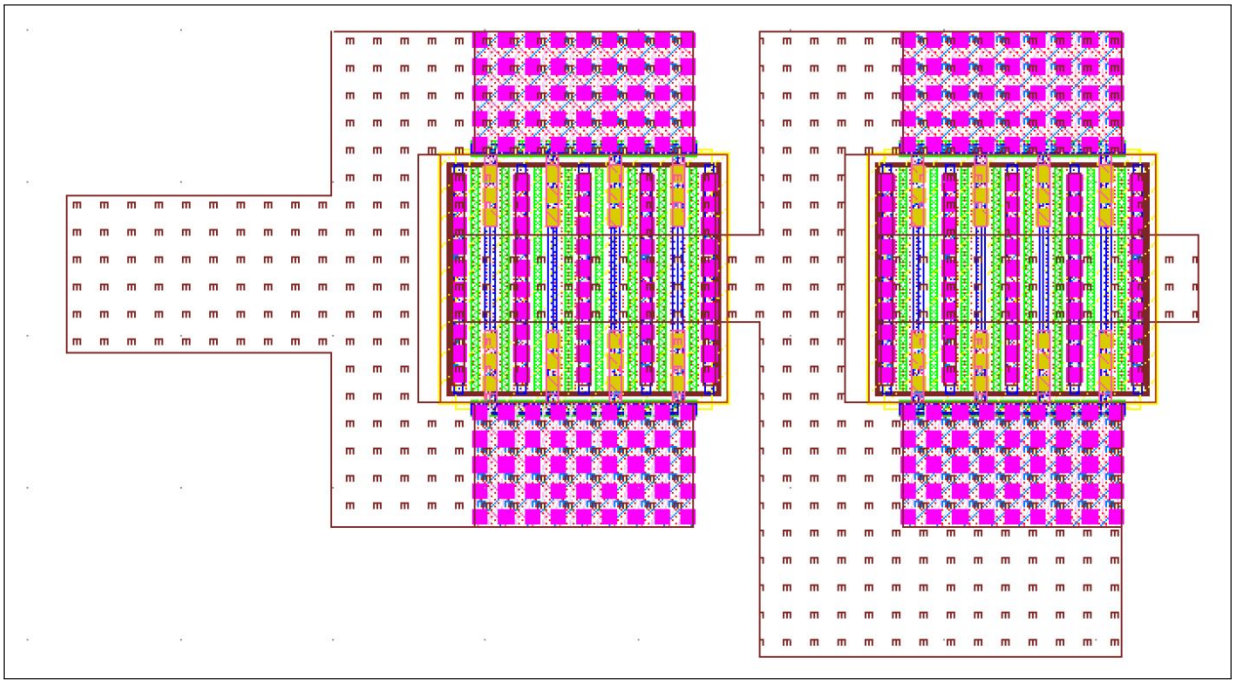
This division was made due to the lack of appropriate capacitances in the *free version* software. To better visualize the physical construction of the capacitors and the electrical connections made, amplified picture is taken an put on Fig. 43.

Figure 43 – Amplified view on the capacitors' layout

Source: (CARNEIRO; VASCONCELOS, 2015).

After that, the NMOS transistors' layout were designed aiming to keep the *Fill Factor* (the relation between the horizontal and vertical dimensions of the MOS) close to one, resembling a square. Also, the highest level of metal was used to avoid parasite capacitances and to assure the good functioning of the transistors.

Figure 44 – Layout of the NMOS transistors

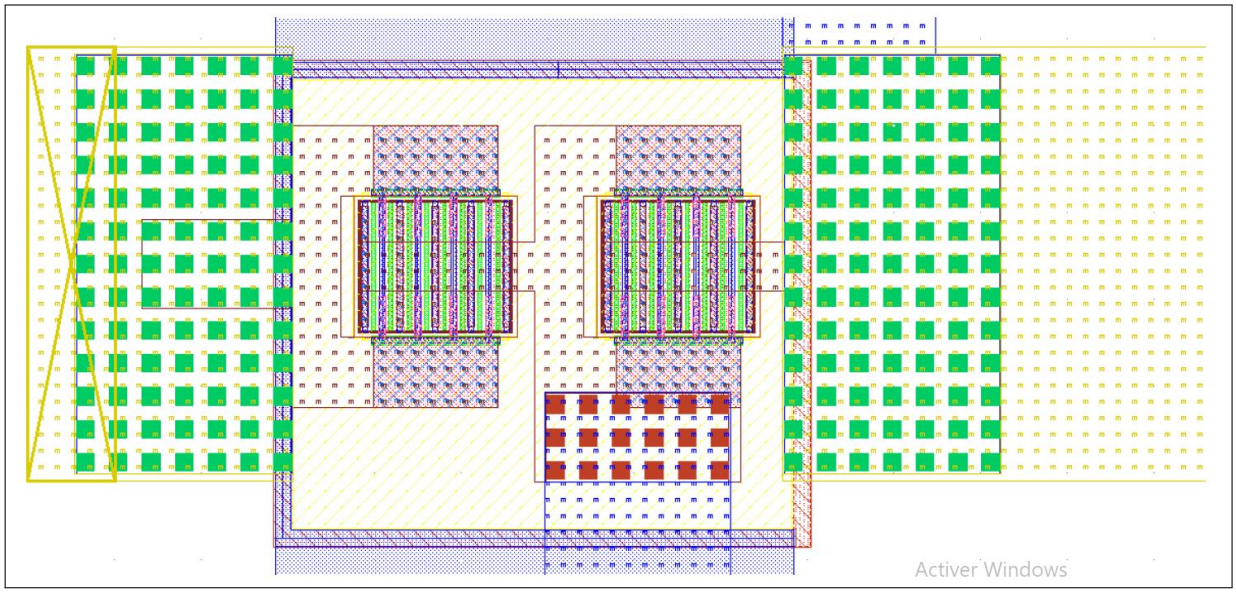


Source: (CARNEIRO; VASCONCELOS, 2015).

One important remark when working on RF design or, in general, High Speed Design

- as it is sometimes referred and by (JOHNSON *et al.*, 1993) for example - is to not close a loop in the created *guard rings*, since it can produce undesirable *Foucault currents* which consume power and can have possibly catastrophic thermal effects inside the circuit. Due to it, the *guard ring* was drawn in a *U* shape:

Figure 45 – The metal 1 (in blue) is in *U* shape in the *guard ring*



Source: (CARNEIRO; VASCONCELOS, 2015).

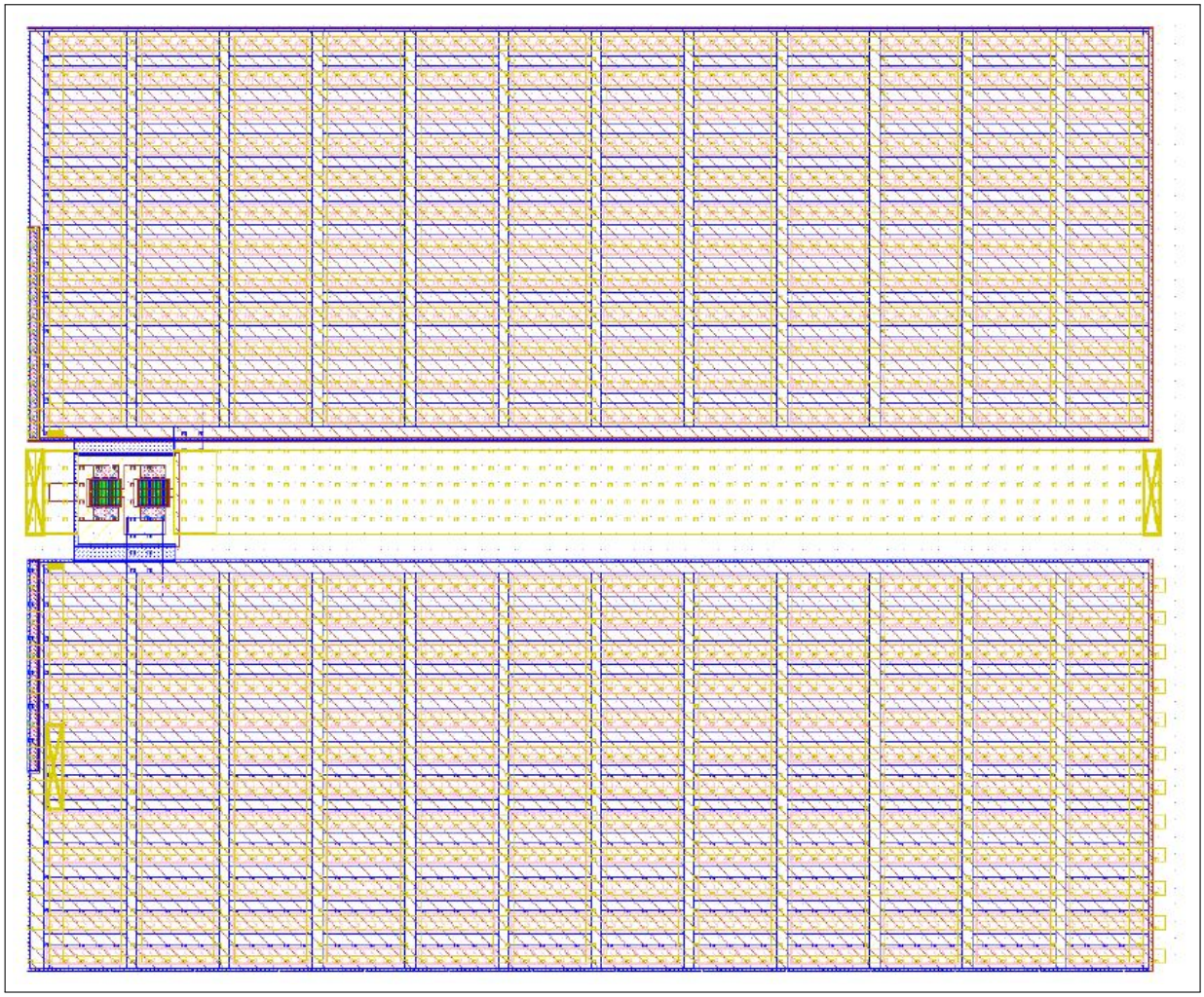
On the sequence, one independent stage of the Dickson Voltage Multiplier was designed, using a technique of increasing the width of one path if the length is large enough with respect to *W* -in order to shrink the electrical resistance- as seen on Fig. 46, in yellow.

Finally, the final design was conceived, with three stages and a total dimensions of 202μm per 56μm on Fig. 47.

Because this work deals with high frequencies, a *chassis ground* plan is strictly necessary to the circuit's proper functioning. On figure 48, it is showed an elementary cell of the *chassis ground* plan, with its three fourths of metal stretching from the substrate to the 2nd metal level, always maintaining the design rule checking with respect to the respective densities.

Finally, the complete *chassis ground* plan projected on Fig. 49.

Figure 46 – One separate stage of the DVM

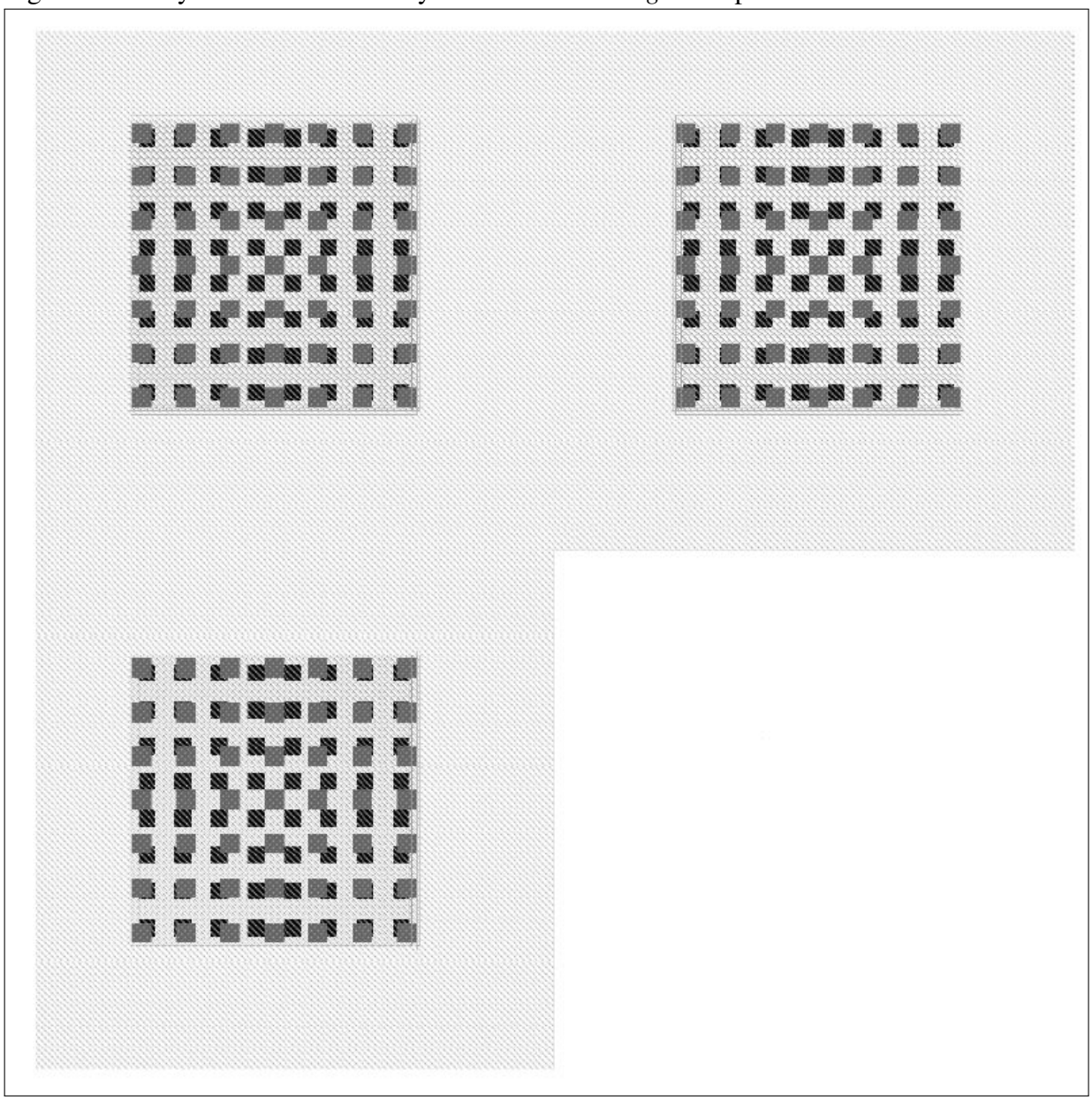


Source: (CARNEIRO; VASCONCELOS, 2015).

Figure 47 – Three Stages Dickson Voltage Multiplier's layout

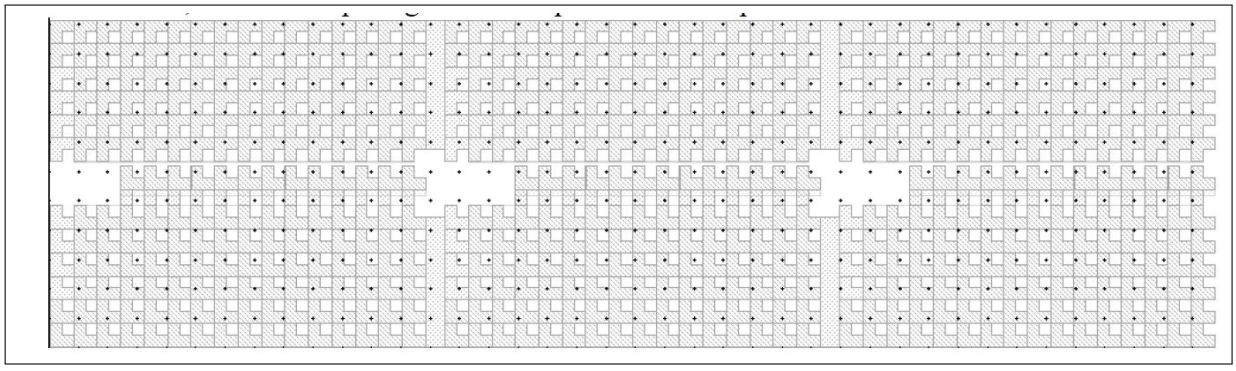
Source: (CARNEIRO; VASCONCELOS, 2015).

Figure 48 – Layout of the elementary cell of the *chassis ground* plan



Source: (CARNEIRO; VASCONCELOS, 2015).

Figure 49 – Layout of the complete *chassis ground* plan



Source: (CARNEIRO; VASCONCELOS, 2015).