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An AC–DC Isolated MMC-Based Structure Suitable for MV SST Traction Applications

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ABSTRACT This paper presents the theoretical study and experimental validation of a single-stage bidirectional ac–dc topology for solid-state transformer (SST) applications. This topology is based on the modular multilevel converter (MMC) and employs the concepts of interleaving converters and integrated power stages. A single magnetic element operating at medium frequency is employed to perform galvanic isolation and coupling between the grid-side and load-side converters. The main characteristics of the structure are derived from the aforementioned characteristics, such as passive elements operating with an effective frequency higher than the switching frequency, minimized current ripples at high frequency, as well as reduced volume and weight. Experimental results of the converter are obtained in a small-scale prototype, operating with a switching frequency of 5 kHz, nominal power of 1.5 kW, output voltage of 300 V, and the supply voltage of 165 V at a frequency of 60 Hz. High-power factor of 0.99, low-harmonic distortion of the input current with 3.6%, and efficiency in the 87% were achieved.

INDEX TERMS Bidirectional AC–DC converter, modular multilevel converter, power factor correction, medium-frequency isolation, single-stage topologies.

I. INTRODUCTION

Rail transport is one of the most widely used forms of public transportation, whose continuous development aims to provide faster and safer travels, as well as greater comfort to the passengers. More specifically, the electric railways traction is significantly different from other applications of such type, since the locomotive is supplied by a single-phase system with medium voltage and low frequency, usually by catenaries with voltage levels about 15 to 25 kV at 16.67 Hz [1]. In fact, this particularity leads to the conception of a large number of solutions in order to drive the motors of the trains, [2] and [3].

One particular solution has gained much attention in the past few years, since it demonstrates to be a good answer for the interface between the medium-voltage catenary terminals and the low-voltage locomotive motor drive system [4]. The Solid State Transformer (SST) or Power Electronic Transformer (PET) is not only limited to railway traction applications. In fact, it can also be applied to smart grid concepts as demonstrated in [5] and [6]. Although this solution has only been more deeply investigated lately, its initial conception was made a while ago, [7] and [8].

SSTs are power electronic converter associated in a particular form, which should provide galvanic isolation between a medium-voltage and low-voltage system through a medium-frequency operation. In other words, these devices allow operation in stages with frequencies higher than the catenary frequency and voltage levels lower than the catenary voltage ones.

The operation at medium frequencies has already been addressed in [9] and [10], where a significant reduction of the magnetic volume was achieved in comparison with the ones in the classical approach using the well-known low-frequency transformer (LFT) [11].

The SSTs present the same basic functionalities of a conventional power transformer, although it was found that they are not drop-in replacements for LFTs. There are still

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challenges that demand further analyses by the scientific and industry communities, together with SST's actual limitations, such as: high implementation cost and complexity, low-voltage blocking capability of semiconductors, among others [12].

On the other hand, SSTs can provides extra functionalities, over the classical LFTs, such as: bidirectional power flow control, adaptation of both voltage and frequency levels, improvements of power quality indices through reactive compensation and active harmonic filtering, voltage drop compensation and fault current limiting, feasibility for connectivity with renewable energy-based power plants, among other aspects [13].

As a way to overcome the limitation of low blocking voltage semiconductors associated with the high voltage levels typically used in traction applications, Modular Multilevel Converter (MMC) [14] topologies have recently raised the interest in this field. The innate modularity of such structures decrease the manufacturing cost, as well as simplifies assembly and maintenance issues. Moreover, it adds the applicability of spare modules, thus enhancing reliability and versatility.

The first solution presented with this characteristic was the M^2 LC in [15] in 2003, when the MMC concept was not yet established. A lot of theoretical research and practical engineering applications were elaborated since then [3] and [16]. For instance, a co-phase traction power supply system is presented in [17] as a solution for the compensation of unbalanced currents and reactive power in a 10 MVA railway system in Meishan, China.

A MMC in a back-to-back configuration is used in [1], as a power conditioner for a railway traction system based on the Scott transformer configuration and compared with other multilevel solutions. The same structure is used in [18] with the same goal, but the authors focused their efforts on the submodule voltage balancing issue, which was solved by the insertion of a power channel between the upper-side and lower-side arms of the MMC.

Even in transformless traction application [19], it is possible to find a contribution for MMCs. For instance, the work developed in [20] presents MMC-based structures with a dc-link stage, as well as single-stage solutions.

It is possible to note the large range of feasible solutions that MMC-based topologies can add to SST traction applications. In fact, it is possible to customize the topologies and its operation depending of the application goal. In this context, this paper proposes a novel power converter based on the MMC structure, which contains a single medium-frequency transformer (MFT).

The proposed converter is an interleaved multilevel modular topology integrated as the dc-stage of a single-phase SST feasible to railway traction systems. This topology was firstly introduced in [21] and [22], where the operating principles, modulation scheme for a single operation method, and simulation results were briefly presented for a for-submodule converter configuration in a medium-voltage, high-power specification. However, being part of this paper scope, the theoretical analysis and modeling, the description of the modulation technique of the primary side and the secondary side of the converter, the calculation of the semiconductor losses of the primary side of the converter, as well as the description of the control system of the proposed converter associated with experimental validation in a small-scale prototype have not been addressed up until now.

II. PROPOSED TOPOLOGY

A. CONCEPTION

The generalized proposed converter structure is presented in Fig.1, with a generic number of submodules n in each module x (upper) and y (lower). The topology is divided in two main parts: primary side and secondary side. In the primary side, there is the input inductor L_i in series with the interleaved-windings T_{11} and T_{12}, thus sharing the input current between the upper and lower modules. Moreover, h-bridge converters in a cascaded association compose such modules, bringing high voltage capability for the proposed structure.

The interleaving technique based on coupled inductors was firstly presented in [23] and its evaluation over time was summarized in [24]. The primary side of the proposed converter can be seen as a structure based on an MMC converter [14]. In fact, it can be categorized as a single leg of a Double-Star Chopper-Cell (DSCC) configuration without the common dc link, but with winding T_2 in the same magnetic structure of the interleaved windings T_{11} and T_{12}, thus providing medium-frequency operation and galvanic isolation for the secondary side.

Winding T_2, inductor L_{tr}, and an h-bridge structure compose the secondary side. Inductor L_{tr} is responsible for the power transfer between both sides. In fact, it allows the converter to act similarly as a dual active bridge (DAB) converter [25], where the voltages across the T_2, v_s, and terminals a and b of the h-bridge are phase-shifted by ϕ as presented in Fig. 1.

Fig. 2 presents an elementary circuit to represent the converter in Fig. 1 with aim to clarify the relationship of the currents and voltages of the topology, considering the positive half cycle of the ac current (i_i) and the power flow from the ac side to the dc one. To simplify the analysis, the following assumptions are made: the single magnetic element (T_{11}, T_{12}, and T_2) was separated in two different structures T_1 and T_2; the leakage inductance and the transformer magnetizing inductance are neglected; and the upper and lower modules are replaced by depended voltage sources.

From the loop analysis, it is possible to derive the relationship of voltages v_{an}, v_x and v_y, as well as the currents through the primary side.

Equation (1) represents the relationship found for v_{an}, where, v_{an} is the multilevel voltage across the grid and the input filter (L_i), v_x is the resulting voltage across the upper-side module, and v_y is the voltage across the lower module,

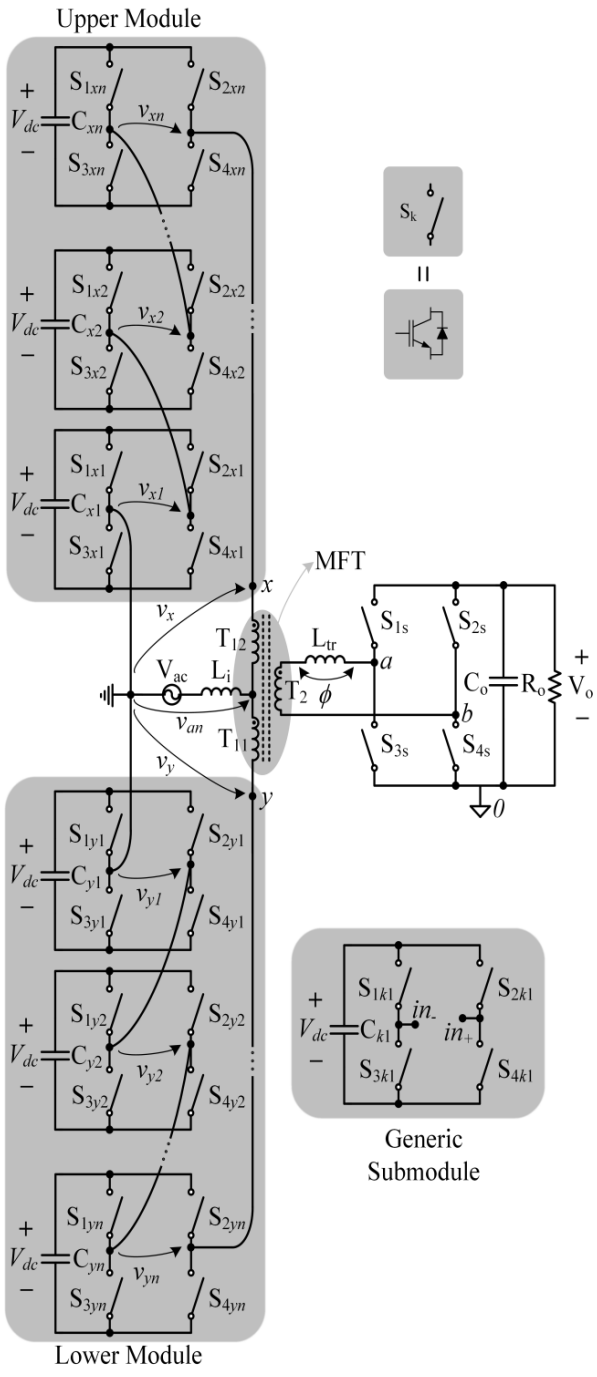

FIGURE 1. Generalized structure of the proposed topology and its inner module and submodule configurations.

which are defined by (2) and (3), respectively.

$$v_{an} = \frac{v_x + v_y}{2} \tag{1}$$

$$v_x = \sum_{k=1}^{n} v_{xk} \tag{2}$$

$$v_y = \sum_{k=1}^{n} v_{yk} \tag{3}$$

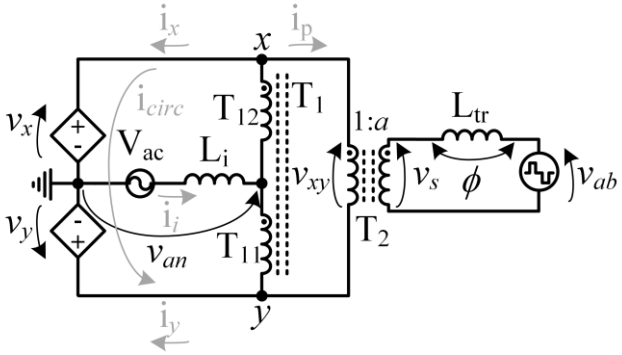

FIGURE 2. Elementary circuit of the proposed converter.

Moreover, the current through the primary winding of T_2 is defined in (4) in terms of the inductance L_{tr}, the angular frequency of the voltages across T_2, ω_{tr}, and the turns ratio of T_2 corresponding to a.

$$i_p = \frac{V_s - V_{ab}}{a \cdot \omega_{tr} \cdot L_{tr}} \tag{4}$$

The currents in T_{11} and T_{12} are the half of that through the input filter inductor L_i, since the coupled windings have the same number of turns. In fact, due the modulation technique, such currents have the same rms value. However, considering the medium-frequency representation, such quantities are phase-shifted by 180° as presented in [24].

The currents in the dependent voltage sources (i_x and i_y) can be defined as in (5) and (6) in terms of the currents through T_1 and (4).

$$i_x = \frac{i_i}{2} + i_{circ} - i_p \tag{5}$$

$$i_y = \frac{i_i}{2} - i_{circ} + i_p \tag{6}$$

Then, from (5) and (6), it is possible to determine the circulating current i_{circ}, which is described by (7).

$$i_{circ} = \frac{i_x - i_y}{2} \tag{7}$$

This current should present null average value in order to decrease its impact in the optimal operation of the converter, as well as the power losses in the submodule [26]. In fact, such current is equal to the magnetizing current in T_2, whose control system acts to avoid the saturation of the MFT.

Expression (8) gives the modulation index M, where V_{ac_pk} and V_{an_pk} are the maximum values of v_{ac} and v_{an}, respectively, being $V_{an\_pk} = n \times V_{dc}$.

$$\mathrm{M} = \frac{V_{ac\_pk}}{V_{an\_pk}} = \frac{V_{ac\_pk}}{n \cdot V_{dc}} \tag{8}$$

B. OPERATION

A 2-submodule configuration will be used to exemplify the operating principle of the converter without loss of generality. In this configuration, it is possible to define 16 operating switching states for the primary-side switches as described

in Table 1, where ss^i represents the switching state; S_{ix} and S_{iy} are the switches in the upper and lower modules, respectively. It is worth mentioning that the pairs of switches (S_{1x} and S_{3x}) and (S_{2x} and S_{4x}) operate complementary, as well as (S_{1y} and S_{3y}) and (S_{2y} and S_{4y}) in the lower module.

TABLE 1. Primary-side switching states.

	S_{1x}	S_{2x}	S_{1y}	S_{2y}	v_x	v_y	v_{an}	v_{xy}
ss^0	0	0	0	0	0	0	0	0
ss^1	0	0	0	1	0	$-V_{dc}$	$-V_{dc}/2$	$+V_{dc}$
ss^2	0	0	1	0	0	$+V_{dc}$	$+V_{dc}/2$	$-V_{dc}$
ss^3	0	0	1	1	0	0	0	0
ss^4	0	1	0	0	$-V_{dc}$	0	$-V_{dc}/2$	$-V_{dc}$
ss^5	0	1	0	1	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0
ss^6	0	1	1	0	$-V_{dc}$	$+V_{dc}$	0	$-2V_{dc}$
ss^7	0	1	1	1	$-V_{dc}$	0	$-V_{dc}/2$	$-V_{dc}$
ss^8	1	0	0	0	$+V_{dc}$	0	$+V_{dc}/2$	$+V_{dc}$
ss^9	1	0	0	1	$+V_{dc}$	$-V_{dc}$	0	$+2V_{dc}$
ss^{10}	1	0	1	0	$+V_{dc}$	$+V_{dc}$	$+V_{dc}$	0
ss^{11}	1	0	1	1	$+V_{dc}$	0	$+V_{dc}/2$	$+V_{dc}$
ss^{12}	1	1	0	0	0	0	0	0
ss^{13}	1	1	0	1	0	$-V_{dc}$	$-V_{dc}/2$	$+V_{dc}$
ss^{14}	1	1	1	0	0	$+V_{dc}$	$+V_{dc}/2$	$-V_{dc}$
ss^{15}	1	1	1	1	0	0	0	0

The signs of v_{an}, v_x and v_y were previously defined, but not in the case of v_{xy}., which is the voltage across the interleaved-windings T_{11} and T_{12}, i.e., the voltage across winding T_2 referred to the primary side as presented in Fig. 2.

It can be noted that the behaviors of voltages v_{an} and v_{xy} are redundant. Therefore, it is possible to represent the converter operation using only eight switching states. For instance, the states in Fig. 3 provide a five-level voltage v_{an} at the grid frequency, while modulating a medium-frequency three-level voltage, v_{xy}, by using the following sequence: ss^0, ss^2, ss^{10}, ss^8,ss^0, ss^4, ss^5, ss^1.

The secondary side consists in an h-bridge topology, whose switching states are given in Table 2.

TABLE 2. Secondary-side switching states.

	S_{1s}	S_{2s}	v_{a0}	v_{b0}	v_{ab}
ss^{0s}	0	0	0	0	0
ss^{1s}	0	1	0	$+V_o$	$-V_o$
ss^{2s}	1	0	$+V_o$	0	$+V_o$
ss^{3s}	1	1	$+V_o$	$+V_o$	0

It is possible to modulate a three-level voltage with such switching states in the secondary side, while the primary-side switching states can modulate voltages with other levels for v_{an}, and v_{xy} according to Fig. 3. The remaining configurations will be further analyzed in the following subsection.

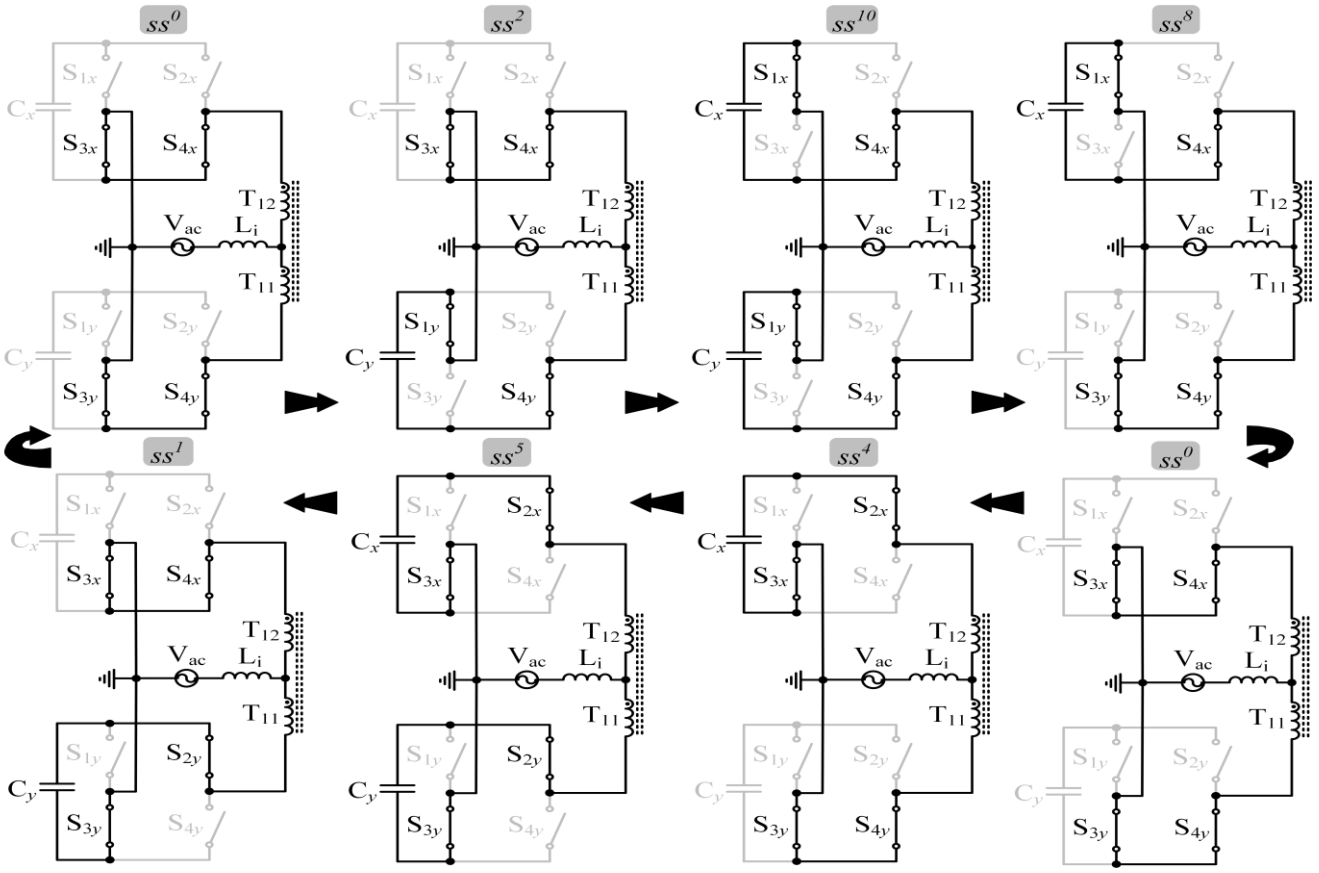

FIGURE 3. Primary-side switching states to generate a five-level voltage v_{an} and three-level voltage v_{xy}.

C. MODULATION THECHNIQUE

The main goal of the adopted modulation technique is to offer the best operating condition for the MFT, filters, and semiconductors, more particularly in terms of high power density, flexible magnetic designs, and high efficiency. For this purpose, the modulation scheme must provide the same switching frequency for each semiconductor element, but with variable duty cycle, thus allowing the proper control of some important variables, e.g., the output voltage, input current, and power flow. Moreover, it must offer the possibility for the MFT to work with fixed medium frequencies, while the topology must provide a multilevel voltage waveform in the ac side.

A proper modulation strategy for each side of the converter is proposed and described as follow.

1) PRIMARY SIDE MODULATION

The switching states presented in Table 1 are used to build the space diagram of the multilevel voltage v_{an} as a function of the MFT primary voltage v_{xy}, normalized in terms of V_{dc}. Fig. 4 presents the complete space diagram of the switching states considering up to eight submodules.

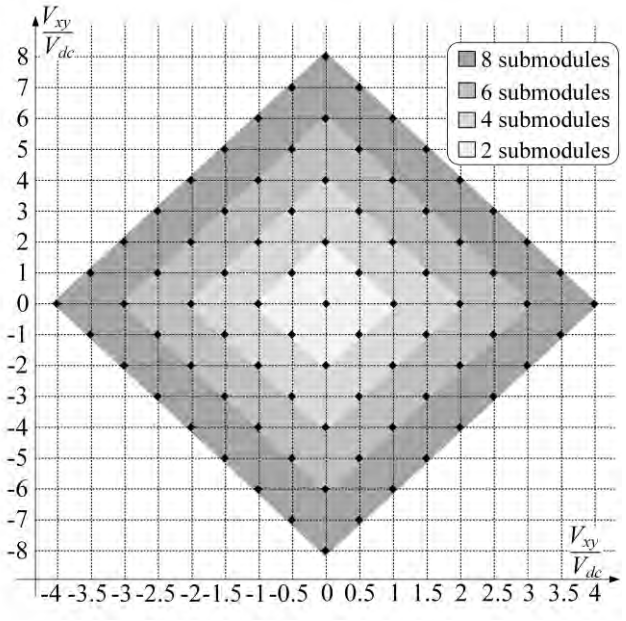

FIGURE 4. Space diagram of the switching states considering two, four, six, and eight submodules.

The adopted modulation scheme was briefly presented in [21] and considers a four-submodule configuration in this specific case, i.e. $n = 2$. Then, two modules are responsible for modulating v_x, while the other two are associated with v_y. As mentioned in the last subsection, it is possible provide the converter operation with distinct voltage levels for v_{an} and v_{xy}, although there is a limited number of combinations. Fig. 5 presents some feasible arrangements for such voltages.

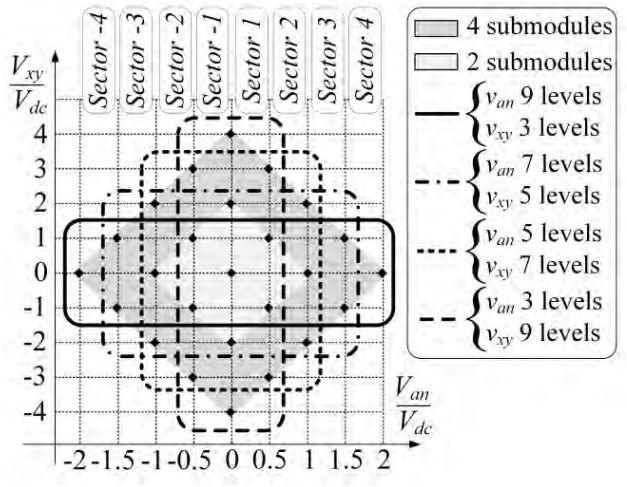

FIGURE 5. Possible voltage level characterization for v_{an} and v_{xy}, considering a four-submodule configuration.

It is possible to see that as the number of levels of a given quantity increases, the number of levels regarding the remaining one decreases. This is due to the adopted unipolar pulse width modulation (PWM) [27], which ensures the medium frequency operation of the MFT, as well as a same fixed switching frequency for the semiconductors.

It is worth mentioning that the operating frequency of v_{xy} changes with its respective number of voltage levels as shown in Fig. 6, where f_{sw} is the fixed switching frequency of the semiconductors of the submodules in the primary side.

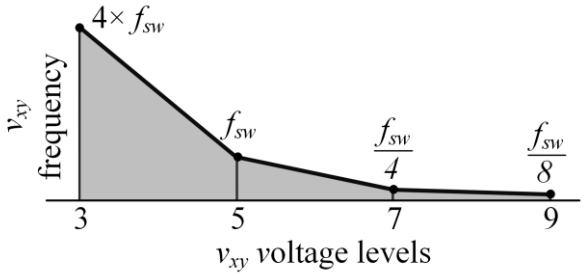

FIGURE 6. Behavior of the frequency associated with v_{xy} as a function of the respective number of voltage levels.

Then, in order to achieve high-voltage capability in the ac side associated with the medium frequency operation in the MFT, a customized unipolar PWM scheme was particularly adopted to obtain a seven-voltage waveform for v_{an} and a three-voltage waveform for v_{xy} in order to address the operation requirements of the proposed topology.

The detailed description of the modulation scheme is presented in Fig. 7. Fig. 7 (a) shows the switching logic used to generate the drive signals, while Fig. 7 (b) represents the disposition of carriers in the submodules and modules.

The modulating signals $v+$ and $v-$ are generated according to Fig. 7 (a). In fact, the modulating signals ensure an 180° phase shift between the legs of a same submodule.

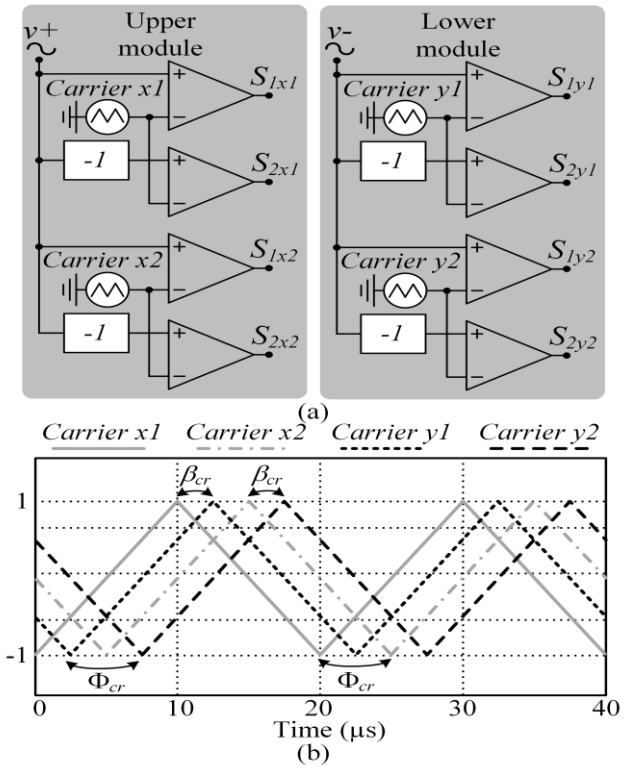

FIGURE 7. Adopted modulation scheme for the primary side of the proposed converter.

Therefore, for the upper module (x), signal $v+$ is compared with a particular carrier disposition in each submodule in order to obtain the modulated voltage v_x. An analogous scenario occurs in the lower module (y) with signal v- resulting in v_y.

Equation (9) describes the phase-shift between any two adjacent submodule carriers in a same module. Fig. 7 (b) shows such relationship for a four-submodule configuration, where both pairs of carriers (*Carrier x1 – Carrier x2* and *Carrier y1 – Carrier y2*) are phase-shifted by Φ_{cr}.

$$\Phi_{cr} = \frac{\pi}{n} \tag{9}$$

Equation (10) describes the phase-shift between the carriers of any two submodules with same superscript in a distinct module. Fig. 7 (b) also shows such relationship for both pairs of carriers (*Carrier x1 – Carrier y1* and *Carrier x2 – Carrier y2*), which are phase-shifted by β_{cr}.

$$\beta_{cr} = \frac{\pi}{2 \cdot n} \tag{10}$$

According to Fig. 1, the ac side of the converter consists in interleaved full-bridge converters operating with unipolar modulation, producing a waveform across the respective output terminals whose levels are $+V_{dc}$, 0, and $-V_{dc}$. Full-bridge converters operating with unipolar modulation provide a classical number of modules [27]. Therefore, expression (11) defines the maximum number of voltage levels for v_{an} as a function of n, particularly for the proposed converter.

$$N_{v_{an}} = 4n + 1 \tag{11}$$

This relationship is graphically expressed in Fig. 4 and Fig. 5, where the maximum number of levels is nine, considering a four-submodule configuration. Moreover, the maximum number of levels for v_{xy} is N_{vxy}, which depends on the frequency configuration adopted for the MFT as established in Fig. 6. This configuration limits N_{vxy}, since in SST applications a medium frequency in the MFT is desirable, while such frequency ratings are still a bottleneck to be overcome in high power application.

It is important to note that the number of submodules varies according to the grid voltage and the blocking voltages of the semiconductors used in the converter. Thus, from (8) and (11), it is possible to obtain the maximum number of voltage levels for v_{an} as a function of M as described in (12).

$$N_{v_{an}} = \frac{4 \cdot V_{ac\_pk}}{M \cdot V_{dc}} + 1 \tag{12}$$

Parameter N_{van} may vary with M, since V_{ac_pk} and V_{dc} can be considered constant during the steady-state operation of the converter. Then, expression (13) describes the behavior of N_{van} when varying M.

$$N_{v_{an}} = \begin{cases} 3 & \text{if } 0 < M \leq 0.3 \\ 5 & \text{if } 0.3 \leq M \leq 0.5 \\ 7 & \text{if } 0.5 \leq M \leq 0.7 \\ 9 & \text{if } 0.7 \leq M \leq 1 \end{cases} \tag{13}$$

Fig. 8 shows the main theoretical multilevel voltage waveforms multilevel generated in the primary side of the converter.

At four different instants (t_1, t_2, t_3 and t_4), it can be noticed that voltage v_{xy} as applied to the transformer inverts its phase with respect to the previous one. In fact, during the transition from *Sector 2* to *Sector 3* in Fig. 5, v_{xy} repeats its previous behavior at instant t_1, resulting in a phase shift of 180°, a presented in Fig. 8. The same behavior occurs at t_2 when the transition is from *Sector 3* to *Sector 2*(Fig. 5). For the negatives values of v_{an}, other two instants t_3 and t_4 occur for the transitions from *Sector -2* to *Sector -3* and from *Sector -3* to *Sector -2*, respectively.

In order to overcome such inconvenient and ensure the accurate operation of the control loops, the secondary-side modulation strategy must aggregate such phase transitions to the switching sequence. The adopted strategy will be addressed in the next subsection.

2) SECONDARY-SIDE MODULATION

Unipolar PWM is adopted in the full-bridge converter connected to the secondary-side of the structure. The modulator applied in the comparator should have the same shape as the effective duty cycle value applied to the primary windings of the transformer for the reasons presented in the end of the last subsection. Thus, Fig. 9 shows the graphic behavior of such effective duty cycle, which is analytically descried

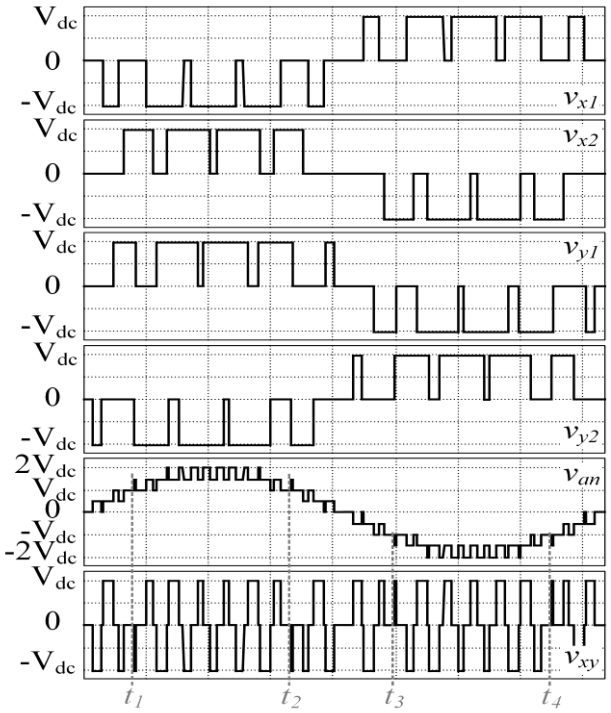

FIGURE 8. Main theoretical multilevel voltage waveforms considering the adopted modulation scheme.

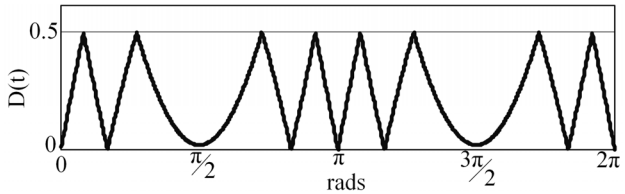

FIGURE 9. Effective duty cycle associated to voltage v_{xy}.

by (15), where $m(t) = 0.99\sin(\omega_{grid} \cdot t)$, ω_{grid} is the angular grid frequency, and t_s is the switching period.

$$D(t) = \begin{cases} 2 \cdot f_s \cdot t_s \, |m(t)| \,, & \text{if } 0 < |m(t)| \leq 0.25 \\ 2 \cdot f_s \cdot t_s \left(\frac{1}{2} - |m(t)| \right), & \text{if } 0.25 \leq |m(t)| \leq 0.5 \\ 2 \cdot f_s \cdot t_s \left(|m(t)| - \frac{1}{2} \right) & \text{if } 0.5 \leq |m(t)| \leq 0.75 \\ 2 \cdot f_s \cdot t_s \left(1 - |m(t)| \right) & \text{if } 0.75 \leq |m(t)| \leq 1 \end{cases} \tag{14}$$

Fig. 10 presents the block diagram detailing the modulation scheme and its particularities. It is possible to see that the secondary-side modulating signal is obtained from the modulating sine wave generated by the input current controller combined with (15), resulting in the same shape as presented in Fig. 9. The carrier signals are lagged by 180° from each other and, from Fig. 6, their respective frequency must be four times higher than that associated with the frequency of the carriers used in the primary side. The carriers uses angle ϕ to

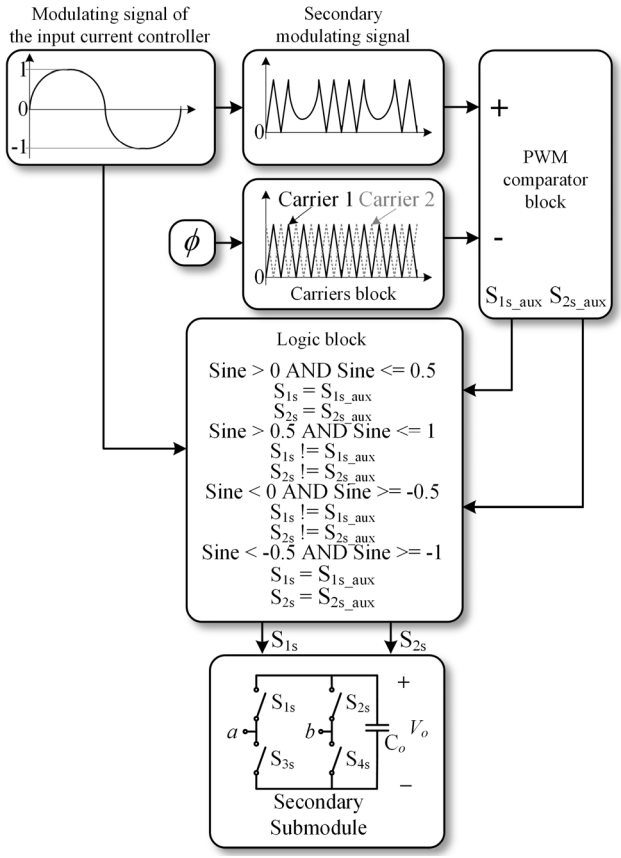

FIGURE 10. Block diagram of the secondary modulation.

generate the requested phase shift between v_s and v_{ab} as seen in Fig. 2 for controlling the power flow between the ac and the dc sides of the converter.

In the PWM comparator block, the secondary-side modulating signal is compared with the carriers, resulting in the auxiliary gate signals for switches S_{1s} and S_{2s}. After that, the logic block will use the modulating signal from the input current control loop to choose the final decision for the states of switches S_{1s} and S_{2s}. In fact, the block identifies the sectors of the modulating signal in order to find the phase shift inversion of v_{xy} (see Fig. 8) and then, it decides whether the pulses must receive complementary signals from the auxiliary gating signals.

This logic action is necessary to ensure the angle ϕ between v_s and v_{ab}, regardless the behavior of v_s imposed by the primary-side operation. Then, it is possible control the direction of the current through inductor L_{tr} analogously to a DAB converter and power flow as a consequence, while bidirectionality can be achieved.

D. CONTROL SYSTEM

The goals of the adopted control strategy are described as follows:

-firstly, the input current must be sinusoidal and in phase with the input voltage.

-secondly, the average voltage across submodules capacitors must be the same;

-thirdly, the average values of voltages v_x and v_y must equal to each other;

-fourthly, the output voltage must be regulated.

Fig. 11 shows the block diagram of the proposed control strategy. The control circuit consists of four loops. Loop (II) maintains the average value of the capacitor voltages across the submodules at the nominal value, generating the peak signal of the current drawn from the ac port. After being multiplied by the reference sinusoidal signal, the output of block (II) becomes the reference of block (I), which is responsible for controlling the current of the ac port, thus ensuring that the converter operates with high power factor.

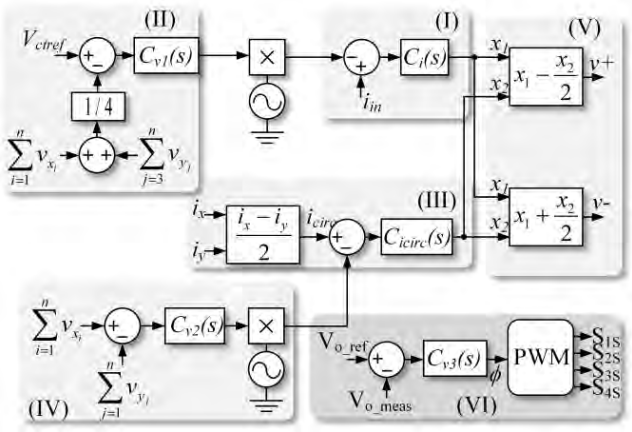

FIGURE 11. Block diagram of the proposed control strategy.

The balance between the sum of the voltages of each module is realized by the loop (IV), which generates a signal that, when multiplied by the sinusoidal reference, generates a negative offset to be applied as reference of the circulation current. Loop (III) is responsible for regulating the signal of the circulating current with null offset.

Block (V) is used to decompose the control signal. Signal decomposition is required to produce a small displacement between the modulating signals $v+$ and $v-$ in order to balance the voltages across the upper and lower modules.

Loop (VI) controls the voltage across the DC port, which is achieved by means of the angular phase difference of the voltages v_s and v_{ab} applied to inductor L_{tr} as seen in Fig. 1. The phase-shift angle is obtained by comparing the measured DC voltage with a reference signal, thus generating an error applied to a proportional-integral (PI) controller. The controller output signal is converted into an angle by means of the gyrator based on [28] and [29].

The PI structure were used for all control loops, but in block (I), where it was applied a Proportional-Resonant (PR) controller in order to provides null error in steady state for sinusoidal references. Table 3 presents the design parameters for each used controller, considering a phase margin of 60°.

TABLE 3. Controllers specifications.

Frequencies	Controllers				
	C_i	C_{icirc}	C_{v1}	C_{v2}	C_{v3}
Crossing	1.25 kHz	400 Hz	12 Hz	6 Hz	100 Hz
Zero	722 Hz	215 Hz	66 Hz	5.52 Hz	57.9 Hz
Grid	60 Hz	–	–	–	–
Cut	0.1 Hz	–	–	–	–

III. ANALYSIS OF LOSSES PRIMARY SIDE

For the estimation of losses in the semiconductors of the primary side, the converter is considered to operate in inverter mode i.e. an ideal dc voltage source is connected to the converter dc link in the secondary side, while a load R_L replaces the ac source representing the grid. Thus power flows from the secondary side to the primary one considering the parameters presented in Table 4.

TABLE 4. Converter specifications.

Specifications	Values
Output power	1500 W
Output voltage	300 V
Input *rms* voltage	165 V
Transformer ratio	1:1.45
Power transfer inductance L_{tr}	50 µH
Switching frequency	5 kHz
Number of submodules	4

It is necessary to determine the average and rms currents through the primary side of the converter to calculate the losses. Thus, from (4), (5), and (6) as a function of time, it is possible to obtain the waveforms of the currents through the primary winding and modules x and y as shown in Fig. 12 and 13, respectively.

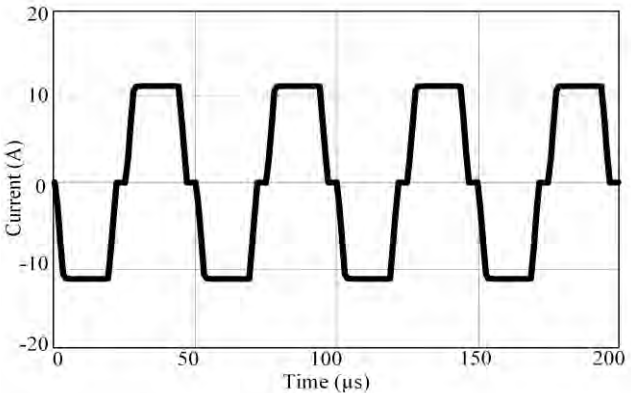

FIGURE 12. Current through the primary winding.

Assuming that currents i_x and i_y vary as a function of time, it is possible to obtain their respective rms and average values over one period of the grid voltage.

Table 5 shows the calculated values for the currents through the diodes and switches, which allow determining the conduction losses in the semiconductors.

In order to assess the overall losses of the prototype, Insulated Gate Bipolar Transistors (IGBT) IRGP4063D are used, as well as ultrafast diodes available in laboratory.

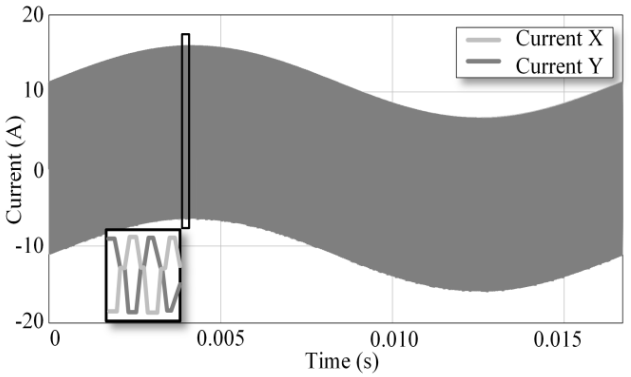

FIGURE 13. Current i_x and i_y.

TABLE 5. Currents through the semiconductors.

Average and rms currents	Calculated values [A]
$I_{Ss1average}$	2.52
$I_{Ss2average}$	2.51
I_{Ss1rms}	3.36
I_{Ss2rms}	
$I_{D1average}$	2.69
$I_{D2average}$	2.67
I_{D1rms}	3.51
I_{D2rms}	3.50

Conduction losses are given by (15) and (16), where V_{ce} is the maximum collector-emitter voltage, R_s is the IGBT on-resistance, V_F is the forward voltage drop across the antiparallel diode, and R_D is the resistance of the antiparallel diode. For comparison purposes, IGBTs model IKB40N65ES5 are employed.

$$P_{S1,2cond} = V_{ce} \cdot i_{S1,2average} + R_s \cdot i^2_{S1,2rms} \quad (15)$$

$$P_{D1,2cond} = V_F \cdot i_{D1,2average} + R_D \cdot i^2_{D1,2rms} \quad (16)$$

The switching losses regarding the switches and diodes are obtained from (17) and (18), respectively.

$$P_{S1,2com\_on} = \frac{1}{2}\int_0^{t_{s\_}} f_{sw} \cdot W_{S1,2com\_on}(t) \cdot dt \quad (17)$$

$$P_{S1,2com\_off} = \frac{1}{2}\int_0^{t_{s\_}} f_{sw} \cdot W_{S1,2com\_off}(t) \cdot dt \quad (18)$$

Parameters $W_{S1,2sw\_on}$ and $W_{S1,2sw\_off}$ represent the total dissipated energy associated with the turning on and turning off acts, as expressed by (19) and (20), respectively. Besides, coefficients $K_{2on} = 0.004$, $K_{1on} = 0.003$, $K_{0on} = 0.0017$, $K_{2off} = 0.0047$, $K_{1off} = 0.003$, and $K_{0off} = 0.0016$ are obtained from IRGP4063D datasheet. Coefficients $K_{2on} = 0.0016$, $K_{1on} = 0.0011$, $K_{0on} = 0.0004$, $K_{2off} = 0.00079$, $K_{1off} = 0.00065$, and $K_{0off} = 0.0003$ are obtained from IKB40N65ES5 datasheet, as well.

$$W_{S1,2com\_on} = K_{2on} \cdot i_{S1,2}(t)^2 + K_{1on} \cdot i_{S1,2}(t) + K_{0on} \quad (19)$$

$$W_{S1,2com\_off} = K_{2off} \cdot i_{S1,2}(t)^2 + K_{1off} \cdot i_{S1,2}(t) + K_{0off} \quad (20)$$

Equations (15) to (20) define the total conduction and switching losses associated with the switches, and also the total conduction losses in the diodes. Considering the losses calculated in the IGBTs, neglecting the losses of the converter connected to the secondary side and losses in the passive elements of the converter, the total losses associated with IRGP4063D are 182.61W, while the ones calculated for IKB40N65ES5 are 99.11W.

Fig. 14 shows a comparison of the losses in IGBT IRGP4063D, with those in IGBT IKB40N65ES. It can be stated that the losses in IRGP4063D are higher. In addition, the highest portion is associated with the diode co-pack. Finally, it is worth to mentioned that IRGP4063D was used in the implementation of the experimental prototype.

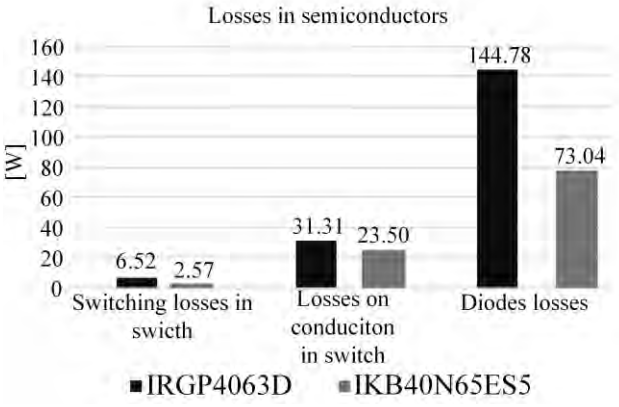

FIGURE 14. Distribution of switching and conduction losses.

IV. DISCUTION OF RESULTS

A. EXPERIMENTAL SETUP

In order to verify the operation and evaluate the performance of the proposed converter, experimental tests were carried out in accordance with the specifications given in Table 6.

TABLE 6. Prototype specifications and parameters.

Specifications	Values
Output power	1500 W
Output voltage	300 V
Rms input voltage	165 V
Transformer turns ratio	1:1.45
Switching frequency	5 kHz
Grid frequency	60 Hz
Number of submodules	4
Modulation index	0.56
Capacitance per submodule	1100 µF
Input inductance, L_i	500 µH
Power transfer inductance, L_{tr}	50 µH

Fig. 15 shows the small-scale experimental prototype used to obtain some practical results. The Texas Instruments Delfino family microcontroller TMS320F28379D was used to embedded the control strategies and the proposed modulation technique. Although the experimental prototype presents

a six-submodule configuration, the modulation and control schemes were implemented considering a four-submodule one.

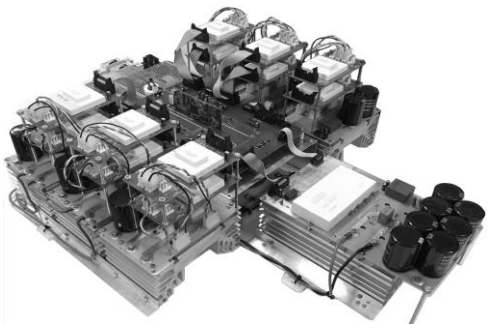

FIGURE 15. Experimental prototype.

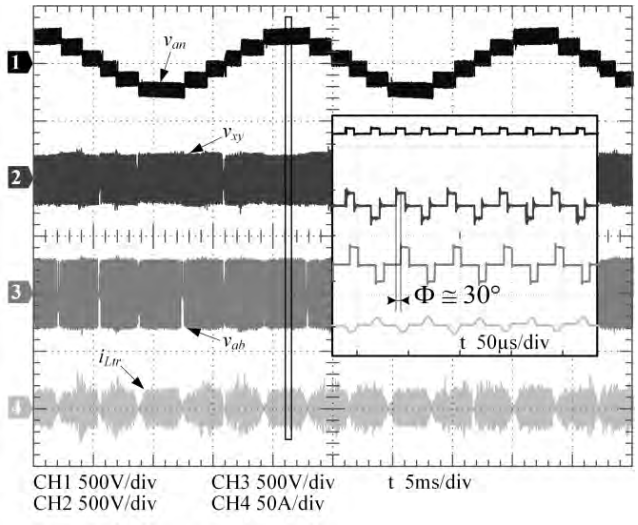

FIGURE 16. Voltage v_{an} (CH1), voltage v_{xy} (CH2), voltage v_{ab} (CH3) and secondary-side current, i_{Ltr} (CH4).

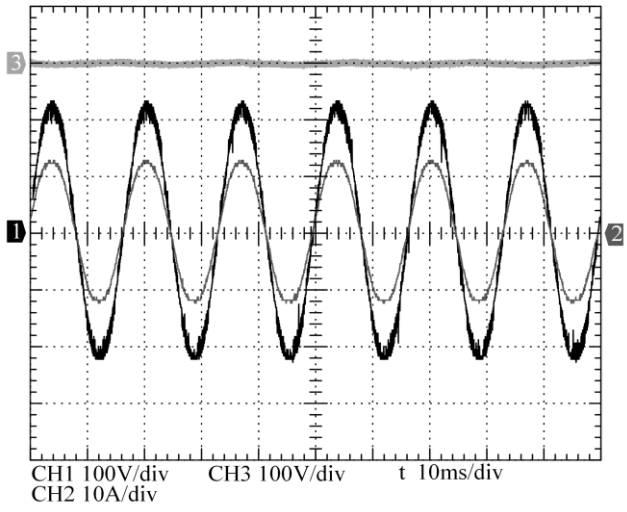

FIGURE 17. Grid voltage (CH1), input current (CH2) and dc output voltage (CH3).

B. STEADY-STATE OPERATION

In this section, experimental results are presented for the converter operating as rectifier in steady-state condition.

Fig. 16 shows the waveforms of voltages v_{an} (CH1), v_{xy} (CH2), v_{ab} (CH3) and the current in the secondary side i_{Ltr} (CH4) of the transformer. Voltage v_{an} has a rms value of 219.1 V, voltage v_{xy} has a rms value of 131.2 V, voltage v_{ab} across the secondary side H-bridge has an *rms* value of 190.2 V and current i_{Ltr} has a rms value of 11 A. The input active power is about 1,875 W. Voltage v_{ab} is about 30° lagged with respect to v_{xy} in order to provide power transfer from the grid to the load.

Fig. 17 shows the grid voltage (CH1), whose rms value is 165 V. The input current (CH2) has a rms value of 11.36 A, being in phase with the grid voltage. Its respective total harmonic distortion (THD_I) is equal to 3.64 %, resulting in a

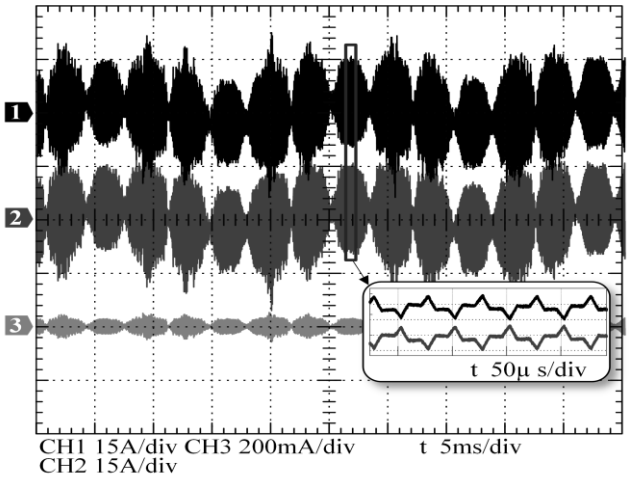

FIGURE 18. Current i_x (CH1) in the upper-side module, current i_y (CH2) in the lower-side module and circulating current, i_{circ} (CH3).

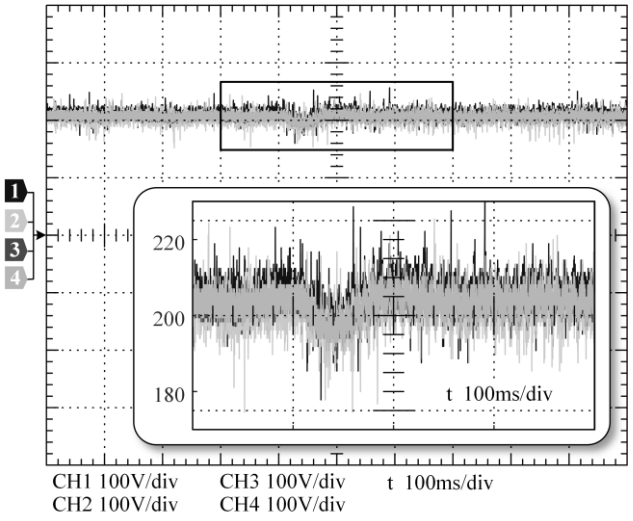

FIGURE 19. Dc voltages across the capacitors used in the submodules during a load step from 50% to 100% of the rated power.

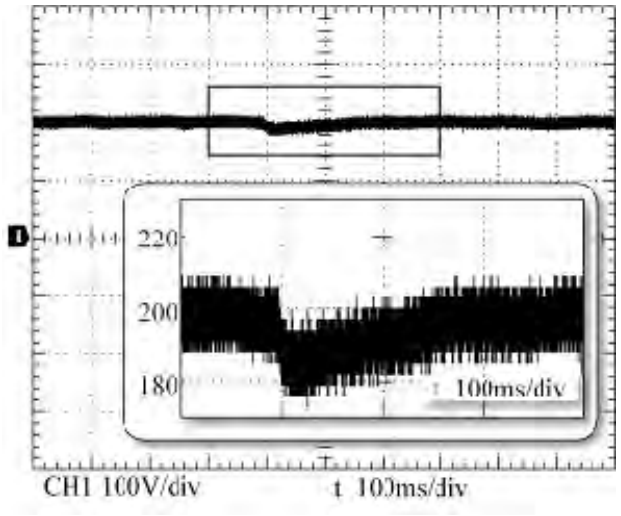

FIGURE 20. DC output voltage during load step of 50% from 100%.

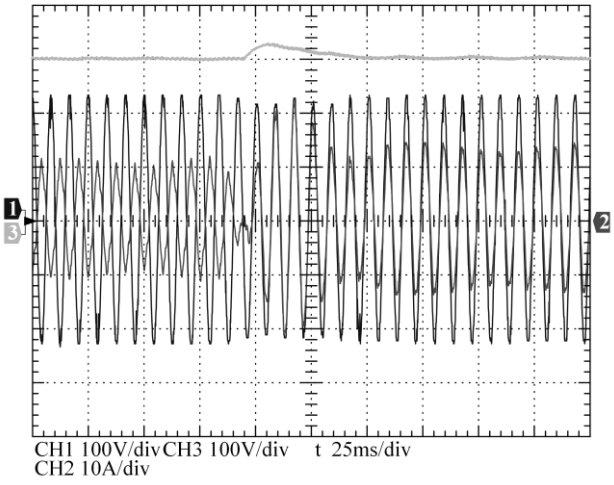

FIGURE 21. Grid voltage (CH1), input current (CH2), and DC output voltage (CH3) during the power flow inversion.

power factor of 0.99. Besides, the rms value of the dc output voltage (CH3) is 300 V.

For an output power of 1.5 kW, the converter input power is 1.687 kW, while the resulting efficiency is 87.5%.

Fig. 18 shows current i_x in the upper module, current i_y in the lower module, and also the circulanting current i_{circ}. Both currents i_x (CH1) and i_y (CH2) have rms values of 10.86 A, and the circulating current (CH3) has an average value close to zero, which ensures that transformer saturation will not occur. Moreover, currents i_x and i_y are in phase with each other at low frequency, but lagged by 180° at high frequency.

C. DYNAMIC BEHAVIOR

In this section, experimental results on the converter dynamic behavior are presented considering both tests with load step from 50% to 100% of the rated power and also the inversion of power flow direction.

Fig. 19 shows the dc voltages across the capacitors used in the sub-modules during a positive load step, which occurs at $t = 490$ ms with a voltage sag of 7.07 %.

Fig. 20 shows the dc output voltage during the positive load step up, which occurs at $t = 400$ ms. It is noted a voltage sag of 6.66 % and setting time of 170 ms.

Fig. 21 shows the grid voltage (CH1), input current (CH2) and dc output voltage (CH3) during the power flow inversion, which occurs during the transition from inverter to rectifier mode, as it takes about seven grid cycles to reach the steady-state condition. The dc output voltage presents an overshoot of 7.66 %.

V. CONCLUSION

A bidirectional ac-dc modular multilevel converter based on interleaving of cascade full-bridge cells has been presented in this paper. The theoretical analysis, design procedures, and experimental results for the proposed topology have been presented and discussed to validate the operation of the proposed topology. In fact, they demonstrate the operation of the proposed converter at high power factor condition, i.e. 0.99 and low harmonic distortion of the input current, i.e. 3.64%. Considering that the losses regarding the passive elements and the semiconductors connected to the secondary side of the converter have been neglected, an efficiency of 87.5 % obtained experimentally shows to be a coherent result, since the theoretical efficiency was about 90 %. Although this is considered to be a low value for SSTs, this limitation can be overcome with the use of semiconductors with improved characteristics, while overall efficiency may reach 93% or even higher ratings as demonstrated by IGBT modules IKB40N65ES5.

The PS-PWM modulation scheme and the average current mode control strategy associated with the additional voltage balance and circulating current control loops demonstrate to be an adequate approach for the proposed converter operation. In addition, the modulation technique provides a higher operating frequency for the magnetic elements, thus leading to reduced weight and volume of the converter.

REFERENCES

[1] Q. Xu, F. Ma, Z. He, Y. Chen, J. M. Guerrero, A. Luo, Y. Li, and Y. Yue, "Analysis and comparison of modular railway power conditioner for high-speed railway traction system," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6031–6048, Aug. 2017.

[2] A. Iraklis, T. Schirmer, H. Dittus, A. Lusiewicz, and J. Winter, "Overview of three-stage power converter topologies for medium frequency-based railway vehicle traction systems," *IEEE Trans. Veh. Technol.*, vol. 68, no. 4, pp. 3268–3278, Apr. 2019.

[3] J. Feng, W. Q. Chu, Z. Zhang, and Z. Q. Zhu, "Power electronic transformer-based railway traction systems: Challenges and opportunities," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 1237–1253, Sep. 2017.

[4] L. H. S. C. Barreto, D. de A. Honório, D. de Souza Oliveira, and P. P. Praça, "An interleaved-stage AC–DC modular cascaded multilevel converter as a solution for MV railway applications," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3008–3016, Apr. 2018.

[5] L. F. Costa, G. D. Carne, G. Buticchi, and M. Liserre, "The smart transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid," *IEEE Power Electron. Mag.*, vol. 4, no. 2, pp. 56–67, Jun. 2017.

[6] F. Nejabatkhah, Y. W. Li, and H. Tian, "Power quality control of smart hybrid AC/DC microgrids: An overview," *IEEE Access*, vol. 7, pp. 52295–52318, 2019.
[7] W. Mcmurray, "Power converter circuits having a high frequency link," U.S. Patent 3 517 300, Jun. 23, 1970.
[8] J. L. Brooks, "Solid state regulated power transformer with waveform conditioning capability," U.S. Patent 4 347 474, Aug. 31, 1982.
[9] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.
[10] J. W. Kolar and G. Ortiz, "Solid-state-transformers: Key components of future traction and smart grid systems," in *Proc. Int. Power Electron. Conf. (IPEC)*, Hiroshima, Japan, 2014, pp. 1–15.
[11] D. Honório, D. Oliveira, and L. H. Barreto, "An AC-DC multilevel converter feasible to traction application," in *Proc. 17th Eur. Conf. Power Electron. Appl. (EPE ECCE-Europe)*, Geneva, Switzerland, 2015, pp. 1–9.
[12] J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in today's and future distribution grids," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 317–326, Jan. 2019.
[13] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 29–42, Sep. 2016.
[14] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.
[15] M. Glinka and R. Marquardt, "A new AC/AC-multilevel converter family applied to a single-phase converter," in *Proc. IEEE 5th Int. Conf. Power Electron. Drive Syst. (PEDS)*, vol. 1, Nov. 2003, pp. 16–23.
[16] Z. Shu, S. Xie, K. Lu, Y. Zhao, X. Nan, D. Qiu, F. Zhou, S. Gao, and Q. Li, "Digital detection, control, and distribution system for co-phase traction power supply application," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1831–1839, May 2013.
[17] D. Ronanki and S. S. Williamson, "Modular multilevel converters for transportation electrification: Challenges and opportunities," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 2, pp. 399–407, Jun. 2018.
[18] W. Liu, K. Zhang, X. Chen, and J. Xiong, "Simplified model and submodule capacitor voltage balancing of single-phase AC/AC modular multilevel converter for railway traction purpose," *IET Power Electron.*, vol. 9, no. 5, pp. 951–959, 2016.
[19] K. Mainali, A. Tripathi, S. Madhusoodhanan, A. Kadavelugu, D. Patel, S. Hazra, K. Hatua, and S. Bhattacharya, "A transformerless intelligent power substation: A three-phase SST enabled by a 15-kV SiC IGBT," *IEEE Power Electron. Mag.*, vol. 2, no. 3, pp. 31–43, Sep. 2015.
[20] M. Coppola, A. Del Pizzo, and D. Iannuzzi, "A power traction converter based on Modular Multilevel architecture integrated with energy storage devices," in *Proc. Elect. Syst. Aircr., Railway Ship Propuls.*, Bologna, Italy, 2012, pp. 1–7.
[21] J. O. Pacheco, F. J. B. Brito, and D. S. Oliveira, Jr., "Bidirectional AC-DC modular multilevel converter based on the three-state switching cell," in *Proc. IEEE 13th Brazilian Power Electron. Conf. 1st Southern Power Electron. Conf. (COBEP/SPEC)*, Fortaleza, Brazil, Nov./Dec. 2015, pp. 1–5.
[22] J. de Oliveira Pacheco, F. J. B. Brito, Jr., D. R. Joca, J. L. W. Oliveira, Jr., P. P. Praça, and D. de Souza Oliveira, Jr., "Bidirectional modular multilevel PFC rectifier based on cascading full-bridge and interleaving technique suitable for SST applications," in *Proc. 12th IEEE Int. Conf. Ind. Appl. (INDUSCON)*, Curitiba, Brazil, Nov. 2016, pp. 1–7.
[23] G. V. Torrico-Bascope and I. Barbi, "A single phase PFC 3 kW converter using a three-state switching cell," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, vol. 5, Jun. 2004, pp. 4037–4042.
[24] B. Cougo, T. Friedli, D. O. Boillat, and J. W. Kolar, "Comparative evaluation of individual and coupled inductor arrangements for input filters of PV inverter systems," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst. (CIPS)*, Nuremberg, Germany, 2012, pp. 1–8.
[25] R. W. De Donker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.
[26] G. Konstantinou, J. Pou, S. Ceballos, R. Picas, J. Zaragoza, and V. G. Agelidis, "Control of circulating currents in modular multilevel converters through redundant voltage levels," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7761–7769, Nov. 2016.
[27] D. G. Holmes, T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley, 2003.
[28] W. M. dos Santos, M. S. Ortmann, R. Schweitzer, S. A. Mussa, and D. C. Martins, "Design and conception of a DAB converter (Dual Active Bridge) using the gyrators theory," in *Proc. 11th Brazilian Power Electron. Conf.*, Brazil, Natal, 2011, pp. 359–364.
[29] H. R. Mamede, W. M. dos Santos, and D. C. Martins, "A new DC-DC power converter derived from the TAB for bipolar DC microgrids," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Montreal, QC, Canada, Sep. 2015, pp. 6217–6222.

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