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# Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter

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**Abstract:** The major consideration in dc–dc conversion is often associated with high efficiency, reduced stresses involving semiconductors, low cost, simplicity and robustness of the involved topologies. In the last few years, high-step-up non-isolated dc–dc converters have become quite popular because of its wide applicability, especially considering that dc–ac converters must be typically supplied with high dc voltages. The conventional non-isolated boost converter is the most popular topology for this purpose, although the conversion efficiency is limited at high duty cycle values. In order to overcome such limitation and improve the conversion ratio, derived topologies can be found in numerous publications as possible solutions for the aforementioned applications. Within this context, this work intends to classify and review some of the most important non-isolated boost-based dc–dc converters. While many structures exist, they can be basically classified as converters with and without wide conversion ratio. Some of the main advantages and drawbacks regarding the existing approaches are also discussed. Finally, a proper comparison is established among the most significant converters regarding the voltage stress across the semiconductor elements, number of components and static gain.

## 1 Introduction

Wide voltage conversion ratio often is demanded in numerous applications that include renewable energy systems [1], motor drives [2], uninterruptible power systems [3], electric vehicles [4] and many others. Typically, it is necessary to step up low voltages from batteries, photovoltaic (PV) modules, fuel cells and wind turbines so that a cascade dc–ac stage can be supplied [5]. In this case, low dc voltages ranging from 12 to 125 V must be stepped up to 300 V or 400 V so that rms ac voltages equal to 127 V or 220 V can be obtained [6].

There are numerous isolated dc–dc converter topologies proposed in the literature, which can provide high-voltage gain by increasing the turns ratio of the high-frequency transformer. The phase-shift full-bridge converter is by far one of the most popular ones, where it is possible to achieve zero-voltage switching over a wide load range by using the high-leakage inductance of the transformer. However, significant drawbacks exist, such as high-circulating current, the voltage stress across the output diode becomes much higher than the output voltage, and efficiency is reduced in applications where the output voltage is high [7]. Besides, the pulsating input current is prohibitive in some applications, for example, PV systems because it can reduce the useful life of arrays, as large electrolytic capacitors are necessary to reduce the appreciable input current ripple [1].

In applications where galvanic insulation is not a must, non-isolated dc–dc converters can be used to achieve voltage step-up or step-down, with consequent reduction of size, weight and volume associated to the increase of efficiency because of the lack of a high-frequency transformer [8]. The classical or conventional dc–dc boost converter is widely employed in voltage step-up, being studied in many books on power electronics [9–11]. The buck–boost converter can be also used in voltage step-up, but the voltage stress regarding both semiconductor elements is equal to the sum of the input voltage and the output voltage. It also occurs in the classical Ćuk, SEPIC (single-ended primary inductance converter) and zeta topologies, although the higher component count and complexity exist [12]. Some effort has also been made towards the conception of hybrid structures involving boost and Ćuk topologies, but at the cost of additional elements without improving the static gain characteristic [13].

By using passive components and semiconductor elements, that is, one input inductor, one output filter capacitor, one active switch and one diode, it is possible to control the duty cycle so that the output voltage becomes higher than the input voltage in the boost converter [14]. Being a simple structure, its main advantages are low cost associated with low component count, use of simple drive circuitry since the input source and the load are connected to the same reference node, and non-pulsating input current when operating in continuous-conduction mode (CCM). However, some drawbacks still exist related to the voltage stresses across the diode and a switch, which are equal to the output voltage. This issue may limit its use in high-output voltage applications, where the reverse recovery of the diode is also of major concern.

Considering an ideal converter without losses, the output voltage tends to infinite as the duty cycle tends to unity in the boost converter. However, this cannot be achieved in practice because high cost and precise drive circuitry would be necessary to avoid low variations in the duty cycle to affect the output voltage drastically. Parasitic elements, for example, the intrinsic resistance of the filter inductor also limit the static gain to a finite value in practical terms.

For applications involving wide voltage conversion ratios, which typically cannot be achieved by conventional non-isolated dc–dc converters, there are several possible solutions. Perhaps one of the earliest papers on this subject is the one proposed in [15], where single-switch buck, boost and buck–boost-based converters are then derived, although they are simple topological variations of cascaded converters. The so-called quadratic converters allow obtaining high-voltage step-up or step-down by simply considering

that the total static gain is equal to the product between the static gains of two individual converters [16]. Some inherent advantages and disadvantages can be addressed to such topologies, which will be analysed in detail as follows.

For high-power applications, the boost converter is not a feasible solution because the load power is processed by only two semiconductors, while appreciable current and/or voltage stresses exist. Particularly in high-current applications, conduction losses lead to the significant reduction of efficiency because they increase with the square of the rms current through the semiconductors. Although the parallelism of switches or even converters is possible, current sharing is compromised because of the intrinsic differences of the involved elements [17].

Considering the main limitations of the classical boost converter, several works have been proposed in the literature to improve key issues, such as the static gain, voltage stress across the semiconductors, efficiency, power capacity and many other aspects of the original topology. The simultaneous search for the terms 'dc–dc' and 'boost converter' in IEEEXPlore® Digital Library demonstrates the relevance of this subject, revealing that more than 4000 papers have been published in conferences and journals over the last decades.

This work is then motivated by an attempt to properly analyse and classify some of the most popular non-isolated dc–dc boost-based converters available in the literature because of their increasing choice for voltage step-up applications. Since several approaches exist, they can be classified as either converters without wide conversion range or converters with wide conversion range [18]. Initially, let us discuss and quantify some of the main limitations of the conventional boost converter in CCM, which have led to the proposal of novel topologies. Considering intrinsic advantages and disadvantages, the existing structures include interleaved converters, three-level converters, cascaded converters, coupled-inductor-based converters, switched-capacitor-based converters and converters based on the three-state switching cell (3SSC). A thorough discussion is carried out in this paper and the aforementioned aspects are analysed in detail.

## 2 Conventional boost converter

As it was mentioned before, the static gain of the conventional boost converter is limited in practice because the high-output voltage demands high duty cycle values, thus leading the switch to remain on for long time intervals. If the current through the diode is high, serious drawbacks regarding the reverse-recovery phenomenon tend to exist. Therefore it is important that the static gain does not rely only on the duty cycle in high-voltage step-up applications [19, 20].

The conventional boost converter is shown in Fig. 1*a*, where the intrinsic series resistance of the inductor is represented by $R_L$. By using the volt-second balance principle and considering the operation in CCM, it is easy to demonstrate that the static gain $G_v$ is given by

$$G_v = \frac{V_o}{V_i} = \frac{1}{1-D} \cdot \frac{1}{\left(1 + (R_L/((1-D)^2 \cdot R_o))\right)} \quad (1)$$

where $V_o$ is the output voltage, $V_i$ is the input voltage, $R_o$ is the load resistance and $D$ is the duty cycle.

Besides, the theoretical efficiency of the boost converter given by $\eta$ can be estimated by the following expression

$$\eta = \frac{1}{\left(1 + (R_L/((1-D)^2 \cdot R_o))\right)} \quad (2)$$

According to (1) and (2), both static gain and efficiency depend on $R_L$, $D$ and $R_o$, while the analysis of the aforementioned expressions leads to interesting conclusions. Initially, let us plot the static gain in (1) as a function of the duty cycle for distinct values of ratio $\alpha = R_L/R_o$ in Fig. 1*b*. If $\alpha = 0$, the static gain is the same as that of the ideal boost converter and is not affected by parasitic elements. If $R_L$ remains constant but $R_o$ decreases, with the consequent increase of the output power, the static gain tends to decrease over the entire range of the duty cycle for $\alpha \neq 0$ if compared with $\alpha = 0$. Analogously, if $R_L$ is increased but $R_o$ remains constant, the same behaviour as before is expected. The curves plotted in for $\alpha = 0.001$, $\alpha = 0.005$ and $\alpha = 0.01$ also show that the static gain drops after a given value of duty cycle. In practical terms, voltage conversion ratio is limited to a finite value when the duty cycle is very high.

The efficiency curves are plotted in Fig. 1*c* for several values of $\alpha$. Of course, the converter is lossless for $\alpha = 0$ and efficiency is 100% over the entire load range for any value of the duty cycle. However, efficiency drops significantly as the value of $R_L$ increases, what is more evident at high power levels. This is because of the increase of losses in $R_L$ with the square of the rms current through the inductor. Other issues related to the equivalent series resistance of the output capacitor, reverse-recovery losses and high $dv/dt$ and $di/dt$ rates associated with the rectifier diode will cause a significant reduction of overall efficiency. It is then reasonable to

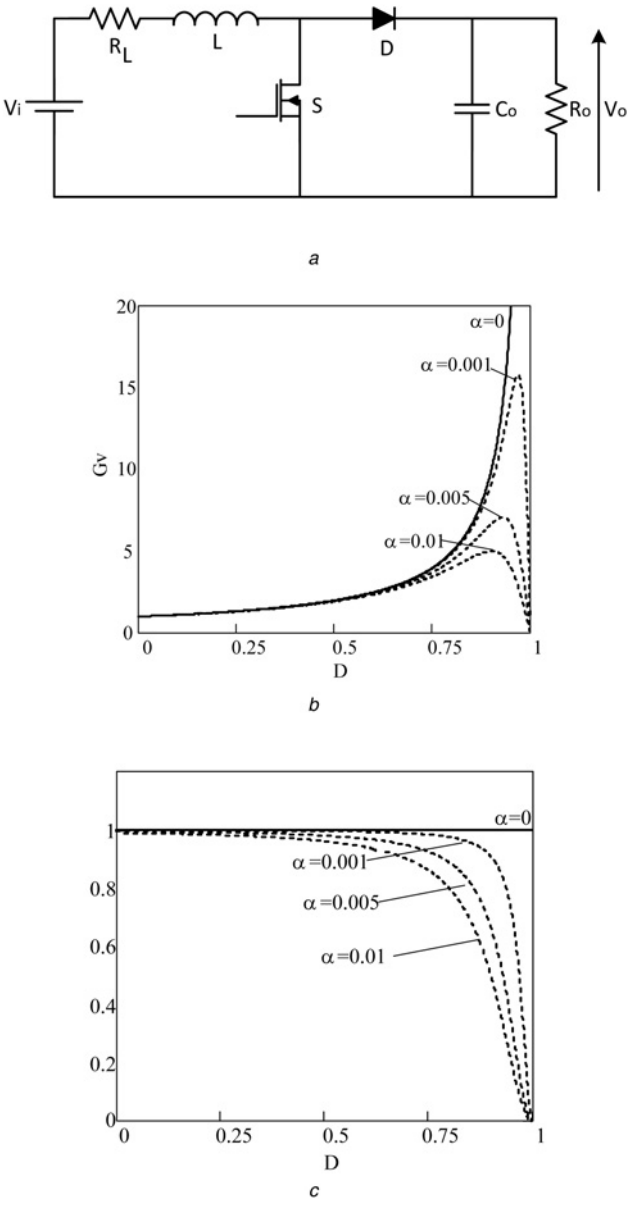


**Fig. 1** *Conventional dc–dc boost converter*

*a* Power stage
*b* Static gain as a function of the duty cycle
*c* Efficiency as a function of the duty cycle considering the influence of $R_L$

assume that the conventional boost converter is a simple and adequate approach for applications where very high-voltage step-up ratios are not necessary, being an approach recommended for low-to-medium power levels.

## 3 Classification of non-isolated dc–dc boost converters

On the basis of the conventional dc–dc boost converter shown in Fig. 1*a*, several step-up dc–dc topologies have been proposed in order to improve key issues, such as efficiency, voltage gain and power handling capacity. Some of the most important techniques typically step the voltage up without the need of extreme duty cycles and may use interleaving of multiple cells to increase the output power levels. A possible classification for dc–dc boost-type converters operating in CCM is then proposed according to Fig. 2, while this work is concerned with the discussion of several structures existent in the literature. The so-called topological variations of the conventional boost converter consist in the application of passive [21] and active snubber cells [22] to the hard-switching converter shown in Fig. 1*a* and will not be analysed here since there is no improvement regarding the static gain of the original structure [23].

### 3.1 Step-up converters without wide conversion ratio

*3.1.1 Conventional interleaved boost converters:* The conventional boost converter is not recommended for high-power, high-current applications because the output power is processed by only two semiconductors and losses become appreciable, especially those regarding the intrinsic resistance of the filter inductor. In this case, interleaving of several converters is very often employed to improve performance and reduce size of filter elements.

The operating frequency of the boost inductors becomes a multiple of the switching frequency according to the number of phases or cells, while the currents through the switches are just fractions of the input current. Besides, the size of the energy storage inductors and electromagnetic interference (EMI) filter can be reduced. A two-phase interleaved boost converter is shown in Fig. 3, where two inductors, two switches and two diodes share the input current [24].

Considering that a generic number of phases can be used, design flexibility results. For instance, when the ripple is already small, further reductions may not be interesting. Different tradeoffs can be made, for example, it is possible to reduce the switching frequency by a factor $N$ (to increase the conversion efficiency) and to reduce the inductance per cell by the same factor $N$ (reducing the converter size). The resulting system will present a per-cell ripple $N^2$ times larger than that of a single-cell converter, but the net interleaved ripple will remain the same. Therefore interleaving is recommended to increase the conversion efficiency and power density associated with the reduction of ripple current [24].

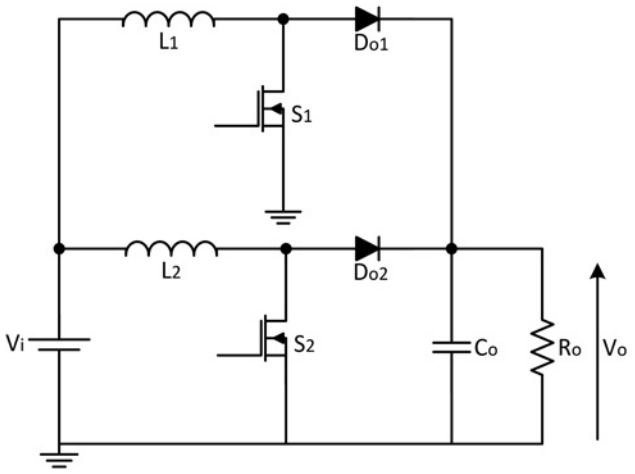


**Fig. 3** *Two-phase conventional interleaved boost converter [24]*

Being a modular approach, the output power can be increased as desired by using additional switches, inductors and diodes. However, cost can be prohibitive when there are many phases and robustness is compromised because of the significant component count, especially active switches. Besides, current sharing between the phases in Fig. 3 may be compromised because of the eventual inherent differences regarding the semiconductor elements and inductors, while the mismatch in duty cycle must be taken into account [25].

The voltage stress across the diodes and switches is equal to the output voltage, what does not make this topology adequate for high-output voltage applications. The reverse recovery of the boost diodes also limits the converter efficiency. Considering that the static gain is the same as that of the conventional boost converter, wide voltage conversion ratio cannot be achieved as well [26].

Multiple inductors can be integrated into a single magnetic core in order to reduce the very dimensions of the power circuit, also maintaining the remaining characteristics of the topology in Fig. 3. The reverse recovery of the output diode can be significantly alleviated because zero current switching occurs because of the leakage inductance of the coupled inductor [27]. Positive or negative coupling can be used for this purpose. The

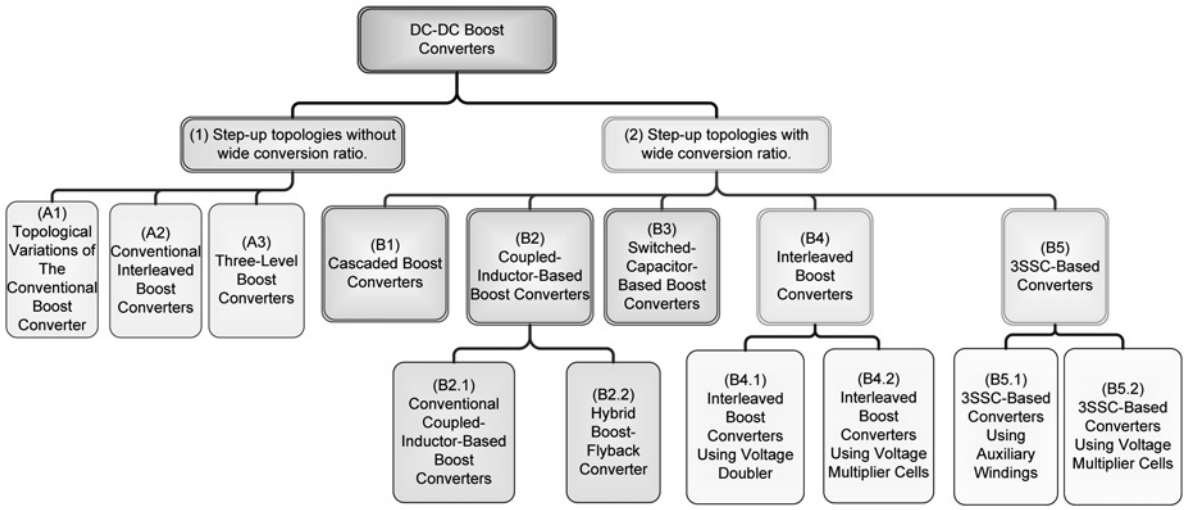


**Fig. 2** *Classification of non-isolated boost-based dc–dc converters*

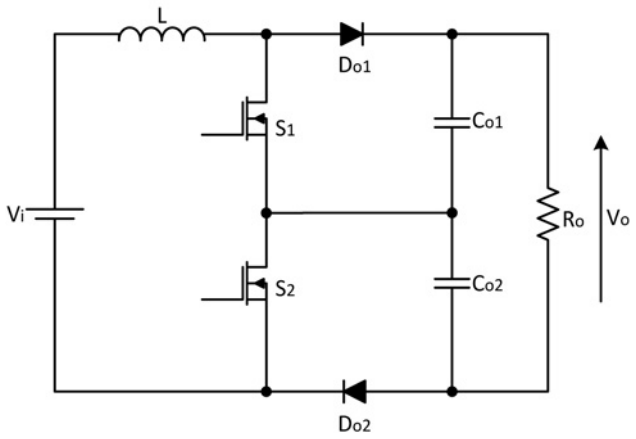


**Fig. 4** *Conventional three-level boost converter [28, 29]*

current ripple is small when positive coupling is used, although it is considerable when the negative coupling approach is adopted because the converter is supposed to operate in discontinuous current mode.

*3.1.2 Three-level boost converters:* The conventional three-level boost converter is shown in Fig. 4, where the voltage stress across all semiconductor elements is equal to half of the total output voltage. However, the static gain is the same as that of the conventional boost converter in Fig. 1*a*. This feature enables the use of metal–oxide–semiconductor field effect transistors with reduced drain-to-source on-resistance, with consequent increase of efficiency and reduction of conduction losses. Switching losses are reduced and EMI levels are minimised because of the reduced voltage across the semiconductors.

Another relevant issue is the dimension the input inductor. If the same voltage and power ratings are considered, and consequently for the same ripple current, the inductance is $L$ for the three-level boost converter, $2 \times 2L$ for the two-phase interleaved boost rectifier and $4L$ for the conventional boost converter.

However, the reverse-recovery phenomenon of the boost diodes is of major concern especially if the duty cycle of the main switches is high [28, 29]. Two sawtooth waves phase-displaced by 180° are necessary to generate the drive signals of the active switches, but isolated circuitry is necessary because they are not connected to the same reference node [30].

### 3.2 Step-up converters with wide conversion ratio

*3.2.1 Cascaded boost converters:* The conventional three-level boost converter is not adequate for applications that demand very high-voltage gain. Wide conversion ratio and reduced current ripple can be achieved if two or more conventional boost converters are cascaded, resulting in the topology shown in Fig. 5*a* [31]. The input voltage is typically low and can be stepped up by the first stage by using high duty cycle values. On the other hand, the second stage is able to operate with reduced duty cycle, thus allowing the minimisation of switching losses. However, robustness is compromised because of the need of multiple active switches, diodes, inductors and capacitors achieve very high-output voltages, while the control circuit must be carefully designed in this case [34]. A similar approach is applied to a dc–dc Ćuk converter in [35] to improve the static gain, but a large number of components and reduced efficiency are significant drawbacks.

This limitation can be partially overcome if switch $S_1$ in Fig. 5*a* is replaced by diode $D_2$ in Fig. 5*b* [12, 34], as this strategy can be applied to any number of cascaded stages to obtain a single-switch converter. Even though the ratio between the output voltage and the input voltage in Figs. 5*a* and *b* is equal to the product between the static gains of multiple conventional boost converters, some

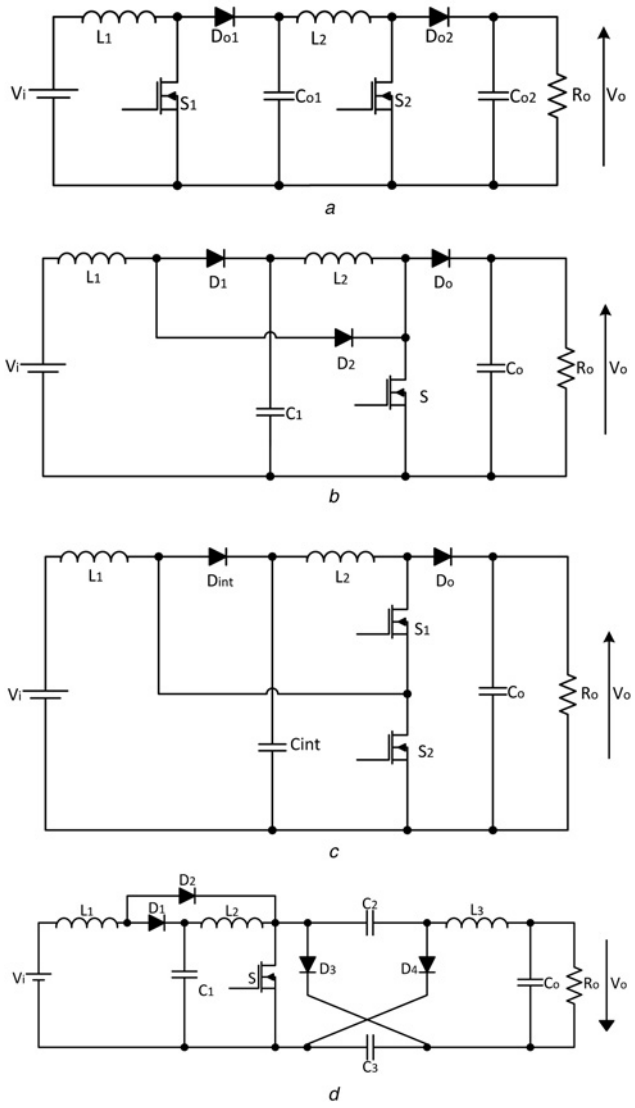


**Fig. 5** *Cascaded boost converters*

*a* Conventional cascaded boost converter [31]
*b* Single-switch quadratic boost converter [12]
*c* Quadratic three-level boost converter [32]
*d* Quadratic three-level boost converter using a CLD cell [33]

significant drawbacks still exist. Considering that many converters can be used, the global efficiency of the resulting structure is significantly reduced, which does not make the aforementioned topologies adequate for high-power applications [36]. In cases where the output voltage is very high, the voltage stresses across the main switch and the boost diode in the last stage are appreciable, that is, equal to the output voltage, thus leading to the use of costly components and poor efficiency. The reverse-recovery problem in such diode and also stability are also of major concern. Besides, increased complexity in terms of the control system is expected because the converters in Figs. 5*a* and *b* are fourth-order systems.

In order to achieve high-voltage gain, the quadratic three-level boost converter shown in Fig. 5*c* was proposed in [32], which aggregates some advantages regarding both converters in Figs. 4 and 5*b*. The converter employs two active switches whose respective voltage stresses are reduced, making it interesting in high-voltage applications. Efficiency is improved if compared with the conventional quadratic boost converter since conduction losses are minimised considering that the current flows through a reduced number of semiconductors simultaneously. However, the use of two inductors with distinct magnetic cores may limit the

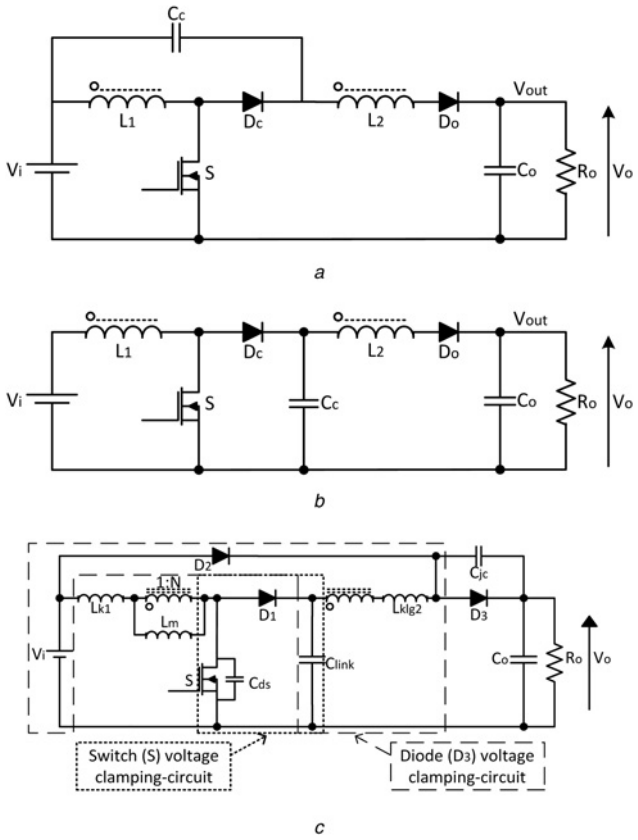


**Fig. 6** *Coupled-inductor-based boost converters*

*a* High-voltage gain boost converter with coupled inductors [40]
*b* High-voltage gain boost converter with coupled inductor and clamping circuit [41]
*c* High-voltage gain boost converter with coupled inductor and clamping circuit [42]

application of such converter to low power levels because size, weight and volume may be appreciable.

The static gain of the quadratic boost converter in Fig. 5*b* can be further increased by the addition of a capacitor–inductor–diode (CLD) cell consisting of one inductor, two diodes and two capacitors, resulting in the topology represented in Fig. 5*d* [33]. Besides, the voltage stress across the main switch is significantly reduced as the rated duty cycle increases. According to Fig. 5*d*, the output voltage has opposite polarity than the input voltage, but it does not represent a significant drawback. Even though it seems to be a good option to achieve high-output voltages, it may be restricted to low-power applications because of the appreciable conduction losses, considering that many semiconductors exist. Size, weight and volume are also of major concern considering that three inductors are used in this case.

### 3.2.2 Coupled-inductor-based boost converters

*(a) Conventional coupled inductor-based boost converters:* Coupled inductors are an alternative to increase the static gain in dc–dc converters [37]. The leakage inductance can be used to limit the diode current falling rate, thus minimising the diode reverse-recovery problem. Furthermore, the coupled inductor can be used as a transformer to avoid extreme duty cycles and to reduce the current ripple in high step-up conversion [38, 39].

Fig. 6*a* shows a high-voltage gain boost converter using coupled inductors, where the turns ratio between the windings can be properly adjusted [40]. Of course, the turns ratio allows extending the static gain as desired in this simple and straightforward approach, also keeping the duty cycle constant. However, the leakage inductance may lead to high-voltage spikes, which will increase the switch voltage stress resulting in serious EMI noise and reducing efficiency. The input current is also pulsating in this case.

A modified version of the aforementioned topology is proposed in [41] and shown in Fig. 6*b*, where a clamping circuit is used to reduce the voltage stress across the main switch because of the leakage inductance of the coupled inductor. A low cost, robust and simple solution is then obtained. The maximum voltage across the active switch becomes then equal to the sum of the input voltage and the voltage across $L_1$. Besides, the maximum voltage across diode $D_o$ is very high, thus leading to the use of high-cost semiconductors that inherently present high forward voltage drop and also low switching speed. This is an approach recommended to low-input voltages and high-voltage step-up since efficiency is typically low because of the voltage ringing, while EMI levels are appreciable because of the pulsating input current [41].

A quite similar topology to the one shown in Fig. 6*b* is presented in Fig. 6*c*, where only one additional diode is used. Conversion ratio can be extended by increasing either the duty cycle or the turns ratio of the coupled inductor considering proper design tradeoffs. The active clamping circuit is able to maintain the voltages across the main switch and the output diode equal to the link capacitor voltage and output voltage, respectively [42]. In this case, voltage ringing does not affect the maximum voltage stresses regarding the semiconductor elements and efficiency is significantly improved if compared with the converter shown in Fig. 6*a*. However, it is not recommended for high-power applications because of the appreciable current stress through the switch.

*(b) Hybrid boost–flyback converters:* The conventional flyback converter using a coupled inductor is able to provide very high-voltage gain, but efficiency is poor because of the leakage inductance, thus restricting its application to very low power levels. The output sides of both flyback and boost converters can be connected so that high-voltage gain is obtained. In this case, the boost converter behaves as a clamping circuit when the active switch is turned off [43]. Fig. 7*a* shows a hybrid boost–flyback converter where the voltage stress across the switch is reduced, that is, less than half of the output voltage, which depends on the turns ratio of the coupled inductor. It is a fairly simple solution where few semiconductors and passive elements are used. The voltage across the switch is naturally clamped by the output capacitor, which recycles the leakage energy. The voltage stress across the output diode is also reduced, alleviating the reverse-recovery problem. However, the input current is pulsating in this case, thus demanding the use of an additional input filter to reduce EMI levels.

Other strategies can be used to integrate the boost and flyback converters [45–47]. Fig. 7*b* shows a boost–flyback converter using a voltage multiplier cell (VMC) in a modular approach [44]. This is an interesting option that allows good tradeoffs between the number of VMCs and the turns ratio of the coupled inductor, while design flexibility exists [48]. The voltage stress across the active switch is less than the output voltage, that is, the voltage across capacitor $C_{o1}$. Besides, it does not depend on the turns ratio or the number of VMCs, making this topology adequate to low-input voltage ratings and high-voltage step-up. The main concern of the high-step-up flyback–boost converters lies in the voltage balance across the output capacitors, which must be considered because of the series connection of the output capacitors.

*3.2.3 Switched-capacitor-based boost converters:* Capacitors can be integrated with dc–dc converters by using a switched approach that allows increasing the voltage gain. Switched capacitors can be also associated with coupled inductors in order to further increase the static gain of dc–dc converters by adjusting the turns ratio as in [49]. Switched-capacitor–inductor approaches also allow obtaining very large step-up, but at the cost of high component count [50, 51].

A switched-capacitor-based converter is proposed in [52] and shown in Fig. 8*a*, where high-voltage step-up can be achieved by

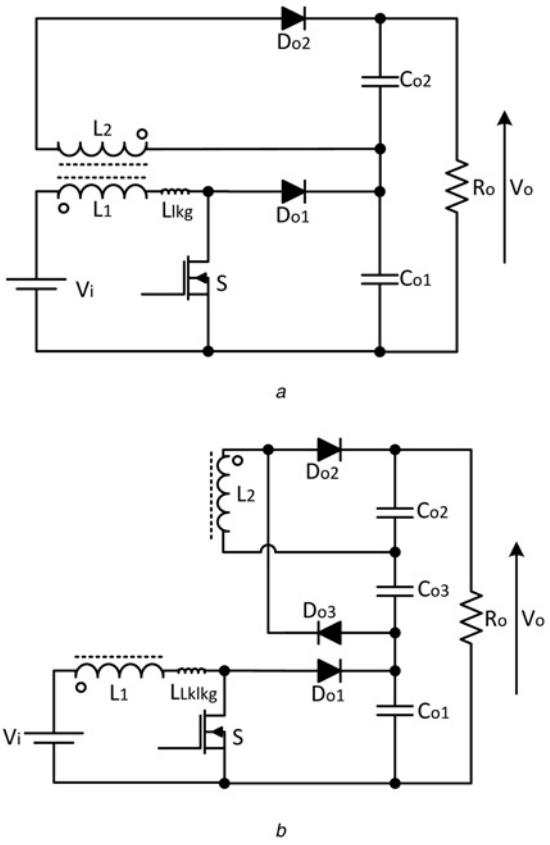


**Fig. 7** *Hybrid boost-flyback converters*

*a* Simple hybrid boost-flyback converter [43]
*b* Hybrid boost-flyback converter using VMCs [44]

properly increasing the number of capacitors. Since the converter operates with typical low-duty cycle, the reverse-recovery issue of the output diode is alleviated. The capacitors behave as voltage sources connected in series, as the current flows through all of them. Their respective equivalent series resistances must be properly minimised by the parallel association of individual components to achieve a given capacitance because they can compromise efficiency. Drive circuitry also becomes more complex as more switches are added, which are not connected to the same reference node. It is also worth to mention that the voltage stresses across they are not the same, leading to the specification of active switches with multiple ratings.

A switched-capacitor boost converter is proposed in [53] and shown in Fig. 8*b*, where the voltage gain is twice that of the conventional boost converter, with reduced voltage stress across the main switch and self-voltage balancing across the output capacitors. The voltage gain can be further extended in a modular approach, but it is not adequate for high-power, high-current levels since the input inductor becomes somewhat large and the current stress through the switch is appreciable.

An improved version of such topology called switched-capacitor-based active-network converter (SC-ANC) is introduced in [54] and represented in Fig. 8*c*. Reduced voltage ratings regarding the semiconductor are achieved, while the self-voltage balancing across the output capacitors is also maintained in this case. Besides, the static gain is increased if compared to the topology in Fig. 8*b*. However, additional components, that is, one inductor and one active switch are used in this topology, while drive circuitry becomes more complex since the switches are not connected to the same reference node.

A high-voltage step-up converter is presented in [55] and shown in Fig. 9*a*, where a basic cell composed by two capacitors, two diodes and one active switch is incorporated to a boost topology. This

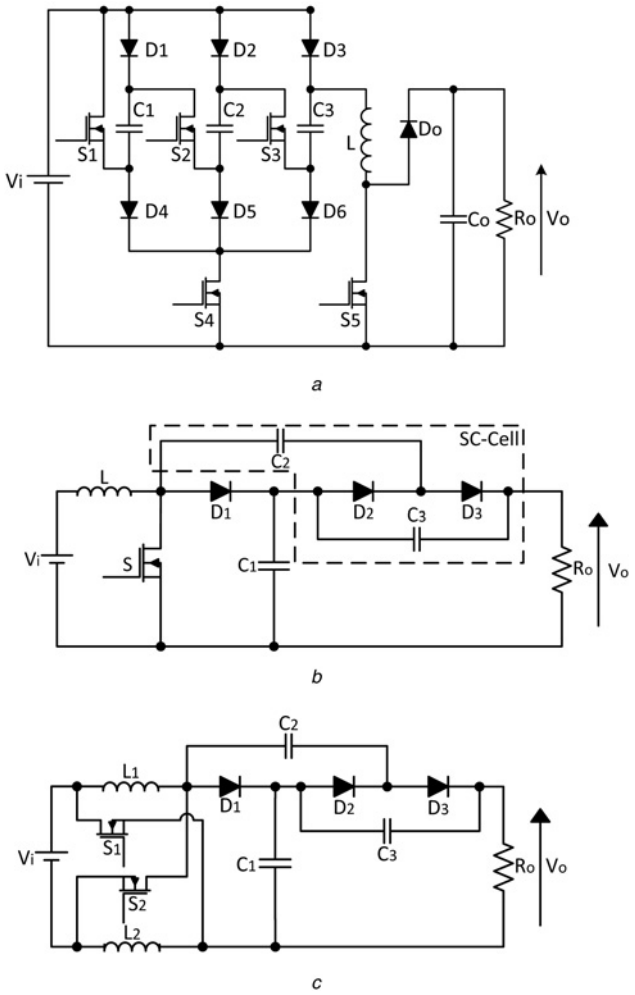


**Fig. 8** *Switched-capacitor-based boost converters*

*a* High-voltage gain boost converter based on switched capacitors [52]
*b* Switched-capacitor-based boost converter [53]
*c* SC-ANC [54]

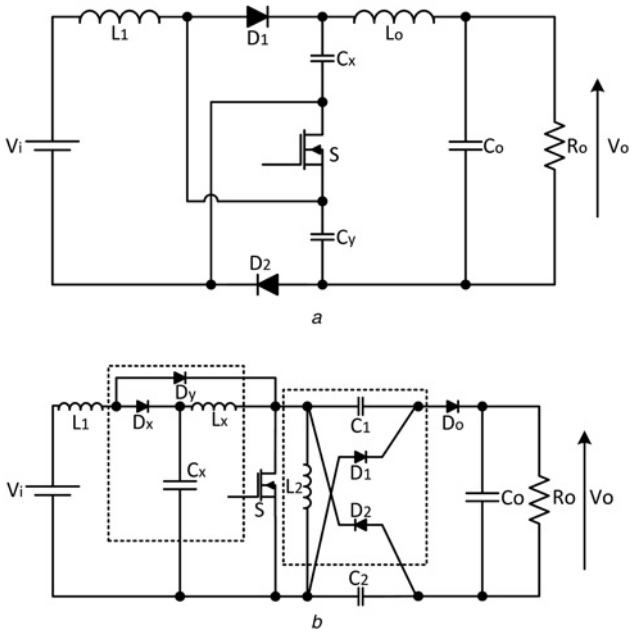


**Fig. 9** *Switched-capacitor-based boost converters*

*a* Switched-capacitor-based boost converter proposed in [55]
*b* Switched-capacitor-based boost converter proposed in [56]

arrangement is similar to a single-switch quadratic boost converter, but three capacitors and two diodes are used instead, while the static gain is not the same in both structures. However, the voltage stress across the switch is reduced if compared to conventional cascaded converters. Efficiency is also claimed to be same as that of the conventional boost converter [55], while this topology is not recommended to high power levels. A similar version of such dc–dc converter is employed in [57] to supply a cascaded two-level dc–ac converter with high-dc voltage and obtain a five-level inverter.

Another switched-capacitor cell is proposed in [56] for the generation of a family of high-voltage conversion ratio dc–dc converters. A boost converter is shown in Fig. 9*b*, where higher output voltages at low-duty cycle values associated with reduced voltage stress across the semiconductor devices are prominent advantages. However, this topology requires the use of numerous components that include two inductors per cell, with consequent increase of size, weight and volume associated to poor efficiency at high power levels.

### 3.2.4 High-voltage gain interleaved boost converters:

*(a) Interleaved boost converters using voltage doubler:* As it was mentioned before, single-switch boost-type converters are not adequate for high-power, high-current applications, while interleaved converters represent a better choice in this case [58, 59]. The circuit proposed in [60] and shown in Fig. 10*a* uses an autotransformer with unity turns ratio, so that the current is equally shared between the switches. The output stage uses a voltage doubler to increase the static gain. The input current is continuous and its respective ripple is reduced. The voltage across the active switches is less or equal to half of the output voltage. Besides, isolated driver circuitry is not necessary. The main drawback of such converter lies in the presence of the auxiliary transformer and also one inductor per phase of the interleaved converter, while increased cost and dimensions result.

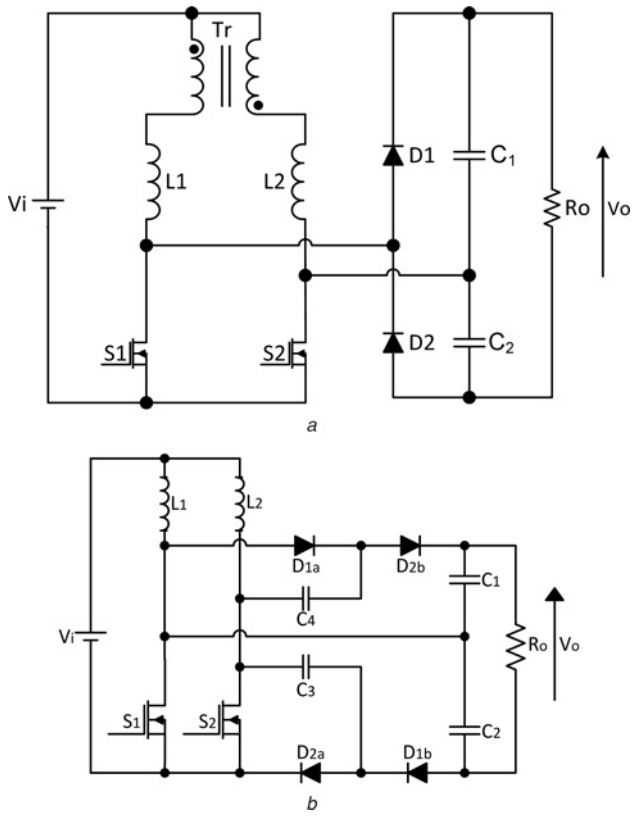


**Fig. 10** *High-voltage gain interleaved boost converters*

*a* Two-phase interleaved boost converter using voltage doubler [60]
*b* Two-phase quadrupler interleaved boost converter [61]

A quadrupler interleaved boost converter is presented in [61] and shown in Fig. 10*b*. The static gain is the same as that obtained for the topology in Fig. 10*a*, but the voltage stress across the main switches becomes one-fourth of the total output voltage. The automatic current sharing capability can be obtained without using an auxiliary transformer, but two diodes and two capacitors are added in this topology.

*(b) Interleaved boost converters using VMCs:* Fig. 11*a* shows an interleaved boost topology using VMCs [62]. Operation at high power levels, reduction of magnetic elements, reduction of current ripple and improved transient response are prominent advantages. Both inductors can also be integrated into a single core so that the very dimensions of the converter are reduced [64]. The approach can be extended to any number of VMCs [65, 66], while the static gain can be further increased. The voltage stress regarding the active switches is also minimised in this case. Since the reverse-recovery currents through the output diode and multiplier

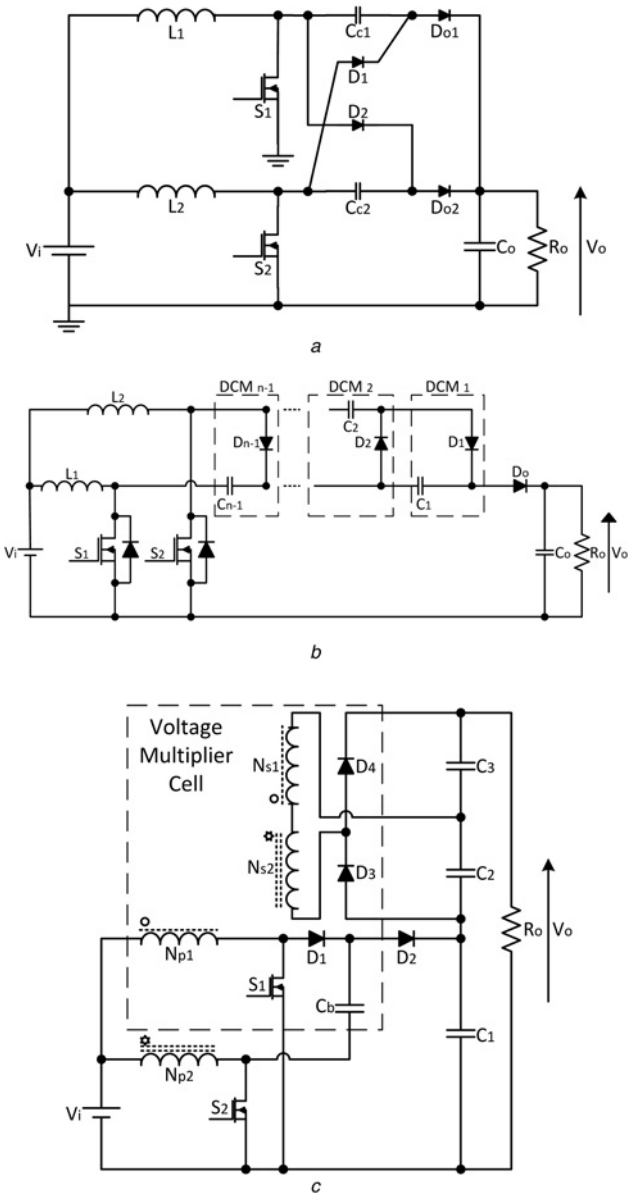


**Fig. 11** *Interleaved boost converters using VMCs*

*a* High-voltage gain two-phase interleaved boost converter using one VMC [62]
*b* High-voltage gain two-phase interleaved boost converter using DCMCs [63]
*c* High-voltage gain two-phase interleaved boost converter using VMCs and coupled inductors [20]

diodes are summed, efficiency can be compromised, while the use of a non-dissipative snubber is necessary as in [62].

An interleaved boost converter based on diode–capacitor multiplier cells (DCMCs) is shown in Fig. 11*b* [63]. It represents a very simple technique that allows increasing the static gain of the conventional interleaved boost converter by using cells with only two components. The voltage stress across the switches is proportionally reduced as more cells are added. However, the cascade connection of several cells leads to reduced efficiency especially at high power levels because of the appreciable conduction losses in the multiplier diodes.

The static gain can be increased without the addition of many VMCs if coupled inductors are used, resulting in the converter represented in Fig. 11*c* [20]. Good tradeoffs can be made between the turns ratio of the inductor and number of VMCs to provide high efficiency [20]. Care must be taken when setting the primary leakage inductances of the coupled inductors, which must be nearly the same to achieve good current sharing [20].

An interleaved boost converter using two coupled inductors and VMCs to achieve high-voltage step-up is presented in Fig. 12*a* [67]. This arrangement is adequate for low-input voltages and high-current levels considering that the voltage stress regarding the active switch depends on the input voltage directly, but is not reduced as the chosen turns ratio increases [67]. The main drawback is the duty cycle limitation, which must be higher than 50%. Besides, a soft-start scheme is necessary to provide initial charge to the output capacitors.

A modular approach for high-voltage step-up, high-power applications is proposed in Fig. 12*b* [68], which allows adjusting the voltage conversion ratio as desired. It is composed by the combination of one forward converter and one boost converter connected to each phase. The converter is able to operate over the entire range of the duty cycle, but higher voltage gains are obtained for $D > 0.5$. Owing to the association of the aforementioned topologies, higher number of components is necessary.

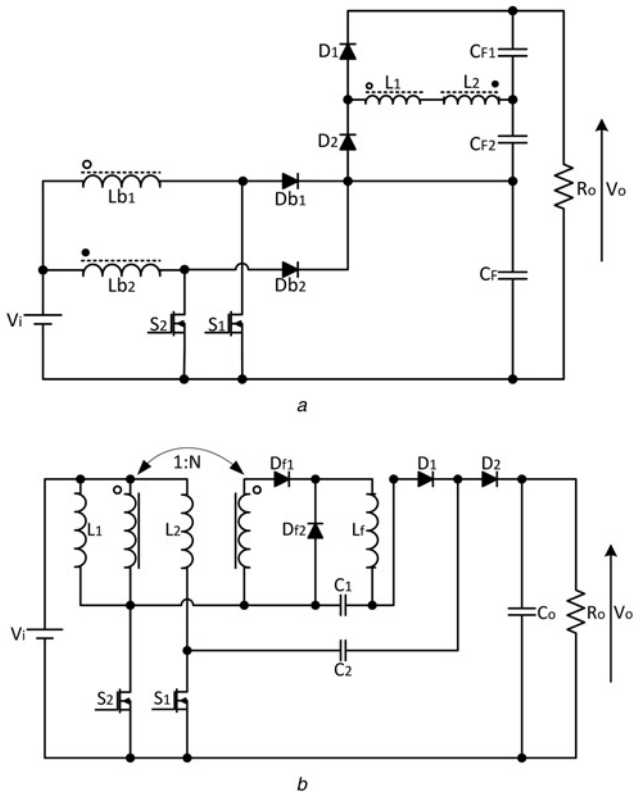


**Fig. 12** *Interleaved boost converters using VMCs*

*a* High-voltage gain two-phase interleaved boost converter using VMCs and coupled inductors [67]
*b* High-voltage gain two-phase interleaved boost converter using coupled inductors and VMCs [68]

*3.2.5 3SSC-based converters:* The 3SSC was initially proposed in [69], thus leading to the proposal of numerous dc–dc and ac–dc converter topologies over the last 12 years. A family of non-isolated dc–dc topologies was also introduced in [69], where basic buck, boost, buck–boost, Ćuk, SEPIC and zeta converters for high-current applications are described. However, the static gains of the aforementioned converters based on the so-called cell B are the same as those of the classical dc–dc structures, what does not make them adequate for wide voltage conversion ratios [70].

The 3SSC is often mistaken by the interleaving technique, but it is also recommended for high-power applications. Even though they are similar approaches, general advantages can be addressed to 3SSC-based converters [71]:

- magnetic components, that is, the autotransformer and inductor are designed for twice the switching frequency, with consequent reduction of size, weight and volume;
- good current sharing is obtained by using an autotransformer with unity turns ratio;
- reduced current stress through the active switches;
- losses are distributed among the semiconductors, with better heat distribution and more efficient use of heat sinks;
- part of the input power is directly transferred to the load (output) through the diodes, mainly when duty cycle is lower than 0.5. As a consequence, conduction and switching losses in the active switches are reduced.

For high-voltage step-up, there are basically two strategies that can be used in boost-type structures: VMCs and auxiliary windings coupled to the autotransformer. Both approaches are described as follows.

*(a) 3SSC-based boost converters using VMCs:* Analogously to the interleaved converter proposed in [65, 66], VMCs can be added to the 3SSC-based boost converter in order to provide high-voltage step-up. The topology shown in Fig. 13*a* uses VMCs composed of two capacitors and two diodes [72]. Unlike the interleaved boost converter shown in Fig. 3, current sharing is not of major concern because of the autotransformer, which keeps the current through the switches satisfactorily balanced. High efficiency is obtained for a wide load range, although it can be compromised if many multiplier cells are used to increase the static gain because of conduction losses in the additional diodes. Besides, this converter is not able to operate with low values of duty cycle i.e. $D < 0.5$ [72].

A similar generic approach based on VMCs and the 3SSC is introduced in Fig. 13*b* [73], where a family of converters for high-power, high-current applications are derived. A 3SSC-based boost converter using three VMCs is implemented and evaluated, where high efficiency is obtained over the entire load range. A similar version of the converter with two VMCs is studied in [74], where it can be seen that efficiency is improved because less multiplier diodes are used, with consequent reduction of conduction losses. In both cases, efficiency is high since the active switches are turned on under soft switching condition without the aid of auxiliary circuits. The main advantage of the converter in Fig. 13*b* if compared with the topology in is the ability to operate over the entire range of the duty cycle. The voltage stress across the main switches is proportionally reduced by increasing the number of VMCs. Once again, tradeoffs must be made between conduction losses in the multiplier diodes and wide conversion ratio.

*(b) 3SSC-based boost converters using auxiliary windings:* Auxiliary windings can be coupled to the magnetic core of the

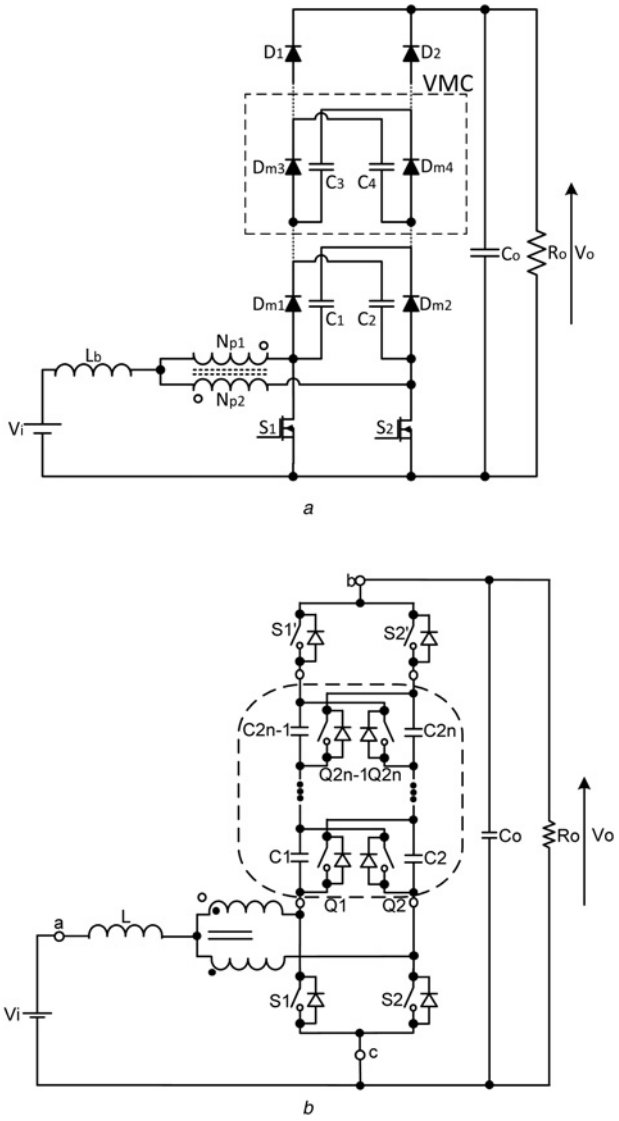


**Fig. 13** *3SSC-based boost converters using VMCs*

*a* Generic 3SSC-based boost converter with VMCs [72]
*b* Modified 3SSC-based boost converter using VMCs [73, 74]

autotransformer that is part of the 3SSC to provide high-voltage step-up [75–77]. A boost-type dc–dc converter is presented in Fig. 14*a*, where one auxiliary winding is used [75]. The static gain can be adjusted according to the turns ratio between the 1:1 autotransformer and the auxiliary (or secondary) winding without compromising the voltage stress across the switches. This concept can be extended to any number of windings, where the output voltage can be increased not only adjusting the aforementioned turns ratio, but also by adding more auxiliary windings [76, 77]. The input current is non-pulsating and presents reduced ripple. Unfortunately, size, weight and volume are somewhat higher than similar approaches in [72–74] considering the same design specifications. Once again, the converter operation is not adequate when $D < 0.5$ because the voltage induced in the secondary winding is low.

An improved version of the converter is shown in [78] and Fig. 14*b*, which is able to operate over the entire range of the duty cycle and is recommended to supply half-bridge inverters. Balanced voltages across the output capacitors that constitute the dc links are obtained because of the use of 3SSC. Once again, design flexibility exists in the adjustment of the static gain. The voltage stress across the active switches can be reduced as the

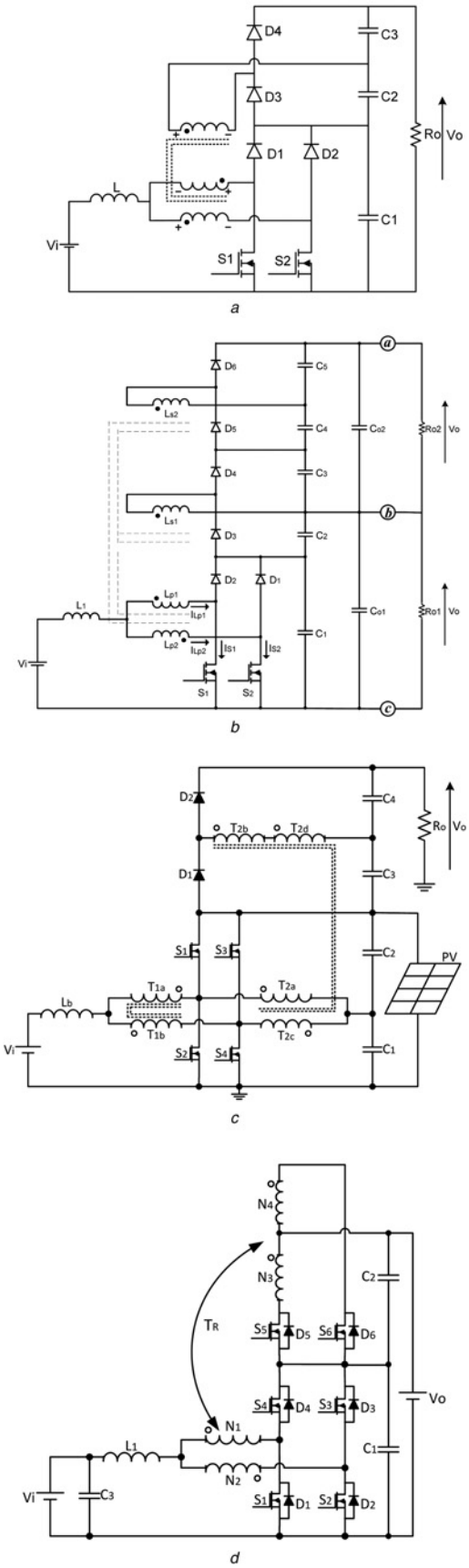


**Fig. 14** *3SSC-based boost converters using auxiliary windings*

*a* 3SSC-based boost converter using auxiliary windings [75–77]
*b* 3SSC-based boost converter using auxiliary windings [78]
*c* 3SSC-based bidirectional boost converter [79]
*d* 3SSC-based bidirectional boost converter [80]

turns ratio and/or number of auxiliary windings are increased, with consequent improvement of the static gain, but at the cost of increased size, weight and volume.

A three-port bidirectional topology is presented in [79] and Fig. 14*c*. Energy flow among distinct energy sources, for example, a battery bank and a PV module can be controlled in a single-stage arrangement, thus demonstrating that high-voltage gain 3SSC-based converters are adequate for renewable energy applications. In this case, the output voltage can be increased by adjusting the duty cycle or the turns ratio of the coupled inductors. The transformer is designed to process about 70% of the total rated power. It is also shown that higher voltage gains are obtained when $D > 0.5$. Unfortunately, the topology employs many magnetic elements with distinct cores, as dimensions may become appreciable.

Another bidirectional topology based on the 3SSC is shown in Fig. 14*d* [80], which is able to operate in either boost mode or buck mode. The output voltage can be stepped up according to the transformer turns ratio. As drawbacks, the converter is not able to operate appropriately if $D < 0.5$ analogously to the converter presented in Fig. 14, and six active switches are necessary, whose drive circuitry becomes quite complex. The leakage inductance of the transformer may also affect the voltage stress across the switches because of appreciable spikes, while efficiency is somewhat low.

### 3.3 Comparison among several step-up converters

The last two sections were dedicated to the analysis of several boost-based dc–dc converters existing in the literature. It is important to compare them adequately so that it is possible to identify eventual advantages and disadvantages in potential applications.

In order to simplify the analysis, the converters are separated into four groups. The first one aggregates topologies A1, A2, A3 and B1 according to the classification given in Fig. 2, which includes:

(1) Conventional boost converter (Fig. 1*a*);
(2) *N*-phase interleaved boost converter (Fig. 3) without coupling among the inductors [24] ($N > 1$);
(3) Three-level boost converter (Fig. 4) [28, 29];
(4) *N*-stage cascaded boost converters (Figs. 5*a* and *b*) [12, 31] ($N > 1$);
(5) Quadratic three-level boost converter (Fig. 5*c*) [32];
(6) Quadratic three-level boost converter using a CLD cell (Fig. 5*d*) [33].

The second group includes topologies B2 and B3, that is,

(7) High-voltage gain boost converter using coupled inductors with turns ratio *n* (Fig. 6*b*) [41];
(8) Hybrid boost–flyback converter with turns ratio *n* (Fig. 7*a*) [43];
(9) Hybrid boost–flyback converter using a given number of VMCs and turns ratio *n* (Fig. 7*b*) [44];
(10) High-voltage gain boost converter using *n* switched capacitor cells (Fig. 8*a*) [52];
(11) Switched-capacitor-based boost converter with *n* switched capacitors (Fig. 8*b*) [53];
(12) SC-ANC (Fig. 8*c*) [54];
(13) Switched-capacitor-based boost converter (Fig. 9*a*) [55].

The third group includes topology B4, that is,

(14) Two-phase interleaved boost converter using voltage doubler (Fig. 10*a*) [60];
(15) Quadrupler two-phase interleaved boost converter (Fig. 10*b*) [61];
(16) High-voltage gain two-phase interleaved boost converter using VMCs (Fig. 11*a*) [62];
(17) High-voltage gain two-phase interleaved boost converter using DCMCs (Fig. 11*b*) [63];
(18) High-voltage gain two-phase interleaved boost converter using VMCs and coupled inductors with turns ratio *n* (Fig. 11*c*) [20];
(19) High-voltage gain two-phase interleaved boost converter using VMCs and coupled inductors with turns ratio *n* (Fig. 12*a*) [67];
(20) High-voltage gain two-phase interleaved boost converter using VMCs and coupled inductors with turns ratio *n* (Fig. 12*b*) [68].

The fourth group includes topology B5, that is,

(21) 3SSC-based boost converter using VMCs (Fig. 13*a*) [72];
(22) 3SSC-based boost converter using VMCs (Fig. 13*b*) [73, 74];
(23) 3SSC-based boost converter using auxiliary windings with turns ratio *a* (Fig. 14*a*) [75–77];
(24) 3SSC-based boost converter using several auxiliary windings *j* with turns ratio $a_j$ (Fig. 14*b*) [78];
(25) 3SSC-based bidirectional converter with turns ratio *n* (Fig. 14*c*) [79];
(26) 3SSC-based bidirectional boost converter with turns ratio *n* (Fig. 14*d*) [80].

Tables 1–4 compare the aforementioned topologies, while their respective static gain curves are plotted in Fig. 15. In order to establish a proper comparison among the structures, the turns ratio of coupled inductors, number of VMCs and DMCMs, and number of auxiliary windings is considered unity in Fig. 15. The curves show that topologies (6) and (13) present the widest conversion ratios for low values of the duty cycle. However, Table 1 shows that (6) is not adequate to achieve high-output voltages because of the appreciable voltage stress across the switch. Besides, Table 2 evidences that (13) is not recommended when the input voltage is high. Of course, the choice of a proper topology for a given voltage step-up application depends on several other aspects than the static gain.

Table 3 and Fig. 15*c* show that interleaved boost converters represent good solutions to achieve high-voltage step-up in high-power applications, especially if coupled inductors are used. However, current sharing schemes may be necessary, while the

**Table 1** Comparison among topologies A1, A2, A3 and B1

| Characteristic | Topologies | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| voltage stress across the switch(es) | $V_o$ | $V_o$ | $(V_o/2)$ | $V_o$ | $V_o \cdot (1-D)$<br>$V_o - V_o \cdot (1-D)$ | $(V_o/1+D)$ |
| static gain | $(1/1-D)$ | $(1/1-D)$ | $(2/1-D)$ | $(1/1-D)^N$ | $(1/1-D)^2$ | $((1+D)/(1-D))^2$ |
| number of switches | 1 | $N$ | 2 | $N$, $N>1$ | 1 | 1 |
| duty cycle range | $0<D<1$ | $0<D<1$ | $0<D<1$ | $0<D<1$ | $0<D<1$ | $0<D<1$ |
| number of diodes | 1 | $N$ | 2 | $N$ | 3 | 4 |
| number of capacitors | 1 | 1 | 2 | $N$ | 1 | 4 |
| operating frequency of magnetics | $f_s$ | $N \times f_s$ | $f_s$ | $f_s$ | $f_s$ | $f_s$ |
| number of inductors | 1 | $N$ | 1 | $N$ | 2 | 3 |
| auxiliary transformers | — | — | — | — | — | — |
| number of inductor cores | 1 | 1 or $N$ | 1 | $N$ | 2 | 3 |
| modularity | no | yes | no | yes | no | no |

**Table 2** Comparison among topologies B2 and B3

| Characteristic | Topologies | | | | | | |
|---|---|---|---|---|---|---|---|
| | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
| voltage stress across the switch(es) | $(V_o/(1+n-D))$ | $(V_o/(1+D{\cdot}n))$ | $(V_o/(1+\text{VMC}{\cdot}n))$ | — | $(V_o/n)$ | $(2{\cdot}V_o/3+D)$ | $(V_o/1+D)$ |
| static gain | $((n+1-D)/1-D)$ | $((1+n{\cdot}D)/1-D)$ | $((1+\text{VMC}{\cdot}n)/1-D)$ | $(((n+1)-n{\cdot}D)/1-D)$ | $(N/1-D)$ | $(3+D/1-D)$ | $(1+D/1-D)$ |
| number of switches | 1 | 1 | 1 | $N+2$ | 1 | 2 | 1 |
| duty cycle range | $0<D<1$ | $0<D<1$ | $0<D<1$ | $0<D<1$ | $0<n<1$ | $0<D<1$ | $0<D<1$ |
| number of diodes | 2 | 2 | 3 | $2{\cdot}n+1$ | $2{\cdot}N+1$ | $2{\cdot}n+1$ | 2 |
| number of capacitors | 2 | 2 | 2 | $n+1$ | $2{\cdot}N+1$ | $2{\cdot}n+1$ | 3 |
| operating frequency of magnetics | $f_s$ | $f_s$ | $f_s$ | $f_s$ | $f_s$ | $f_s$ | $f_s$ |
| number of inductors | 2 | 2 | 2 | 1 | 1 | 2 | 2 |
| auxiliary transformers | — | — | — | — | — | — | — |
| number of inductor cores | 1 | 1 | 1 | 1 | 1 | 2 | 2 |
| modularity | no | no | no | yes | yes | no | no |

**Table 3** Comparison among topology B4

| Characteristic | Topologies | | | | | | |
|---|---|---|---|---|---|---|---|
| | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
| voltage stress across the switch(es) | $(V_o/2)$ | $(V_o/4)$ | $(V_o/\text{VMC}+1)$ | $(V_o/\text{DCMC})$ | $(V_o-((2{\cdot}n+1)/1-D){\cdot}V_i)$ | $(V_o/(2{\cdot}n{\cdot}\text{VMC}+1))$ | $(V_o/(2+n{\cdot}D{\cdot}(1-D)))$ |
| static gain | $(4/1-D)$ | $(4/1-D)$ | $((\text{VMC}+1)/1-D)$ | $((\text{DCMC}+1)/1-D)$ | $((2{\cdot}n+2)/1-D)$ | $((2{\cdot}n{\cdot}\text{VMC}+1)/1-D)$ | $(2/1-D)+n{\cdot}D$ |
| number of switches | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| duty cycle range | $0<D<1$ | $0<D<1$ | $0<D<1$ | $0<D<1$ | $0<D<1$ | $0.5<D<1$ | $0<D<1$ |
| number of diodes | 2 | 4 | $2{\cdot}\text{VMC}+2$ | $\text{VMC}+1$ | 4 | $2{\cdot}\text{VMC}+2$ | $2{\cdot}\text{VMC}+2$ |
| number of capacitors | 2 | 4 | $2{\cdot}\text{VMC}+1$ | $\text{VMC}+1$ | 4 | $2{\cdot}\text{VMC}+1$ | $\text{VMC}+2$ |
| operating frequency of magnetics | $f_s/2$ | $f_s/2$ | $f_s/2$ | $f_s/2$ | $f_s/2$ | $f_s/2$ | $f_s/2$ |
| number of inductors | 2 | 2 | 2 | 2 | 2 | 2 | 4 |
| auxiliary transformers | 01 (02 windings) | — | — | — | — | — | — |
| number of inductor cores | 2 | 2 | 2 | 2 | 2 | 2 | 4 |
| modularity | no | no | yes | yes | no | yes | yes |

**Table 4** Comparison among topology B5

| Characteristic | Topologies | | | | | |
|---|---|---|---|---|---|---|
| | 21 | 22 | 23 | 24 | 25 | 26 |
| voltage stress across the switch(es) | $(V_o/\text{VMC}+1)$ | $(V_o/(2{\cdot}\text{VMC}^{0.3}))$ | $(V_o/a+1)$ | $\dfrac{V_o}{\left(1+\sum_{j=1}^{n}a_j\right)}$ | — | — |
| static gain | $((\text{VMC}+1)/1-D)$ | $((\text{VMC}+1)/1-D)$ | $(a+1/1-D)$ | $\dfrac{1}{1-D}\cdot\left(1+\sum_{j=1}^{n}a_j\right)$ | $\dfrac{1}{1-D}+\dfrac{2\cdot n}{1-D+\alpha}(D<0.5)$ $\left(\dfrac{1}{1-D}\right)\cdot\left[\dfrac{2\cdot n\cdot D^2}{D^2+\alpha\cdot(1-D)}+1\right](D>0.5)$ where $\alpha=((4{\cdot}n{\cdot}I_o{\cdot}L_s)/(V_i{\cdot}T_s))$ is the normalised load current | $((2+n)/(2{\cdot}(1-D)))$ (boost mode) |
| number of switches | 2 | 2 | 2 | 2 | 4 | 6 |
| duty cycle range | $0.5<D<1$ | $0<D<1$ | $0.5<D<1$ | $0<D<1$ | $0<D<1$ | $0.5<D<1$ |
| number of diodes | $2{\cdot}\text{VMC}+2$ | $2{\cdot}\text{VMC}+2$ | $2{\cdot}a+2$ | $2{\cdot}a+2$ | 2 | 6 |
| number of capacitors | $2{\cdot}\text{VMC}+1$ | $2{\cdot}\text{VMC}+1$ | $2{\cdot}a+1$ | $2{\cdot}a+1$ | 4 | 3 |
| operating frequency of magnetics | $f_s/2$ | $f_s/2$ | $f_s/2$ | $f_s/2$ | $f_s/2$ | $f_s/2$ |
| number of inductors | 1 | 1 | 1 | 1 | 1 | 1 |
| auxiliary transformers | 01 (02 windings) | 01 (02 windings) | 01 ($02+a$ windings) | 01 ($02+a$ windings) | 02 (06 windings) | 01 (04 windings) |
| number of inductor cores | 1 | 1 | 1 | 1 | 1 | 1 |
| modularity | yes | yes | yes | yes | no | no |



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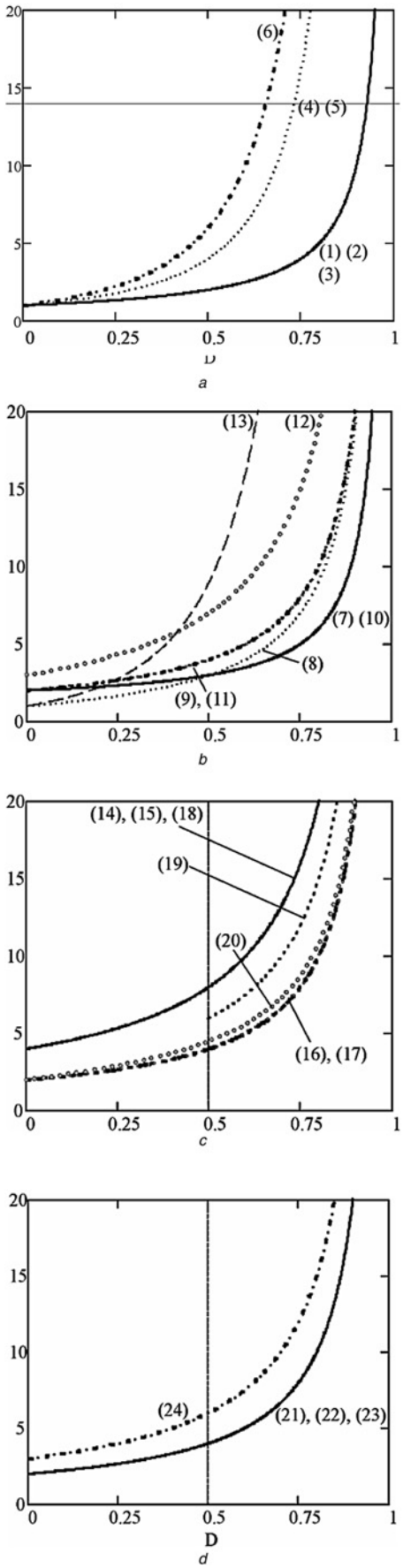


**Fig. 15** *Static gain of non-isolated boost-based dc–dc converters*

*a* A1, A2, A3 and B1
*b* B2 and B3
*c* B4
*d* B5

leakage inductance of the coupled inductor must be also taken into account.

As it was mentioned before, all 3SSC-based converters do not present current sharing issues because of the use of an autotransformer with unity turns ratio, as they can achieve high-voltage gain by using modular approaches, for example, VMCs and auxiliary windings coupled to the autotransformer. It is worth to mention that tradeoffs must be made between number of components and the conversion ratio in this case. According to Table 4, some derived topologies can only operate properly when the duty cycle is higher than 0.5, which is a possible drawback.

## 4 Conclusion

The literature presents numerous topologies where the output voltage can only be stepped up by increasing the duty cycle. However, the operation with high duty cycle values leads to poor performance in terms of increased losses, reduced efficiency and the need of high cost and accurate drive circuitry. Within this context, this paper has presented an extensive review on non-isolated boost-based dc–dc converter topologies.

It has been shown that the conventional boost converter is typically limited to low-power applications because the output power is processed by only two semiconductor elements. Besides, it is not adequate to achieve high-voltage step-up since the static gain is limited in practice considering the existence of parasitic elements. This is an assumption that can be extended to boost-based dc–dc converters, as the increase of the static gain must not rely only on the duty cycle.

As possible solutions, three-level converters allow doubling the static gain of the conventional boost converter, with prominent advantages in the reduction of size, weight and volume of the filter inductor. However, the conversion ratio is not as wide as that of cascaded converters, which on the other hand present appreciable voltage stress across the active switch. A hybrid approach may result in a quadratic three-level boost converter, but the presence of two inductors with significant dimensions may limit its application in high-power levels.

Coupled inductors provide a simple solution for high-voltage step-up by properly adjusting the respective turns ratio. However, voltage ringing often results because of the resonance between the leakage inductance and the intrinsic capacitance of the active switch, thus leading to poor efficiency even when clamping circuits are used. By using switched capacitors, it is also possible to achieve high-output voltages in a modular approach, but tradeoffs must be made between component count, efficiency and the static gain.

For high-power, high-current applications with high-voltage step-up, interleaved converters or 3SSC-based topologies are possible choices, which can typically employ coupled inductors or VMCs for this purpose. Current sharing can only be achieved in interleaved converters with complex control schemes, while it is naturally maintained in all converters based on the 3SSC because of the existence of an autotransformer with unity turns ratio. Recent works have also demonstrated the potential application of the 3SSC in the generation of novel high-voltage-step converter topologies with high efficiency.

## 5 Acknowledgments

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