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A Computational Tool for Simulation an Design of Multilevel Inverters

A. Mesquita, S[1], Antunes, F[1], Daher, S[1], C. Marins, D[1] and Oliveira Jr, D.[1]

[1] Electrical Engineering Department, Federal University of Ceará, UFC, Campus do Pici, Fortaleza- Ce, Brasil, Caixa Postal 6001, Cep: 60.455-760 Phone: +55 3366-9586 / Fax: +55 3366-574,
emails: samuelufc@gmail.com, fantunes@dee.ufc.br, sdaher@secrel.com.br, deividmarins@yahoo.com.br, demercil@dee.ufc.br

Abstract. This paper proposes an aiding tool to the design and development of multilevel inverters studies using the cascade configuration to achieve output voltage waveform shaped step with several levels. The program contribution is to aid inverter simulation using the software Pspice Orcad besides set the best switching instant of each level which work in harmonics selective elimination, contributing to a lower THD of the output voltage waveform. This software also shows a flexible code which can be automatically adapted for implementation in a microcontroller or DSP.

Key words

Simulation, Multilevel Inverters, Orcad Pspice, Efficiency.

1. Introduction

Most multilevel inverters are distinguished for their application in high power and high voltage to allow the operation its switches in lower voltage levels. However there is a big possibility these inverters are applied in medium powers, achieved in [1], which implemented a high performance inverter to be used in power autonomous systems. Normally when is desired its implementation, uses the PWM modulation ad its PD variants (phase disposition), POD (phase opposition disposition) and APOD (alternative phase opposition disposition) PS configuration (phase shifted) and the hybrid modulation [2,3,4].

One disadvantage of using of the PWM modulation applied to high powers is to increase the losses in the semiconductors (conduction and switching) which could derail the application in active filters used in harmonics and reactive compensation [8].

In addition to losses in high power, the PWM modulation can generate harmonic components of several frequencies which requires an LC filter of order greater than 2. An alternative to PWM modulation for use in medium and high power is the use of switching strategies that generates an output voltage shaped step with levels equally spaced figure 1.

Therefore, to have a good resolution in the output voltage (low THD) can be used at various levels. So this work is a contribution to implementing the strategy of switching ladder by allowing the acquisition of all time of transition from a wave output voltage for *z* levels and generate files aid the simulation of multilevel inverters with Orcad PSpice program which leads to values close to actual implementation.

2. Compositions of a sinusoidal waveform and the logic used to obtain the waveform

To maintain a low THD (total harmonic distortion) at the output voltage, the levels (+ z to -z) should be equally spaced and the z-level logic consists in structuring as the graphic fig.1.

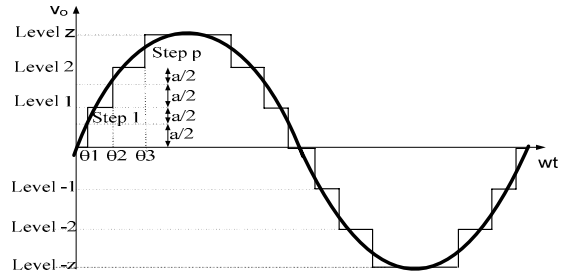


Figure 1: Multilevel waveform.

Vcc is the fixed value of each level, and Vp is the peak value of the desired waveform. Then, for the sinusoid formation, it is only necessary to know the step length in 1 / 4 of the period and the other steps are obtained by symmetry, observing that the sine wave is perfectly symmetric in the following quadrants.

The advantage of this software is the ability to easily obtain the transition times of each step, by using simple information on the amount of maximum levels in 1 / 4 of the period.

3. THD Optimization

Currently there are several types of multilevel inverters, according to studies performed in [5] the inverter that allows more levels in the output voltage with fewer components among conventional topologies is the cascaded inverter using h-bridge cells. The cascaded inverters can increase the level number in the output voltage through a combination of input dc sources of each cell arranged together by a multiplicity factor: two for the *binary configuration (1:2:4...)* or three to the *ternary configuration (1:3:9...)*, these settings are common to result in a output voltage with levels equally spaced, which does not compromise the THD [6].

Table 1 shows the comparison between the binary and ternary configuration which can be implemented without penalizing the inverters cost.

Table 1: Number of cells x number of levels in ¼ cycle.

Number of cell		2	3	4	5
*Levels or steps (P) in fourth cycle	binary	3	7	15	31
	ternary	4	13	40	121

*Number of levels (z) is same number of step (p) alone fourth cycle.

The harmonic content behavior in output voltage THD_{nopt} without the switching optimization angles is shown in fig.2.

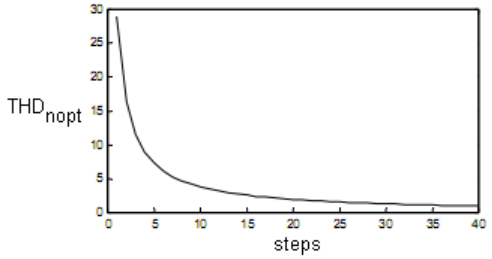


Figure 2: THD output voltage depending on the number of steps in 1 / 4 cycle of sine.

For the inverter topology shown in fig.3, the three switching angles seen can be used: one to adjust the modulation index *mi* (θ_1) (1.3) and the other two to eliminate two harmonics (θ_2 and θ_3).

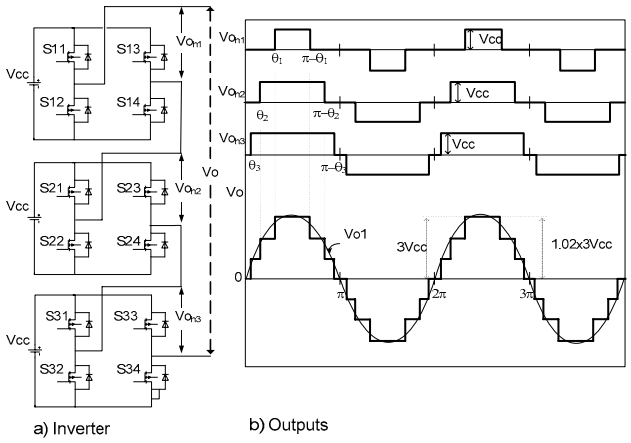


Figure 3: From top to bottom, the output voltage in the cells (Vo_{h1}, Vo_{h2} *and* Vo_{h3}) fourth cycle and the last graph in the output voltage of the inverter.

The output voltage *Vo* of the topology seen in fig.3 a), can be expressed in Fourier series terms:

$$Vo = \frac{4Vcc}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}\left[\cos(n\theta_1)+\cos(n\theta_2)+\cos(n\theta_3)\right]\sin(n\omega t) \qquad (1.1)$$

$$with \qquad 0 \le \theta_3 \le \theta_2 \le \theta_1 \le \frac{\pi}{2}$$

Where: the coefficient $4Vcc/\pi$ represents the peak value of the fundamental output voltage $Vo1_{max}$ of a H-bridge cell (eg, cell Vo_{h1}) which occurs when the switching angle θ_1 is reduced to zero, n is the harmonic order and θ_1, θ_2 e θ_3 are the switching independent angles.

The total harmonic content in output voltage can be measured by:

$$THD = \frac{\sqrt{\sum_{2}^{\infty}(Vo_{nrms})^2}}{Vo_{1rms}} = \frac{\sqrt{(Vo_{rms})^2 - Vo_{1rms}}}{Vo_{1rms}} = \frac{\sqrt{H_o^{\,2}+H_2^{\,2}+H_n^{\,2}+C}}{H1} \qquad (1.2)$$

Where: Vo_{nrms} is the rms value of the *nth* (nth-nth) output voltage harmonic order, Vo_{1rms} is the rms value of output voltage fundamental harmonic and H_n is the magnitude of each harmonic.

For a given number of step P, the staircase modulation allows to eliminate (or reduce) harmonics of higher orders by adjusting the steps transition angles, fig. 3 b). The transition angles can be programmed to override the corresponding angles to the higher order harmonics [7].

The harmonics selective elimination is commonly used in high power applications by reason of operating with fewer levels in the output voltage. However when is desired to implement the inverter average power for applications in isolated systems can be used topologies operating on many levels in the output [1], which also allow voltage regulation by eliminating or adding of levels with little THD variation, fig.4, thus eliminating the additional cost of a converter to control the DC bus.

To implement a multilevel converter with several output voltage levels, there is a costly work to be the harmonics selective elimination, $THDc_{el}$, but also in using the criterion THD_{min} of *minimum THD*, so the computational tool, fig7, helps the projects implementation with various output voltage levels and allows the designer to choose the best option, $THDc_{el}$ or THD_{min},, tables 2 and Table 3.

Because the multilevel wave to be composed of finite levels, considering the multilevel wave peak value *Vpk* (*PxDC*) equal to the reference sinusoid fig.1, the ratio of the sinusoid rms value cascading and *Vpk* /√2 is slightly different, this difference is called the modulation index *mi*:

$$mi = \frac{Vo_{RMS}}{\left(V_{pk}/\sqrt{2}\right)} \qquad (1.3)$$

Where: Vo_{rms} is the output voltage *rms* value and V_{pk} is the multilevel wave peak value, the *mi* can be used as a voltage regulation measure.

To implement the optimal control of high-resolution of the multilevel wave, can use the simultaneous use of addition and subtraction of levels to acquire the best result fig.1.

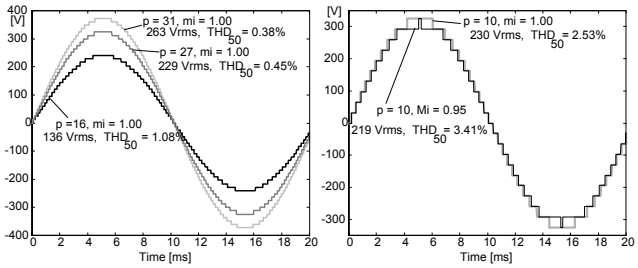


Figure 4: Method to implement the optimal control staircase.

The computational tool generates the optimum switching angles which can be used to implement the multilevel control of high resolution. The principle used to obtain them realize the variation (or scan) of the reference sinusoid by changing the amplitude determined by the factor k_f and exemplified in the steps below.

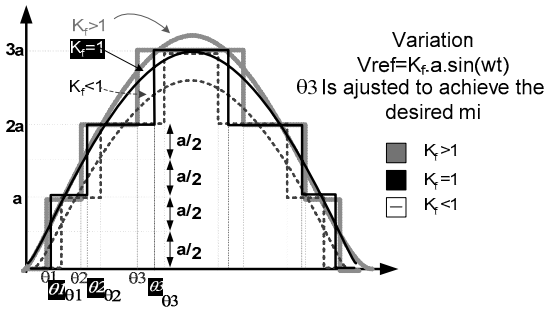


Figure 5: Flexible method of sinusoid reference used to obtain the optimized THD.

As showed, when is desired to eliminate harmonic with the inverter operating at various levels in the output voltage (63 and 81 levels) the work is costly, so the computational tool presented in figure 7 can generate

both the transition times of the steps waveform natural (without the harmonics elimination) THD_{nopt} as well the optimized times with the odd harmonics THD_{cel} elimination, or a attenuation in THD for a total of harmonics defined THD_{min} (first 90 harmonics). The diagram below shows the algorithm structure implemented to acquire the optimum angles.

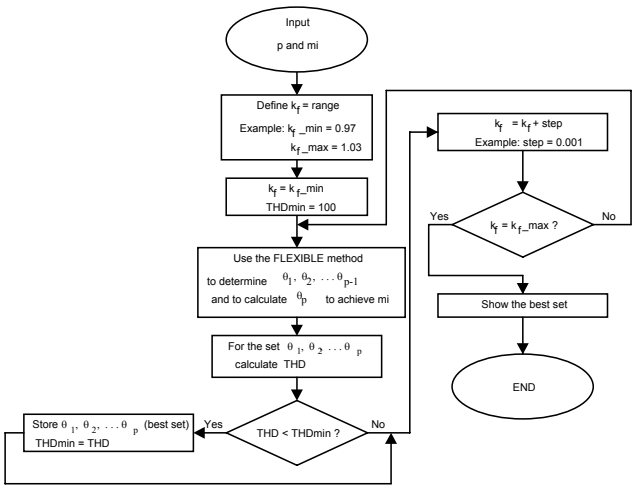


Figure 6: Algorithm for acquire the minimun THD.

Table below shows the comparison of the THD obtained with the odd harmonics elimination (THDsel) versus the natural THD (without the flexible method) for various numbers of normal level applied to high resolution multilevel inverters in the output voltage.

Table 2: THD with the odd harmonics elimination (THDsel) and THD generated without the flexible method (THD_{nopt}).

P		3	4	7	13	15	31	40
THD_{vo}	THD_{nopt}	11.61	8.75	4.93	2.48	1.92	0.56	0.35
	THD_{sel}	11.92	8.83	4.78	2.45	1.84	0.56	0.33
mi	THD_{nopt}	1.03	1.02	1.01	1.00	1.00	1.00	1.00
	THD_{sel}	1.04	1.02	1.02	1.01	1.01	1.00	1.00

The following table shows the harmonic content obtained by the criterion of minimum THD.

Tab.3: Minimum THD obtained for the various types of *p* usual.

P	3	4	7	13	15	20	31	40
THD_{min}	11.15	8.45	4.71	2.44	1.78	0.699	0.56	0.32
Mi	1.04	1.03	1.03	1.01	1.01	1.01	1.00	1.00

4. Computational tool for development of the steps compounding the sinusoidal wave in staircase

The proposed software tool has been developed in C language, and it is composed by two computational programs. The first one treats the waveform (Fig.7), and has the basic function of producing the time of transitions of every step of the sine wave.

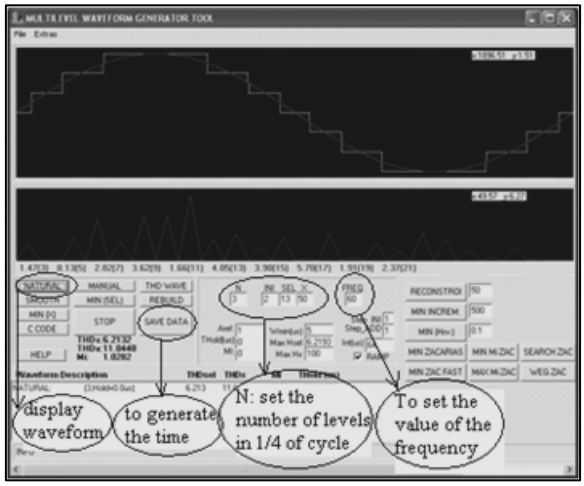


Figure.7 Environment interface: sine wave treatment unit, generator of the transition times of the sine staircase levels.

These time of transitions are used to determine which switches will be driven in order to produce the inverter output voltage waveform, as seen in fig.8.

For each transition time there the software determines which switches will be driven in such a way to produce the desired multilevel output voltage.

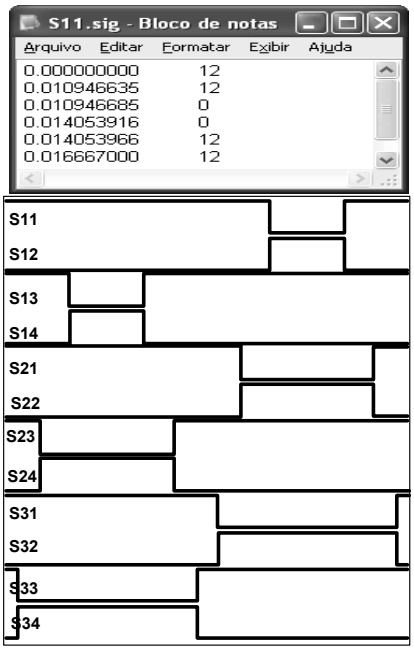
The second program imports and compile a .txt file (fig.8) which function are to show at the monitor screen the driven pulses of the switches and to generate the files *.sig* (fig.9) which will be imported by the Orcad Pspice, through the VPWL_FOREVER function.

Pseudo code z=7 level, file .txt : topology shown in figure3 a),:

```
% Comments
% Pseudo – code, for 7 levels fig. 3 (n=3 in the ¼ of the cyclo)
% Initial (I) command states: Level of the switches:
% H=high, L=Low
I  11=H 12=L 13=H 14=L;
I  21=H 22=L 23=H 24=L 31=H 32=L 33=H 34=L;
% General Settings
% Period,    dead time,    rise/fall,   drive volt.
S 16.667e-3   2000e-9       100e-9       12;
% Transition (T) <time in seconds> switch= b, e, a
%b: before, a: after (b/a=-/+dead time); e:exact dead time
T 0.000444188          33=e                    34=a;
T 0.001388896          23=e                    24=a;
...
```

Fig. 8 Programming the drive switches on each level, e.g. switch S11=11 level high exact time transition, see fig9: a) and d).

a)



b)

Fig.9: b) File .sig imported by through the VPWL_FOREVER function; c) monitor screen the driven pulses of the switches.

A. The contribution/advantages of using this software are:

1) It allows simulation of all multilevel inverter topologies for *z* level in Orcad Pspice program which shows a simulation with closer results to the real structure.
2) The code is portable, or easily adaptable for digital implementation.
3) It facilitates a better efficiency of the converter by adjusting the optimal dead time between two switches of the same arm mutually complementary to each other. This is done based on semiconductor technologies, which provide the minimum ascent time and minimum descent time (change state, on/off). This adjustment is hardly ever achieved through ordinary means such as PWM.
4) It is an excellent tool to help professors during multilevel inverter classes and tasks about digital implementation.

5.0 Simulation results and software validation with the utilization of Orcad Pspice program in many multilevel topologies

The fig.7 shows the interface of the program generating a sine wave, structured in C Language. This tool makes it possible the simulation and development of any multilevel inverter which output waveform has *z* level as seen in fig.1. Below some examples of simulations of inverters obtained with the help of the proposed computational tool is seen in fig.3.

The output voltage with 81 levels has also been obtained, it's showed in the figure below:

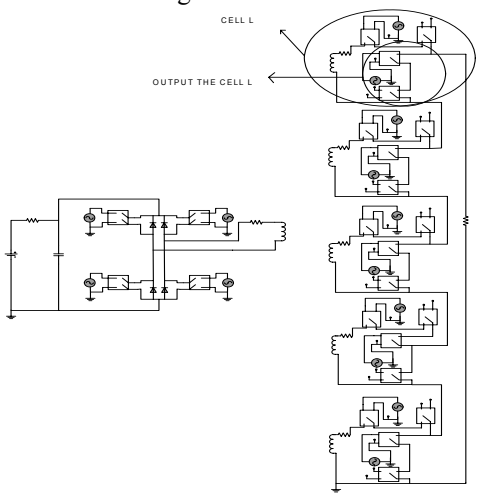


Fig.10 Simulate inverter employed by [1] with 63 levels (+z to –z) in output voltage, simulated with input voltage of 48V, and output 220-1kVA (waveform: fig.12).

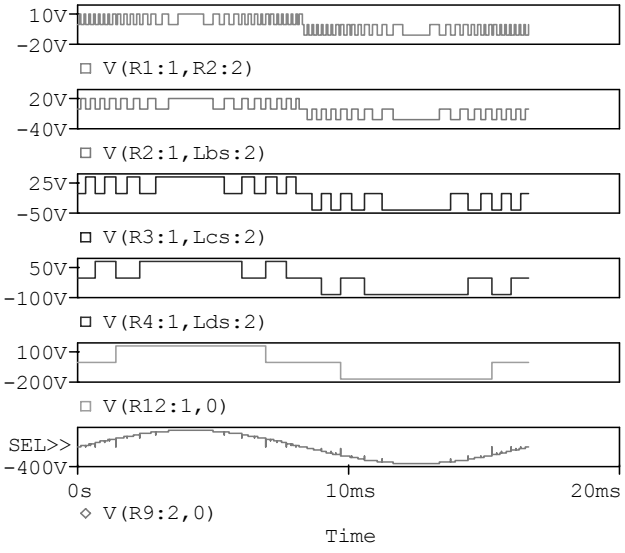


Fig.11: Waveforms from the first to the fourth graphic, in the output, from first to last cell L (fig. 11). Last graphic is a sine curve, with output voltage in linear load (R).

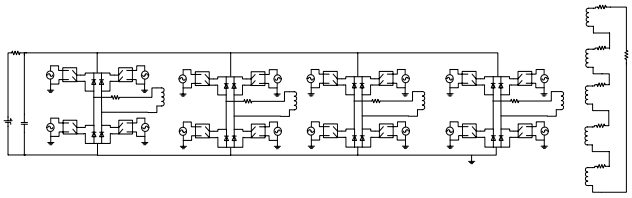


Fig.12: Topology simulated with the ternary configuration with 81 levels (+z to –z) in the output voltage (waveform: fig. 14).

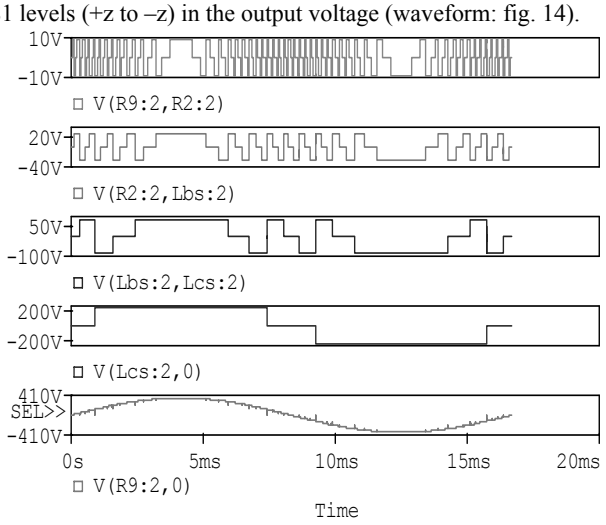


Fig.13 The first to the fourth graphics show voltages in secondary windings, respectively, from first to last using the secondary configuration ternary. Last graphic: output voltage waveform, operating in 220VA 1kVA.

6.0 Conclusion

Concluded that the software was effective in helping multilevel inverters simulation with several voltage levels (63 and 81 levels) because produce all output voltage transition times by a simple information on the levels number in a sine quarter-cycle, and generate the best switching times to allow the some harmonics elimination in the output voltage and promote a output voltage level with less harmonic content as possible. With a few steps it is possible to generate the files pulses needed for multilevel inverters simulation in any version of Orcad PSpice allowing development of studies and analysis of the inverters multilevel behavior. This software allows setting the switches pulses (rise time and fall time) according to semiconductor technology which increases the converter efficiency by reducing switching losses. It also provides a code easily adaptable for implementation in a microcontroller or DSP used in inverter control.

Acknowledgments

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