A Bidirectional Single Stage AC-DC Converter with High Frequency Isolation Feasible to DC Distributed Power Systems

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Abstract— **This paper proposes a single-phase bidirectional ac-dc converter feasible to dc distributed power systems. The topology provides galvanic isolation and is able to protect the system during short-circuits occurrence in the load side. The power factor control in the ac side is performed by the duty cycle variation in the primary bridge. It is supposed to regulate the dc bus voltage even during voltage dips and short-circuits. The secondary side bridge is driven with constant duty cycle and the power flow is controlled by the variation of the phase shift angle between the two bridges. The basic equations are shown and the simulation results are presented and discussed.**

I. INTRODUCTION

With the expansion of the Distributed Generation (DG) reinforced by the renewable energies in the last decades, the concept of Smart Grids (SG) comes to allow the integration of distributed sources to the main grid utility with certain feedback from the consumers and a more characteristic intelligent [1]-[3]. This concept is based on the concept of six principal axes: advanced metering infrastructure to improve demand-side management, energy efficiency to make the business more profitable, great adaptability for different scenarios, self-healing electrical grid to make the system more robust, improved supply reliability and adequate response to severe faults and natural disasters [4]. Indeed, there is the necessity of a smart system able to deliver energy efficiently by using the integration of advanced technologies such as communication, information technologies [5], electronics and new materials [6] joining forces to maintain an environmentally sustainable system.

In order to make distributed power systems feasible, power electronic converters must be fault tolerant. For example, let us consider Fig. 1. During a short-circuit in the residence, the main power supply must remain connected during a time interval long enough to drive the local protection device, which will isolate the fault in the circuit without interrupting the supply to the remaining consumers.

Rectifiers with Power Factor Correction (PFC) are widely used in electronic equipment in both commercial and industrial environments. They meet the requirements of standards related to power quality, providing stable DC voltages to be processed by converters connected to the loads [7]-[9].

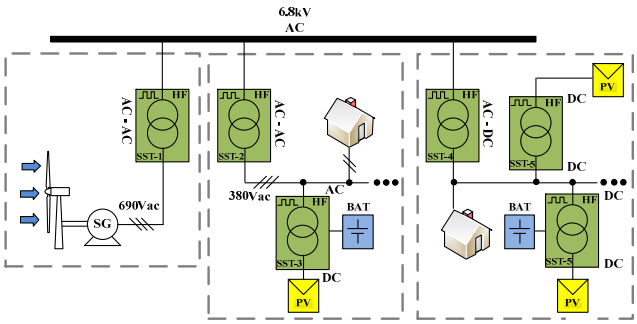

Fig. 1 Typical distributed power system.

Additionally, bidirectional power flow is expected in power converters used in generated distribution. Moreover, the topology is supposed to aggregate reactive power compensation and voltage sag restorer characteristics [6]. However, recent proposals for dc power systems [10]-[12] do not comprise with such characteristics, since they are based on the traditional bidirectional PWM boost rectifier, which is not able to handle short-circuits in the dc side and also does not provide galvanic isolation. The work described in [13] presents a survey on Solid State Transformers (SST).

Concepts employing three-state switching cell allow good distribution of losses between the semiconductors and reduction of high frequency harmonic content for both voltages and currents. Thus, it leads to the decrease of current RMS levels for the output capacitors, increasing system reliability due to lower operating temperatures. The volume of magnetic is also reduced, with consequent reduction of the very dimensions and losses of the converter. The use of the three-state switching cell also reduces switching and conduction losses due to the power divided among the various components. The disadvantages are the increase in the number of semiconductors in the prototype, necessary to the design

and implementation of gate drivers, with consequent practical difficulties in the system layout [14].

The PFC rectifier employing the three-state switching cell represents a fairly new technology. The concept employed in single-phase rectifiers has been proposed in [15].

Fig. 2a shows the arrangement based on a bidirectional version of the three-state switching cell [15], where a secondary winding can be coupled with transformer T1. In order to avoid transformer saturation, the legs are phase-shifted by 180° and the individual currents must be monitored. Fig. 2b shows an alternative configuration, where the secondary side can be coupled with the transformer T2 and saturation can be avoided by using a series capacitor. Another similar configuration can be obtained using the interleaving technique. The secondary windings may be coupled to inductors L1 and L2, as shown in Fig. 2c, or use a separate core, as seen in Fig. 2d.

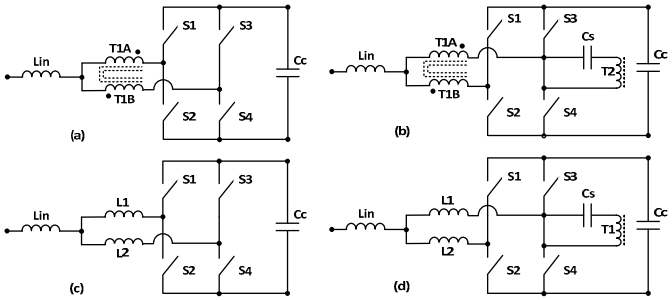

Fig. 2 - Basic Cells: (a) Bidirectional three-state cell with a transformer. (b) Bidirectional three-state cell with a separate transformer. (c) Interleaved bidirectional boost cell. (d) Interleaved bidirectional boost cell with separate transformer.

The topology proposed in this paper is a bidirectional ac-dc single phase SST, isolated by high frequency stage. The variation of the duty cycle on the primary bridge is responsible for the Power Factor Correction (PFC) . The phase shift angle between two bridges controls the power flow through the converter even with voltage dips. Besides, the dc primary bus voltage is regulated.

It has the following advantages: ability to operate at high power levels, high efficiency, low ripple current in both the input and the output sides, reduced volume and size of the input inductor, which ensures reduced losses, weight lower volume.

Due to the bidirectionality and PFC, the system allows the converter to act as an inverter for the interconnection of any dc power source to the grid.

II. PROPOSED TOPOLOGY

Fig. 3 presents the proposed topology. It was obtained from the combination of the dual active bridge converter with the bidirectional three-state switching cell (Fig. 2a), using the half-bridge configuration in the secondary side. According to [16], the power flow between the primary and secondary sides can be controlled by the phase-shift angle φ between the two bridges. Also, the PFC is perfomed by the duty cycle variation in the primary bridge.

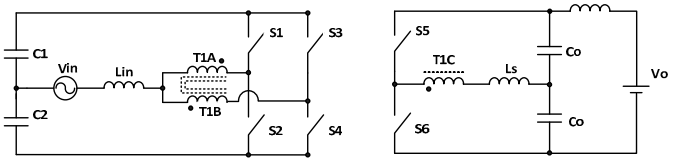

Fig. 3. Single-phase ac-dc solid state transformer.

The mathematical analysis will be developed from the elementary dc/dc converter. Thus, all possible regions of operation of the ac/dc will be properly identified..

From the theoretical analysis, the equations of the static gain that relate the output current and the input voltage for different duty cycles and phase shift angles are obtained for each condition of phase-shift angle φ and duty cycle D.

All possible regions of operation are shown in Table I. In each region, there are six stages of operation, which are defined by the switches' states and the resulting topologic configuration.

TABLE I – Regions of Operation.

REGION	CONDITION
1	$\emptyset < D \; and \; D < 0.5$ and $\emptyset \geq 0$
2	$\emptyset > D \; and \; D < 0.5 \; and \; \emptyset \geq 0$
3	$\emptyset < (D - 0{,}5) \; and \; D \geq 0{,}5 \; e \; \emptyset \geq 0$
4	$\emptyset \geq (D - 0{,}5) \; and \; D \geq 0{,}5 \; e \; \emptyset \geq 0$
5	$\lvert\emptyset\rvert < (0{,}5 - D) \; and \; D < 0{,}5 \; e \; \emptyset < 0$
6	$\lvert\emptyset\rvert < (1 - D) \; and \; D \geq 0{,}5 \; e \; \emptyset < 0$
7	$\lvert\emptyset\rvert \geq (0{,}5 - D) \; and \; D < 0{,}5 \; e \; \emptyset < 0$
8	$\lvert\emptyset\rvert \geq (1 - D) \; and \; D \geq 0{,}5 \; e \; \emptyset < 0$

A. First Region

The six stages in this region are shown in Fig. 4 and Fig. 5. The first stage can be seen in Fig. 4a. Switches S2, S3 and S6 are turned on. In the primary side, the current flows through S2 and S3 and the input inductor is discharging. At the secondary side, the current flows through the anti-parallel diode of switch S6. When switch S2 turns off and S1 turns on, the current through the input inductor starts increasing and the current flows through switch S3 and the anti-parallel diode of switch S1. The current keeps flowing through the anti-parallel diode of switch S6 until the current through the leakage inductance becomes null. After that, the current starts to flow through S6. That is the second stage and it can be seen in Fig. 4b. Fig. 4c shows the third stage of operation in the first region. The current flows through switches S1 and S4 and through the input inductor and the bus capacitor starts discharging. At the secondary side, the current flows through S6. Fig. 6a shows the fourth stage. The current keeps flowing through the switches S1 and S4, and the input inductor and the bus capacitor keep discharging. At the secondary side, the

current starts flowing through the anti-parallel diode of the switch S5. Fig. 6b shows the fifth stage of operation. The current through the input inductor starts increasing and the current flows through switch S1 and through the anti-parallel diode of switch S3. The current keeps flowing through the anti-parallel diode of switch S5 until the current through the leakage inductance becomes null. After that, the current starts flowing through S5. Fig. 6c shows the sixth stage of operation. In the primary side, the current flows through S2 and S3 and the input inductor is discharging. At the secondary side, the current flows through S5. The three stages in Fig 4 are responsible for the decrease of the current in the leakage inductance, and the remaing stages in Fig. 6 are responsible for the respective decrease.

Fig. 5 shows the equivalent circuit for the first stage of operation. For the remaining stages, the polarity of the input and/or output voltage sources changes accordingly.

Fig. 7 shows the gating signals for switches S1, S3, and S5 and the current through the leakage inductor for Region 1. Fig. 8 shows the same waveforms for Region 3.

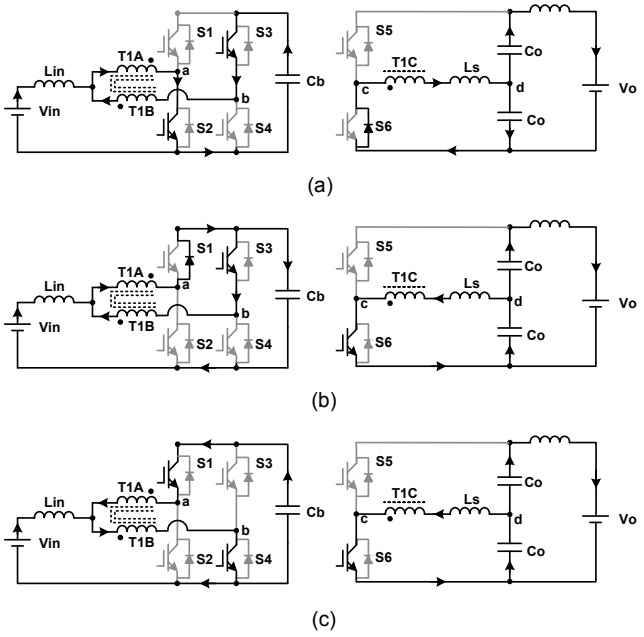

Fig. 4. First three topological stages associated to region 1.

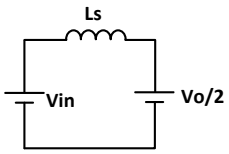

Fig. 5. Equivalent dc circuit for the first stage.

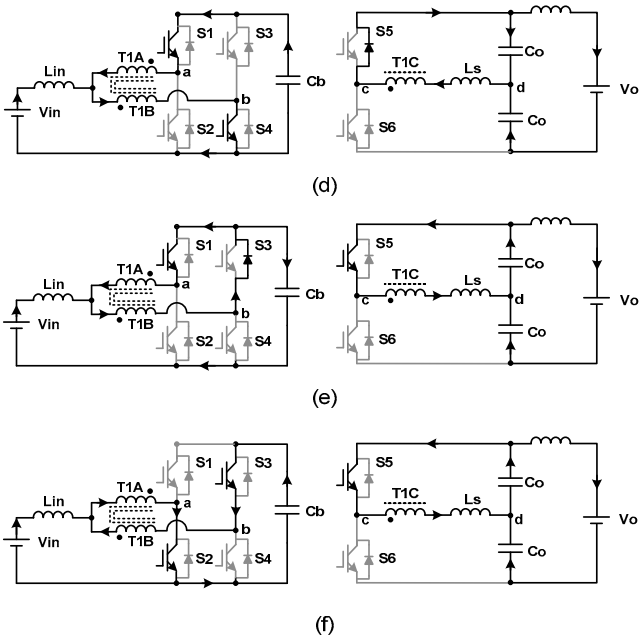

Fig. 6. Final three topological stages associated to region 1.

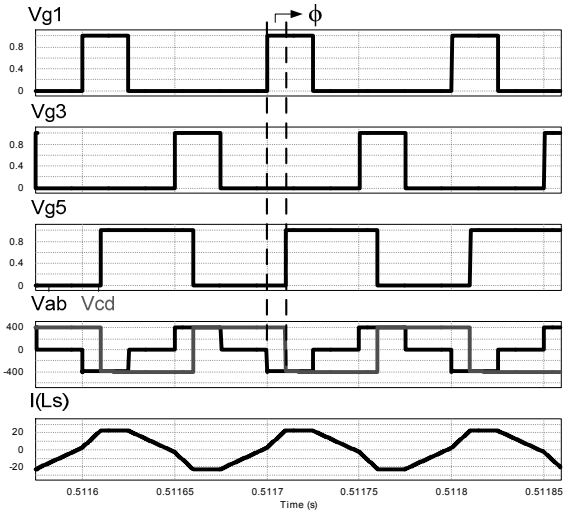

Fig. 7. Gating voltages, voltages through coupled inductors and current through the leakage inductance for region 1.

1) First Stage

The first stage occurs when switches S2, S3 and S6 are turned on. In that condition, the voltage through the input inductance is $-V_{in}$ and the output voltage is $-{}^{V_0}/_2$. The time interval for this stage is given by $(D-\phi).T_S$.

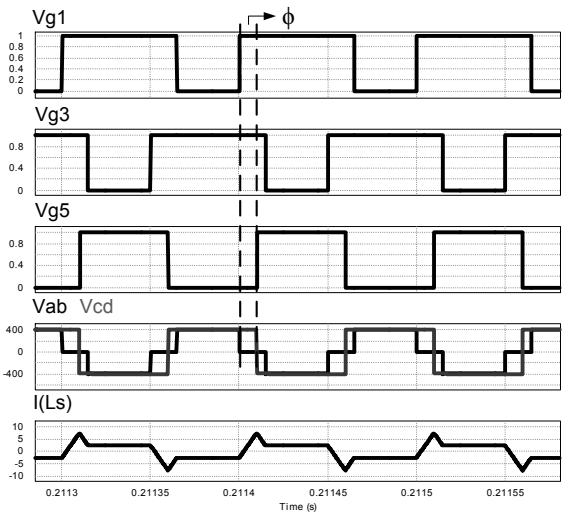

Fig. 8. Gating voltages, voltages through the coupled inductors and current through leakage inductance for Region 3.

The current is given by (1).

$$i(t) = I_0 + \frac{V_{in} - \frac{V_0}{2}}{L}.t \quad (1)$$

Where I_0 is the initial current value, Vin is the dc bus voltage, L is the input inductor and V_0 is the output voltage.

2) Second Stage

The second stage occurs when switches S1, S3, and S6 are turned on. In this case, the voltage through the input inductance is 0 and the output voltage is $-V_0/2$. The time interval for this stage is given by (0.5–D).T_S.

The current is given by (2).

$$i(t) = i(\Delta t_1) - \frac{V_0}{2.L}.t \quad (2)$$

Where $i(\Delta t_1)$ is the final current value of the first stage.

3) Third Stage

The third stage occurs when switches S1, S4, and S6 are turned on. In this case, the voltage through the input inductance is $+V_{in}$ and the output voltage is $-V_0/2$. The time interval is given by $\phi.T_S$.

The current is given in (3).

$$i(t) = i(\Delta t_2) - \frac{V_{in} + \frac{V_0}{2}}{L}.t \quad (3)$$

Where (Δt_2) is the final current value of the second state.

The remaining three states are similar to the first three but with sign reversed. It means that the final current in the third stage is $-I_0$ and the final current in the sixth stage is I_0.

The static gain can be obtained considering the voltage through the leakage inductance and the respective time intervals.

$$I_0 = \frac{V_0 - 4.D.V_{in} + 8.V_{in}.\phi}{8.L.f_s} \quad (4)$$

Where f_s is the switching frequency, D is the duty cycle, and ϕ is the phase-shift angle between the two bridges.

Then, it is possible to obtain the average output current value for this region as:

$$I_0 = \frac{V_{in}}{4f_S L}.(4D\phi - 2D^2 + D - 4\phi^2) \quad (5)$$

The same procedure realized for the first region can be performed in order to obtain the static gain for the remaining seven ones.

B. Second Region

The static gain is given in equation (6).

$$I_0 = \frac{V_{in}}{4f_S L}.D.(2D - 4\phi + 1) \quad (6)$$

C. Third Region

The static gain is given in equation (7).

$$I_0 = \frac{V_{in}}{4f_S L}.(1 - D).(4\phi - 2D + 1) \quad (7)$$

D. Fourth Region

The static gain is given in equation (8).

$$I_0 = \frac{V_{in}}{4f_S L}.(4D\phi - 2D^2 + D - 4\phi^2) \quad (8)$$

E. Fifth Region

The static gain is given in equation (9).

$$I_0 = \frac{V_{in}}{4f_S L}.(1 - 4|\phi| - 2D) \quad (9)$$

F. Sixth Region

The static gain is given in equation (10).

$$I_0 = \frac{V_{in}}{4f_S L}.(4D|\phi| + 2D^2 - 3D + 4|\phi|^2 - 4|\phi| + 1) \quad (10)$$

G. Seventh Region

The static gain is sho given wn in equation (11).

$$I_0 = \frac{V_{in}}{4f_S L}.(4D|\phi| + 2D^2 - 3D + 4|\phi|^2 - 4|\phi| + 1) \quad (11)$$

H. Eighth Region

The static gain is given in equation (12).

$$I_0 = \frac{V_{in}}{4f_S L}.(4|\phi| - 2D^2 + 5D - 4D|\phi| - 3) \quad (12)$$

As it can be seen in Fig. 9, the steady state output current does not depend on the output voltage. Therefore, during output short-circuit condition, even considering open loop operation, the output current is maintained after the transient discharge of output capacitor C_o. Thus, the converter is naturally fault tolerant and feasible to distribution systems.

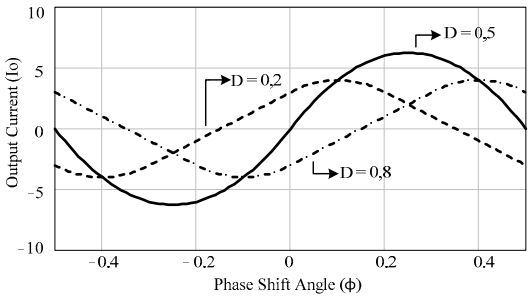

Fig. 9. Static gain curve of the dc-dc SST.

The ac input voltage source and the input power factor correction introduce a 120-Hz component in the output current. By solving (5)-(12) in order to obtain the correct values of D and Φ for a constant steady state output current, the curve shown in Fig. 10 results. So, theoretically, the 120-Hz ac component imposed by the duty cycle variation can be mitigated by the adequate choice of the of phase-shift angle Φ.

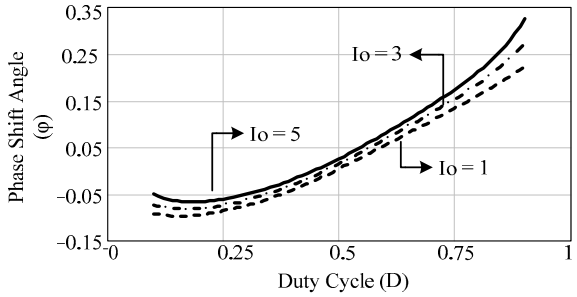

Fig. 10. D and Φ values for a constant steady state output current.

III. Simulation Results

The simulation of the circuit presented in Fig. 3 was performed and the specifications and parameters used to implement the prototype are shown in Table II.

The results for a step-up in the phase-shift angle can be seen in Fig. 11. The current is drawn from the power supply with unity power factor and low harmonic content as shown in Fig. 11(a). Fig. 11(b) demonstrates that the output current increases when φ is changed, but the ripple current is high because a control strategy for the ripple mitigation has not been implemented. Fig. 11(c) shows the dc bus voltage during this simulation. Fig. 12(a), (b), and (c) shows the input current, the output current, and the primary dc bus voltage during a short-circuit circuit in the output side, respectively.

TABLE II – Simulation Specifications and Parameters

PARAMETER	SPECIFICATION
Input Voltage	127 Vrms
Output Voltage	800 Vdc
Switching frequency	10 kHz
Input inductor	1.5 mH
Output Power	1 kW

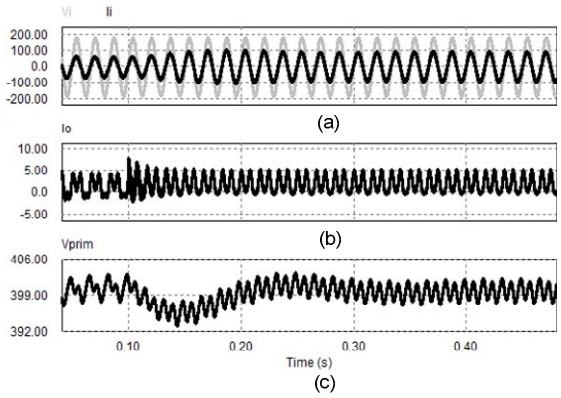

Fig. 11. (a) Input current and input voltage (b) output current (c) bus voltage.

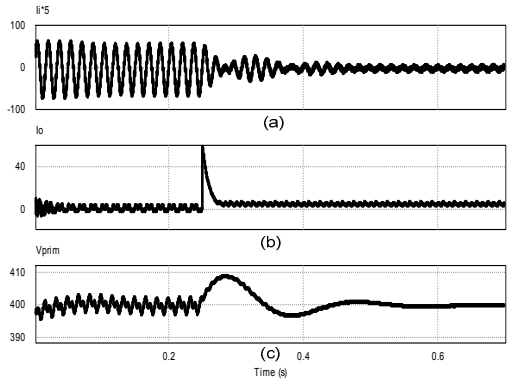

Fig. 12. (a) Input current during short-circuit (b) output current (c) bus voltage during short-circuit.

IV. Similar Topologies

A. AC-DC Configurations

From the basic concept introduced in this paper, many topologies with similar characteristics can be derived. For example, Fig. 13 shows that a full-bridge configuration can also be used in the secondary side. Then, the current stress in the secondary side switches is reduced and high power capability can be obtained. Besides, current source characteristic is obtained. Fig. 14 presents a double full-bridge

associated with the three-state switching cell resulting in a higher power configuration. Finally, the three-phase configuration is presented in Fig. 15.

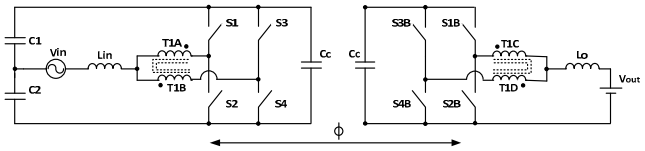

Fig. 13. AC-DC converter with a full-bridge in the secondary side.

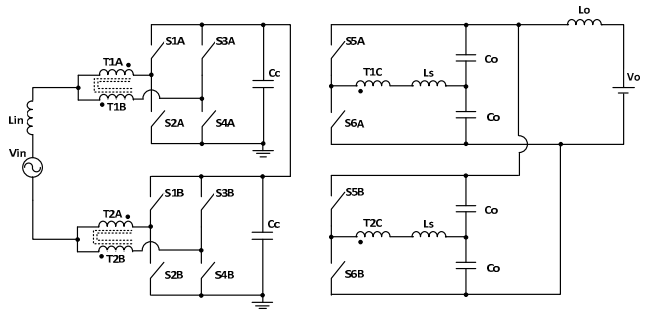

Fig. 14. AC-DC converter with a double full-bridge in the primary side.

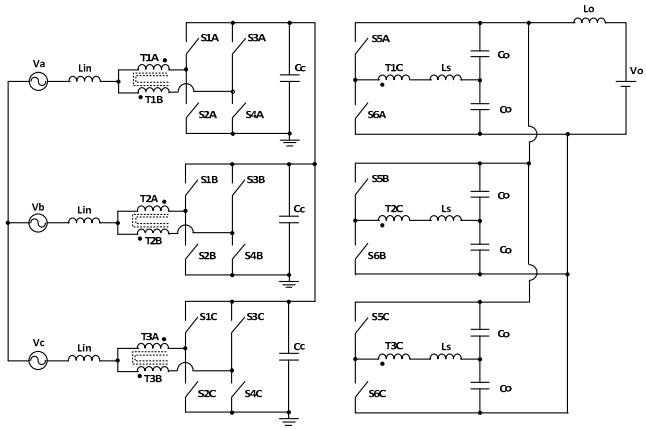

Fig. 15. Three-phase AC-DC configuration.

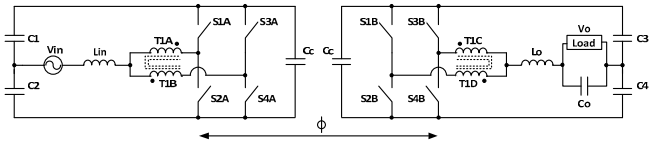

Fig. 16. One phase AC-AC converter.

B. AC-AC Configurations

Similarly, AC-AC topologies with similar characteristics can be obtained. For example a single-phase AC-AC configuration is obtained in Fig. 16. Then, the three-phase configuration can also be obtained as in Fig. 17. The presented AC-AC topologies allow the development of new alternatives to topologies for solid-state transformers. The analysis of multilevel versions for this basic topology is the next step in this study.

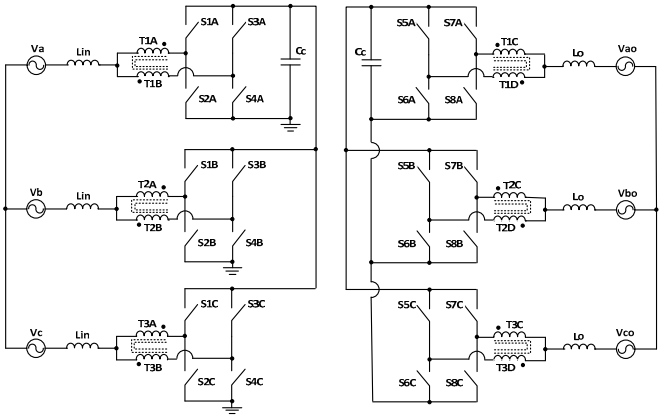

Fig. 17. Three-phase AC-AC converter.

V. CONCLUSION

This paper has presented a single-stage ac-dc topology feasible to dc distribution power systems. The theoretical analysis was developed and the simulation results validate the principle of operation. As a result, a single stage AC-DC conversion with high frequency isolation was achieved. This topology is the basis of three-phase, AC-AC and multilevel versions that allow the implementation of a real solid state transformer. The main advantages of the converter are the good performance during short-circuits and transients.

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